LOW EMI CLOCK GENERATOR

ICS4231-03

Description

The ICS4231-03 generates a low EMI output clock from a clock or crystal input. The device uses ICS' proprietary mix of analog and digital Phase Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

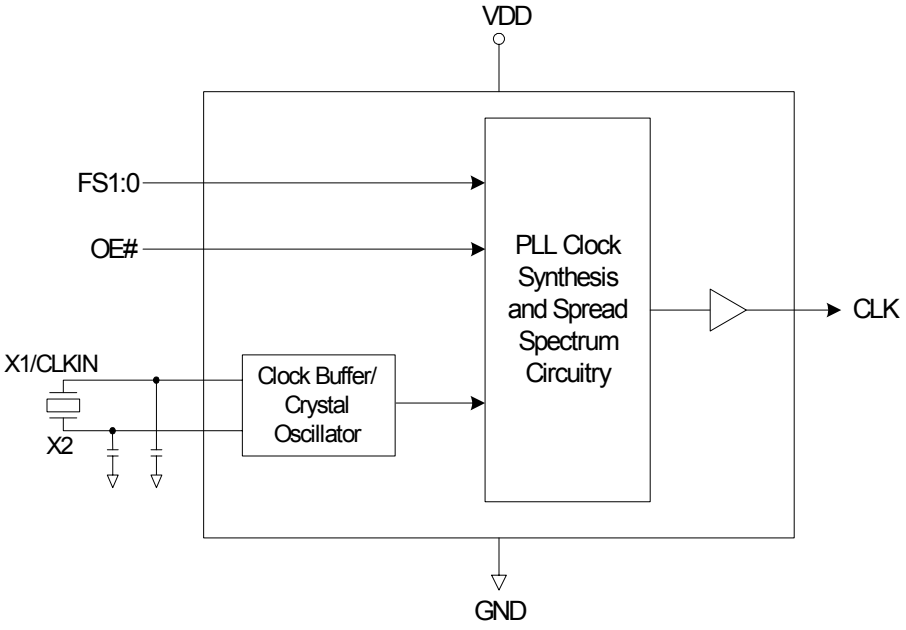
The ICS4231-03 offers four different center and down spread selections. Refer to the MK1714-01/02 for the widest selection of input frequencies and multipliers.

ICS offers a complete line of EMI reducing clock generators. Consult us when you need to remove crystals and oscillators from your board.

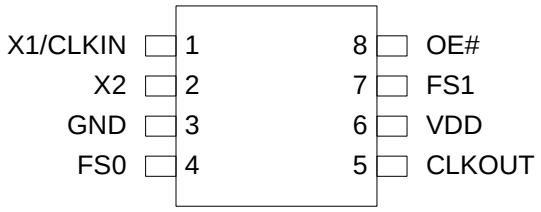
Features

- Pin and function compatible to Cypress W42C31-03
- Packaged in 8-pin SOIC (Pb free available)
- Provides a spread spectrum output clock
- Accepts a clock or crystal input and provides same frequency dithered output
- Input clock frequency of 10 to 33 MHz
- Peak reduction by 8dB - 14dB typical on 3rd - 19th odd harmonics
- Spread percentage selections of ±1.875%, ±1.0%, and -2.0%
- Operating voltage of 5V
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8 pin (150 mil) SOIC

Output Enable Function Table

OE# (Pin 8)	Output Status
0	Running
1	Tri-state

0 = connect to GND
1 = connect directly to VDD
Note: OE# pin has an internal pull-down resistor

Frequency Range and Spread Table

FS1 (Pin 7)	FS0 (Pin 4)	Clock Input Frequency (MHz)	Crystal Input Frequency (MHz)	Spread Amount
0	0	10-20	10-20	±1.875%
0	1	10-20	10-20	±1.0%
1	0	20-33	20-25	±1.875%
1	1	20-33	20-25	-2.0%

Note: FS1:0 have internal pull-up resistors

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal or Clock Input.
2	X2	Output	Crystal output. Float for a clock input.
3	GND	Power	Connect to ground.
4	FS0	Input	Select pin for input frequency and spread amount. See table above. Internal pull up resistor.
5	CLKOUT	Output	Spread spectrum clock output per table above.
6	VDD	Power	Connect to 5V.
7	FS1	Input	Select pin for input frequency and spread amount. See table above. Internal pull up resistor.
8	OE#	Input	Output Enable. Active Low. See table above. Internal pull-down resistor.

External Components

The ICS4231-03 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 6 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

value of these capacitors is given by the following equation:

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS4231-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS4231-03. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

DC Electrical Characteristics

Unless stated otherwise, VDD = 5V, ±10%, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.5	5	5.5	V
Supply Current	IDD	No load, at 3.3V		18	32	mA
Input High Voltage	V_{IH}		0.7VDD			V
Input Low Voltage	V_{IL}				0.15VDD	V
Output High Voltage	V_{OH}	I_{OH} = -24mA	2.5			V
Output Low Voltage	V_{OL}	I_{OL} = 24mA			0.4	V
Input Capacitance	C_{IN}	All pins except X1, X2		5	7	pF
Load Capacitance		X1, X2, as seen by the xtal, Note 1		17		pF
Output Impedance	Rout			20		Ω
Input Pull-Up Resistor				500		KΩ
Power-Up Time		First locked clock cycle after Power Good			5	ms

Note 1: Pins X1 and X2 each have 34 pF capacitance. When used with a crystal, the total combined capacitance as seen by the crystal is 17 pF. If driving X1 with a clock input, the load capacitance will be 34 pF.

AC Electrical Characteristics

Unless stated otherwise, VDD = 5V±10%, Ambient Temperature 0 to +70° C, C_L=15pf

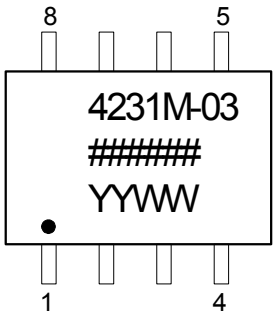
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency		Input Clock	10		33	MHz
Output Frequency			10		33	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Note 1	45	50	55	%
Output Rise Time	t_{OR}	0.8 to 2.4V, note 1		2	5	ns
Output Fall Time	t_{OF}	2.4 to 0.8V, note 1		2	5	ns
Jitter		cycle-to-cycle			300	ps
Harmonic Reduction			8			dB

Note 1: Measured with 15pF load

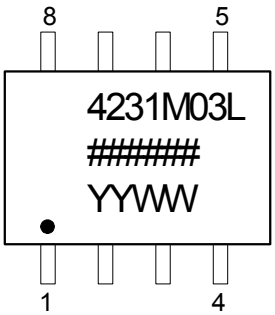
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram



Marking Diagram (Pb free)

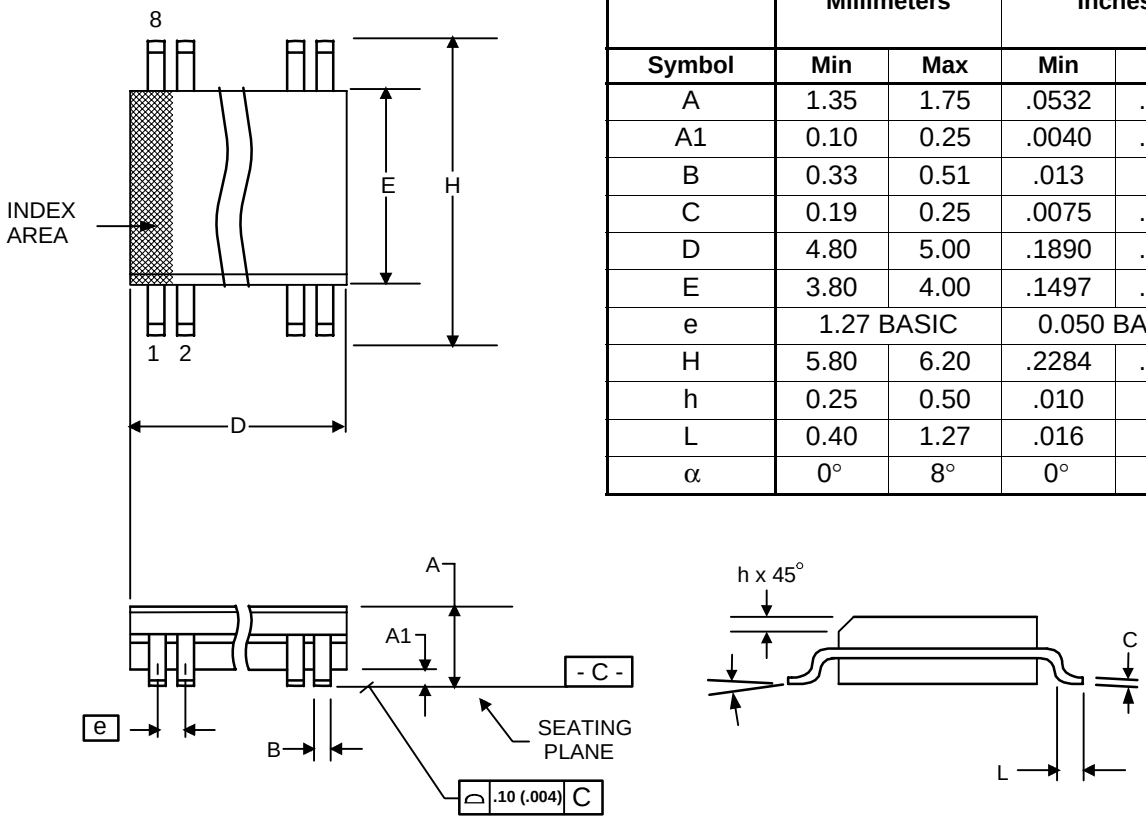


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “L” denotes Pb (lead) free package.
4. Bottom marking: country of origin.

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
4231M-03	see page 5	Tubes	8-pin SOIC	0 to +70° C
4231M-03T		Tape and Reel	8-pin SOIC	0 to +70° C
4231M-03LF		Tubes	8-pin SOIC	0 to +70° C
4231M-03LFT		Tape and Reel	8-pin SOIC	0 to +70° C

"LF" denotes Pb free packaging.

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