# PECL TO CMOS CONVERTER

#### DATASHEET

#### **ICS508**

### Description

The ICS508 is the most cost effective way to generate a high quality, high frequency CMOS clock output from a PECL clock input.

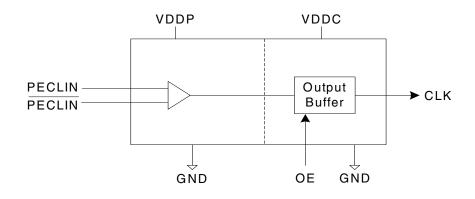
The ICS508 has separate VDD supplies for the PECL input buffer and the output buffer, allowing different voltages to be used. For example, the input clock could use a 3.3 V supply while the output operates from 2.5V.

The device has an Output Enable pin that tri-states the clock output when the OE pin is taken low.

The ICS508 is a member of IDT's ClockBlocks<sup>TM</sup> family.

#### Features

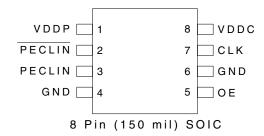
- Packaged in 8 pin SOIC (Pb-free) or die
- Separate VDD supplies allow voltage translation
- Clock frequency of 0 250 MHz
- Duty cycle of 45/55
- Operating voltages of 2.375 to 5.5V
- Tri-state output for board level testing
- 24mA output drive capability
- Industrial temperature version available
- Advanced, low power, sub-micron CMOS process



### **Block Diagram**

1

# **Pin Assignment**



# **Pin Descriptions**

Pin Number	Pin Name	Pin Type	Pin Description
1	VDDP	Output	Connect to 3.3V or 5V. Supplies PECL input buffer.
2	PECLIN	Input	Complementary PECL clock input.
3	PECLIN	Input	PECL clock input.
4	GND	Power	Connect to ground.
5	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up to VDDC.
6	GND	Power	Connect to ground.
7	CLK	Output	Clock output.
8	VDDC	Power	Connect to 2.5 V, or 3.3 V, or 5 V. Supplies output buffer and OE pin.

### **External Components**

The ICS508 requires two  $0.01\mu$ F decoupling capacitors to be connected between VDDP and GND and between VDDC and GND. They must be connected close to the ICS508 to minimize lead inductance. A  $33\Omega$  series terminating resistor can be used next to the CLK pin.

# **Absolute Maximum Ratings**

Stresses above the ratings listed below can cause permanent damage to the ICS508. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDDP and VDDC	7 V
PECL Inputs	-0.5 V to VDDP+0.5 V
Clock Output and OE Pin	-0.5 V to VDDC+0.5 V
Ambient Operating Temperature, ICS508	0 to +70° C
Ambient Operating Temperature, ICS508MI	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

# **Recommended Operation Conditions**

Parameter	Min.	Тур.	Max.	Units
Ambient Operating Temperature, ICS508M	0		+70	°C
Ambient Operating Temperature, ICS508MI	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

# **DC Electrical Characteristics**

**VDDP = VDDC =3.3V ±5%**, Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Operating Voltage	VDD	VDDP	3		5.5	V
	VDD	VDDC	2.375		5.5	V
Peak to Peak Input Voltage		PECLIN	0.3		1	V
Common Mode Range		PECLIN VDDP = 5 V	VDDP - 3.7		VDDP - 0.6	V
		PECLIN VDDP = 3.3 V	VDDP - 2.0		VDDP - 0.6	V
Input High Voltage	V <sub>IH</sub>	OE only	2		VDDC	V
Input Low Voltage	V <sub>IL</sub>	OE only			0.8	V

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Output High Voltage	V <sub>OH</sub>	VDDC = 5 V IOH = -24 mA	VDDC - 0.4			V
		VDDC = 3.3 V IOH = -18 mA	VDDC - 0.4			V
		VDDC = 2.5 V IOH = -8 mA	VDDC - 0.4			V
Output Low Voltage	V <sub>OL</sub>	VDDC = 5 V IOL = 24 mA			0.4	V
		VDDC = 3.3 V IOL = 18 mA			0.4	V
		VDDC = 2.5 V IOL = 8 mA			0.4	V
On Chip Pull-up Resistor	R <sub>PU</sub>	OE		250		kΩ
Operating Supply Current	IDDP	100 MHz, no load		1.5		mA
	IDDC	100 MHz, no load		8		mA

Note 1: VDDP must always be greater than or equal to VDDC

# **AC Electrical Characteristics**

VDDP = VDDC = 3.3V±5%, Am	bient Temperature 0 to +70° C, unless stated otherwise
---------------------------	--

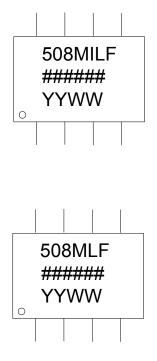
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Input Frequency	f <sub>IN</sub>		0		250	MHz
Output Clock Rise Time	100 MHz	0.8 V to 2.0 V, VDDP=VDDC = 5 V		0.4		ns
	100 MHz	0.8 V to 2.0 V, VDDP=VDDC=3.3 V		0.6		ns
	100 MHz	0.8 V to 2.0 V, VDDP=VDDC=2.5 V		1		ns
Output Clock Fall Time	100 MHz	2.0 V to 0.8 V, VDDP=VDDC = 5 V		0.4		ns
	100 MHz	2.0 V to 0.8 V, VDDP=VDDC=3.3 V		0.6		ns
	100 MHz	2.0 V to 0.8 V, VDDP=VDDC=2.5 V		1		ns
Output Enable Time	100 MHz	OE high to output on 0 - 100 MHz		7	20	ns
Output Disable Time	100 MHz	OE low to tri-state 0 - 100 MHz		7	20	ns
Propagation Delay		VDDP = 5 V, VDDC = 5 V,		4	6	ns
	100 MHz	VDDP = 5 V, VDDC = 3.3 V		4.5	7	ns
	100 MHz	VDDP = 5 V, VDDC = 2.5 V		5.5	9	ns
	100 MHz	VDDP = 3.3 V, VDDC = 3.3 V		4.5	7	ns
		VDDP = 3.3 V, VDDC = 2.5 V		5.5	9	ns
Output Clock Duty Cycle 0 - 100 MHz		Any VDD combination	45		55	%

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Output Clock Duty		VDDP = 5 V, VDDC = 5 V	45		55	%
Cycle 100 - 166 MHz		VDDP = 5 V, VDDC = 3.3 V	45		55	%
		VDDP = 5 V, VDDC = 2.5 V	40		60	%
		VDDP = 3.3 V, VDDC = 3.3 V	40		60	%
		VDDP = 3.3 V, VDDC = 2.5 V	45		55	%
Output Clock Duty		VDDP = 5 V, VDDC = 5 V	40		60	%
Cycle 166 - 250 MHz		VDDP = 5 V, VDDC = 3.3 V	40		60	%
100 - 250 MITZ		VDDP = 5 V, VDDC = 2.5 V	35		65	%
		VDDP = 3.3 V, VDDC = 3.3 V	35		65	%
		VDDP = 3.3 V, VDDC = 2.5 V	40		60	%

# **Thermal Characteristics**

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Thermal Resistance Junction to	$\theta_{JA}$	Still air		150		° C/W
Ambient	$\theta_{JA}$	1 m/s air flow		140		° C/W
	$\theta_{JA}$	3 m/s air flow		120		° C/W
Thermal Resistance Junction to Case	θ <sub>JC</sub>			40		° C/W

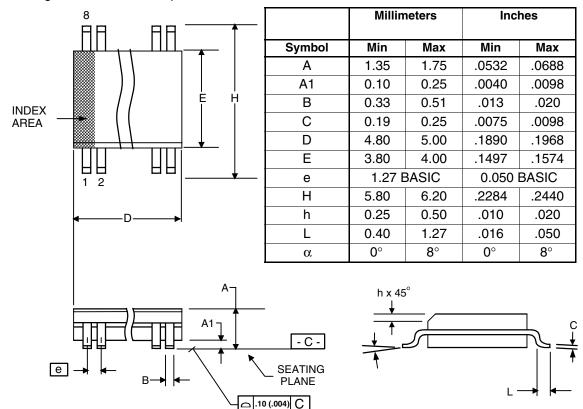
# **Marking Diagrams**



#### Notes:

- 1. ###### is the lot number
- 2. YYWW is the last two digits of the year and the week number that the part was assembled.
- 3. "I" denotes industrial temperature range.
- 4. "LF" denotes Pb-free.
- 5. Bottom marking: country of origin if not USA.

# Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)



Package dimensions are kept current with JEDEC Publication No. 95

### \*Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
508MLF		Tubes	8 pin SOIC	0 to +70° C
508MLFT	see page 6	Tape and Reel	8 pin SOIC	0 to +70° C
508MILF		Tubes	8 pin SOIC	-40 to +85° C
508MILFT		Tape and Reel	8 pin SOIC	-40 to +85° C
508-DWF	-	Die on uncut, probed wafers		0 to +70° C
508-DPK	-	Tested die in w	0 to +70° C	

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

# Innovate with IDT and accelerate your future networks. Contact:

# www.IDT.com

#### **For Sales**

800-345-7015 408-284-8200 Fax: 408-284-2775

#### For Tech Support www.idt.com/go/clockhelp

#### **Corporate Headquarters** Integrated Device Technology, Inc.

www.idt.com



© 2006 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. IDT and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners. Printed in USA