

## Improved Quad CMOS Analog Switches

### DESCRIPTION

The DG201B, DG202B analog switches are highly improved versions of the industry-standard DG201A, DG202. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG201B and DG202B can handle up to  $\pm 22$  V input signals, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (see Truth Table.)

### FEATURES

- $\pm 22$  V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance -  $R_{DS(on)}$ : 45  $\Omega$
- Low leakage -  $I_{D(on)}$ : 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching -  $t_{ON}$ : 120 ns
- Low glitching - Q: 1 pC
- **Compliant to RoHS Directive 2002/95/EC**



**RoHS\***  
COMPLIANT

### BENEFITS

- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Superior to DG201A, DG202
- Space savings (TSSOP)

### APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Disk drives
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### TRUTH TABLE

Logic	DG201B	DG202B
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.4$  V

\* Pb containing terminations are not RoHS compliant, exemptions may apply



ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 55 °C to 125 °C	16-pin CerDIP	DG201BAK
		DG202BAK
- 40 °C to 85 °C	16-pin Plastic DIP	DG201BDJ DG201BDJ-E3
		DG202BDJ DG202BDJ-E3
	16-pin narrow SOIC	DG201BDY DG201BDY-E3 DG201BDY-T1 DG201BDY-T1-E3
		DG202BDY DG202BDY-E3 DG202BDY-T1 DG202BDY-T1-E3
	16-pin TSSOP	DG201BDQ DG201BDQ-E3 DG201BDQ-T1 DG201BDQ-T1-E3
		DG202BDQ DG202BDQ-E3 DG202BDQ-T1 DG202BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter	Limit	Unit	
Voltages Referenced, V+ to V-	44	V	
GND	25		
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first		
Current (Any terminal)	30	mA	
Peak Current S or D (Pulsed at 1 ms, 10 % duty cycle max.)	100		
Storage Temperature	(AK, DK suffix)	- 65 to 150	°C
	(DJ, DY, DQ suffix)	- 65 to 125	
Power Dissipation (Package) <sup>b</sup>	16-pin plastic DIP <sup>c</sup>	470	mW
	16-pin narrow SOIC and TSSOP <sup>d</sup>	640	
	16-pin CerDIP <sup>e</sup>	900	
	LCC-20 <sup>f</sup>	750	

Notes:

- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.
- e. Derate 12 mW/°C above 75 °C.
- f. Derate 10 mW/°C above 75 °C.

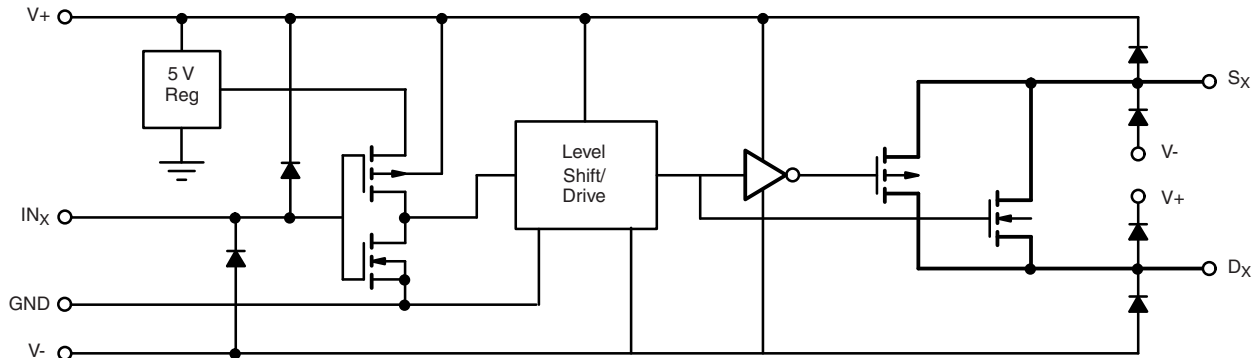
**SCHEMATIC DIAGRAM** (typical channel)


Figure 1.

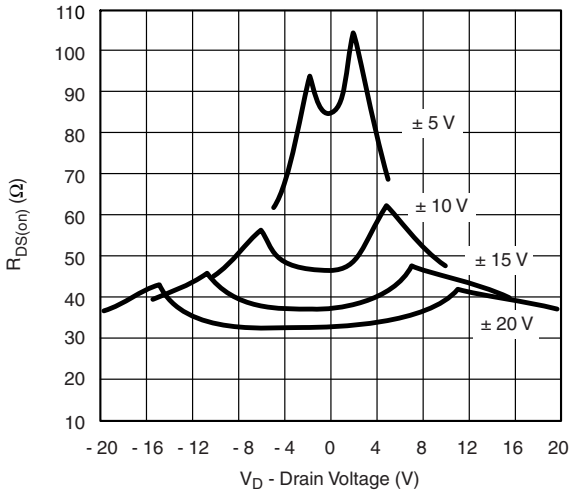
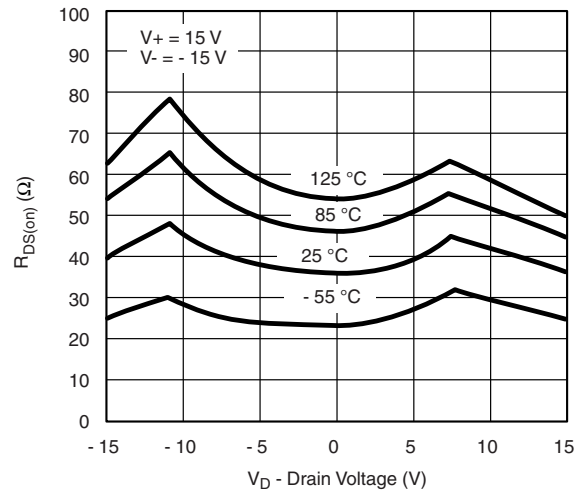
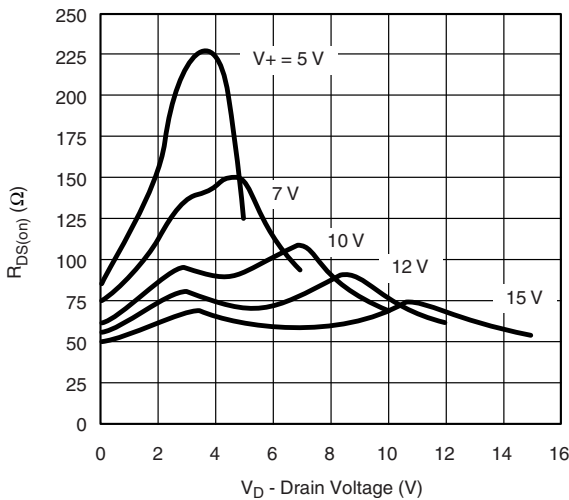
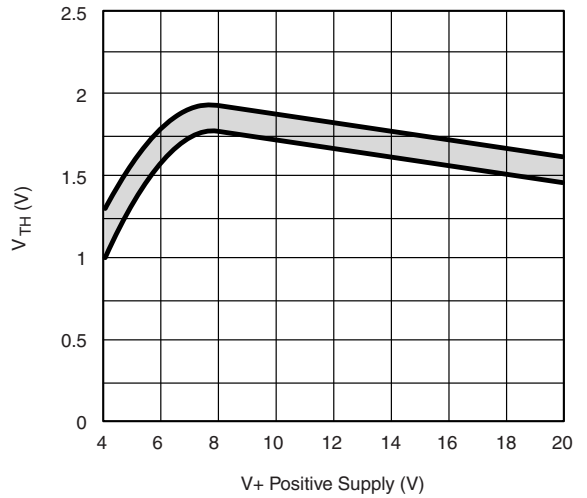
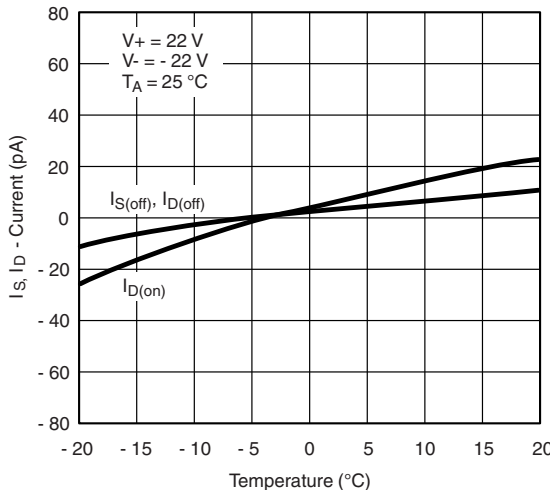
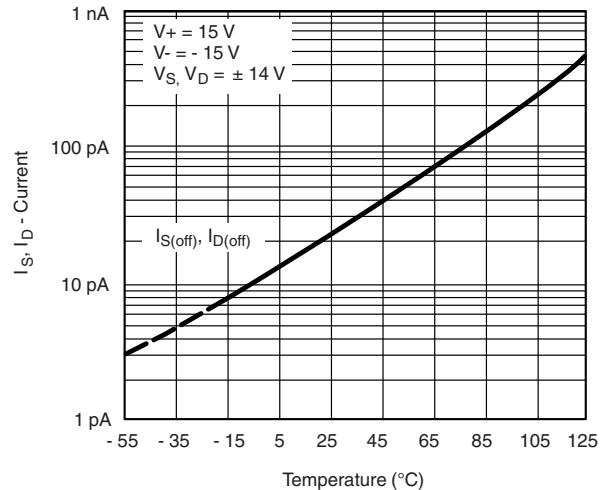
<b>SPECIFICATIONS<sup>a</sup></b>									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix -55 °C to 125 °C		D Suffix -40 °C to 85 °C		Unit
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$	Room	45		85		85	$\Omega$
$R_{DS(on)}$ Match	$\Delta R_{DS(on)}$		Room	2					
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}$ , $V_D = \pm 14\text{ V}$	Room	$\pm 0.01$	-0.5	0.5	-0.5	0.5	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 14\text{ V}$ , $V_S = \pm 14\text{ V}$	Room	$\pm 0.01$	-0.5	0.5	-0.5	0.5	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room	$\pm 0.02$	-0.5	0.5	-0.5	0.5	
<b>Digital Control</b>									
Input Voltage High	$V_{INH}$		Full		2.4		2.4		V
Input Voltage Low	$V_{INL}$		Full			0.8		0.8	
Input Current	$I_{INH}$ or $I_{INL}$	$V_{INH}$ or $V_{INL}$	Full		-1	1	-1	1	$\mu\text{A}$
Input Capacitance	$C_{IN}$		Room	5					pF
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$V_S = 2\text{ V}$ see switching time test circuit	Room	120		300		300	ns
Turn-Off Time	$t_{OFF}$		Room	65		200		200	
Charge Injection	Q	$C_L = 1000\text{ pF}$ , $V_g = 0\text{ V}$ $R_g = 0\ \Omega$	Room	1					pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)}$	$V_D = V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room	16					dB
Off Isolation	OIRR	$C_L = 15\text{ pF}$ , $R_L = 50\ \Omega$ $V_S = 1\text{ V}_{RMS}$ , $f = 100\text{ kHz}$	Room	90					
Channel-to-Channel Crosstalk	$X_{TALK}$		Room	95					
<b>Power Supply</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0$ or $5\text{ V}$	Room			50		50	$\mu\text{A}$
Negative Supply Current	$I_-$		Room			-1		-1	
Power Supply Range for Continuous Operation	$V_{OP}$		Full		$\pm 4.5$	$\pm 22$	$\pm 4.5$	$\pm 22$	V

<b>SPECIFICATIONS</b> (for Single Supply) <sup>a</sup>									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 12\text{ V}$ , $V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = 3\text{ V}$ , $8\text{ V}$ , $I_S = 1\text{ mA}$	Room Full	90		160 200		160 200	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$V_S = 8\text{ V}$ see switching time test circuit	Room	120		300		300	ns
Turn-Off Time	$t_{OFF}$		Room	60		200		200	
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_{gen} = 6\text{ V}$ $R_{gen} = 0\ \Omega$	Room	4					pC
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			50 100		50 100	$\mu\text{A}$
Negative Supply Current	I-		Room Full		- 1 - 5		- 1 - 5		
Power Supply Range for Continuous Operation	$V_{OP}$		Full		+ 4.5	+ 25	+ 4.5	+ 25	V

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

 **$R_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages**

 **$R_{DS(on)}$  vs.  $V_D$  and Temperature**

 **$R_{DS(on)}$  vs.  $V_D$  and Single Power Supply Voltages**

**Input Switching Threshold vs. Supply Voltage**

**Leakage Currents vs. Analog Voltage**

**Leakage Currents vs. Temperature**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Switching Time vs. Single Supply Voltage



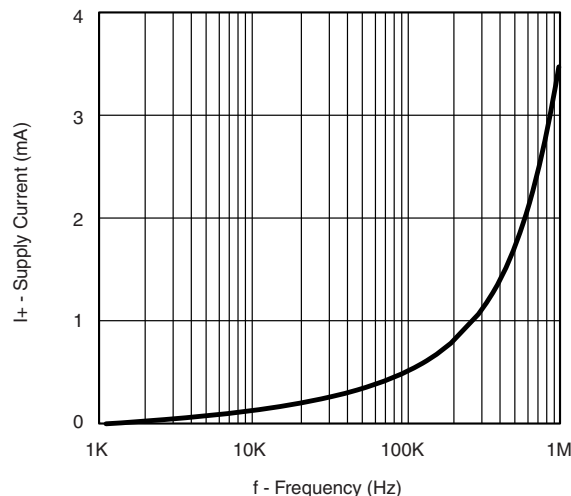
Switching Time vs. Power Supply Voltage



$Q_S, Q_D$  - Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency



Supply Current vs. Switching Frequency

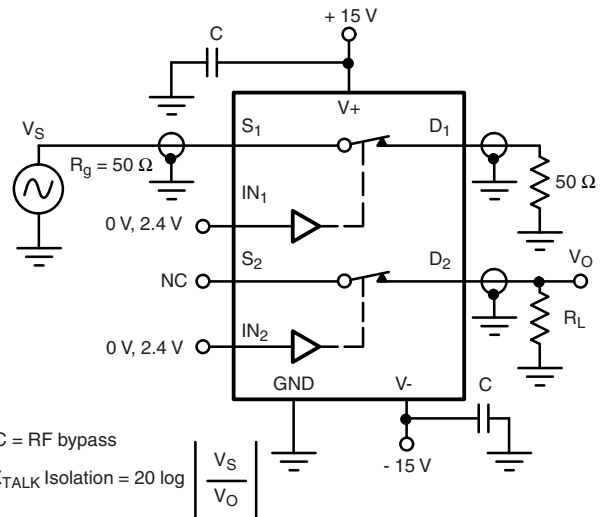
**TEST CIRCUITS**



**Figure 2. Switching Time**



**Figure 3. Off Isolation**



**Figure 4. Channel-to-Channel Crosstalk**



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

**Figure 5. Charge Injection**

## APPLICATIONS



Figure 6. Sample-and-Hold

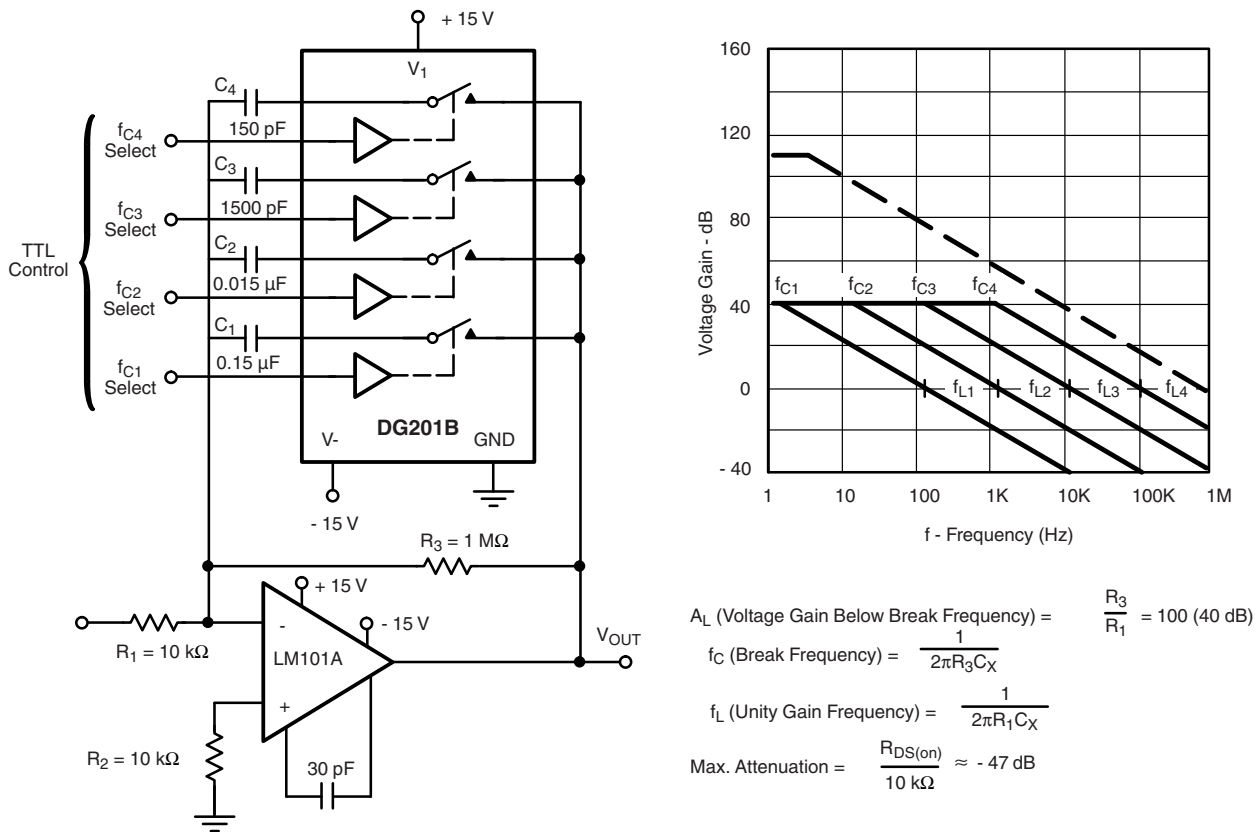
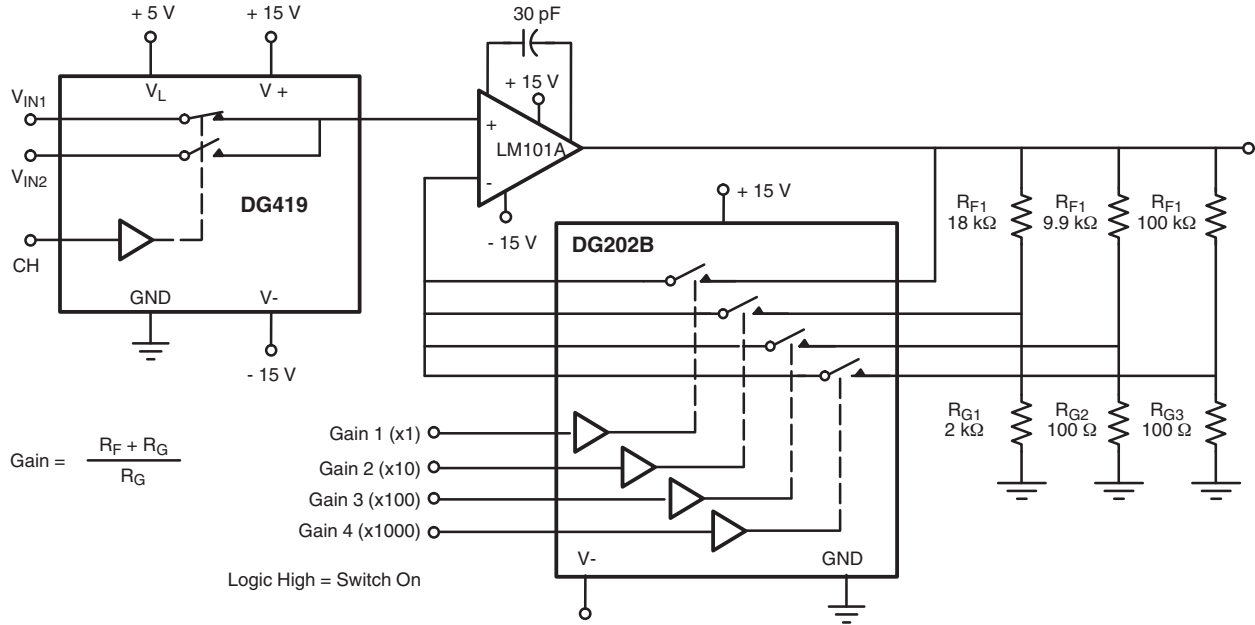


Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency



**APPLICATIONS**



**Figure 8. A Precision Amplifier with Digitally Programmable Input and Gains**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70037](http://www.vishay.com/ppg?70037).

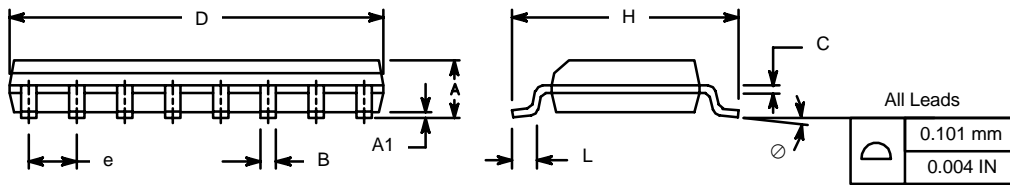


**SOIC (NARROW): 16-LEAD**  
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5300





**PDIP: 16-LEAD**



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482

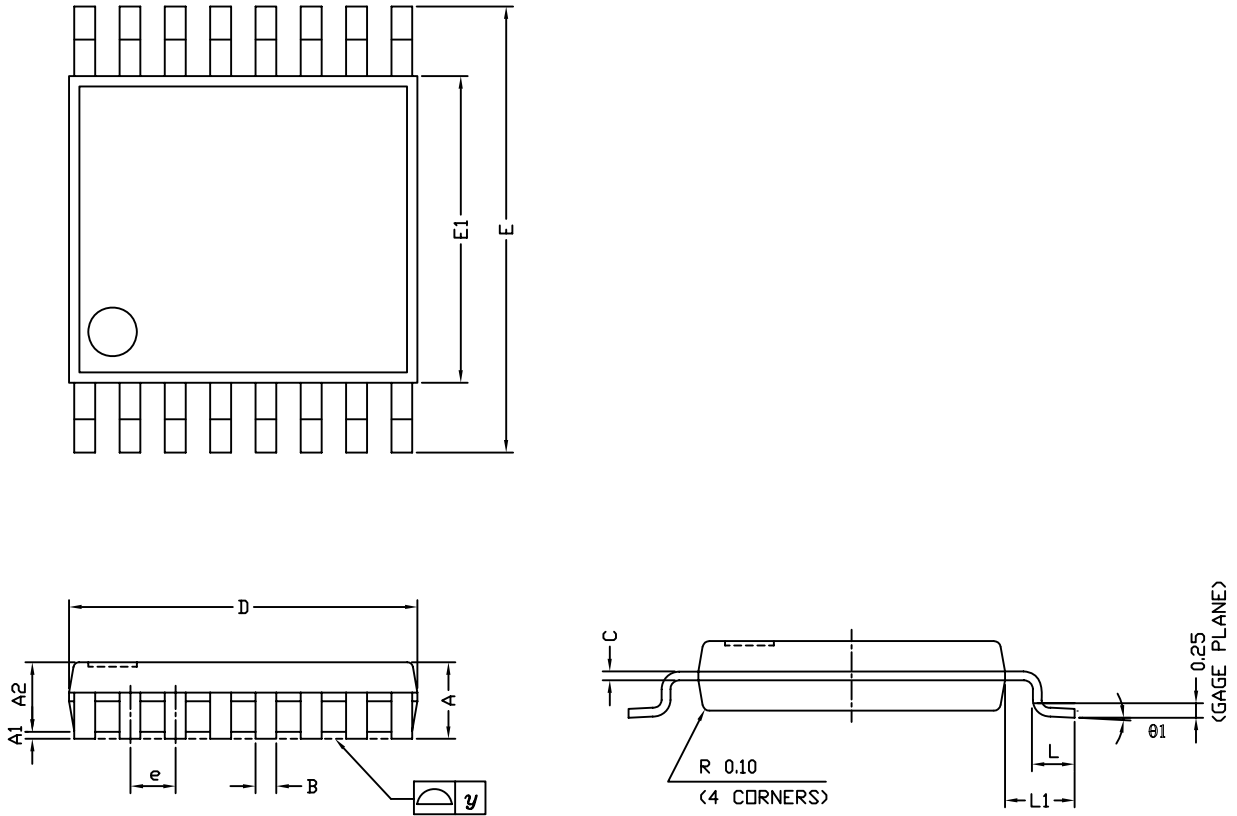
### CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	4.06	5.08	0.160	0.200
<b>A<sub>1</sub></b>	0.51	1.14	0.020	0.045
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	1.14	1.65	0.045	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	19.05	19.56	0.750	0.770
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	6.60	7.62	0.260	0.300
<b>e<sub>1</sub></b>	2.54 BSC		0.100 BSC	
<b>e<sub>A</sub></b>	7.62 BSC		0.300 BSC	
<b>L</b>	3.18	3.81	0.125	0.150
<b>L<sub>1</sub></b>	3.81	5.08	0.150	0.200
<b>Q<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>S</b>	0.38	1.14	0.015	0.045
$\infty$	0°	15°	0°	15°

ECN: S-03946—Rev. G, 09-Jul-01  
DWG: 5403

## TSSOP: 16-LEAD

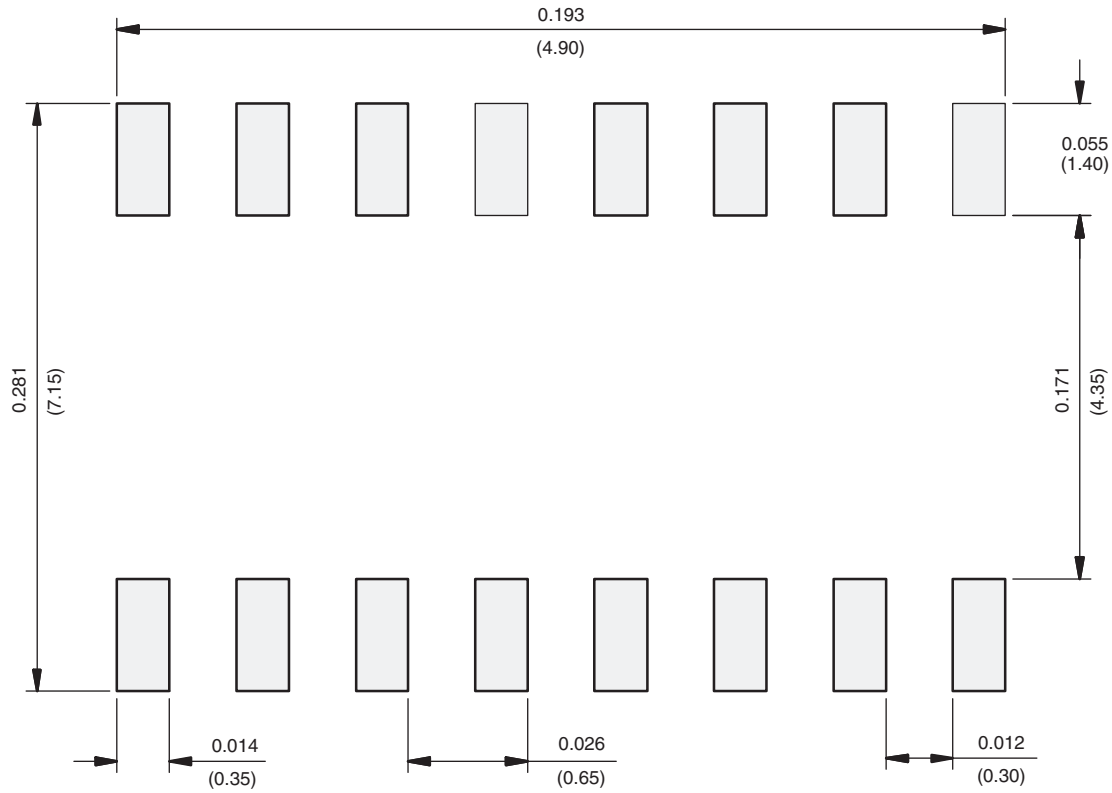


Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°

ECN: S-61920-Rev. D, 23-Oct-06  
DWG: 5624

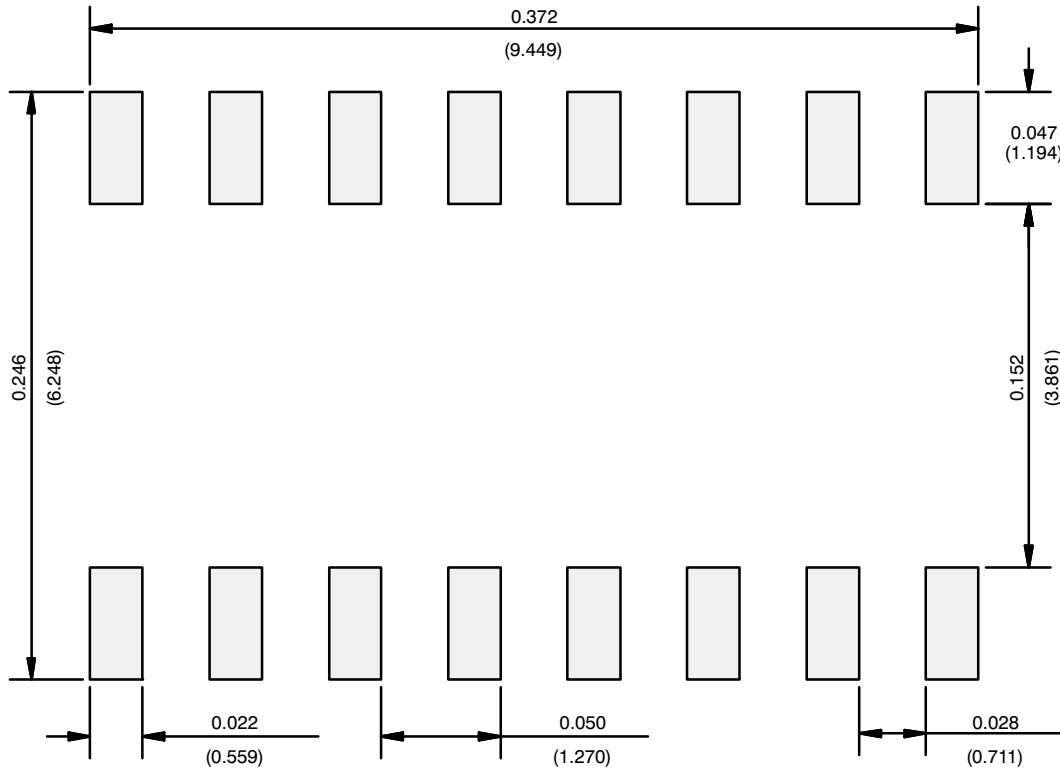


## RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads  
Dimensions in inches (mm)

## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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