Quad, 14-Bit, 125 MSPS Serial LVDS 1.8 V Analog-to-Digital Converter

Preliminary Technical Data

AD9253-EP

FEATURES

1.8 V supply operation
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
Qualification data available on request
Low power: 110 mW per channel at 125 MSPS
SNR = 74 dB (to Nyquist)
SFDR = 90 dBc (to Nyquist)
DNL = ±0.8 LSB (typical); INL = ±2.0 LSB (typical)
Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)
650 MHz full power analog bandwidth
2 V p-p input voltage range
Serial port control
- **Full chip and individual channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Multichip sync and clock divider**
- **Programmable output clock and data alignment**
- **Programmable output resolution**
- **Standby mode**

APPLICATIONS

Medical ultrasound
High speed imaging
Quadrature radio receivers
Diversity radio receivers
Test equipment

GENERAL DESCRIPTION

The AD9253-EP is a quad, 14-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip, sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled. The ADC contains several features

FUNCTIONAL BLOCK DIAGRAM

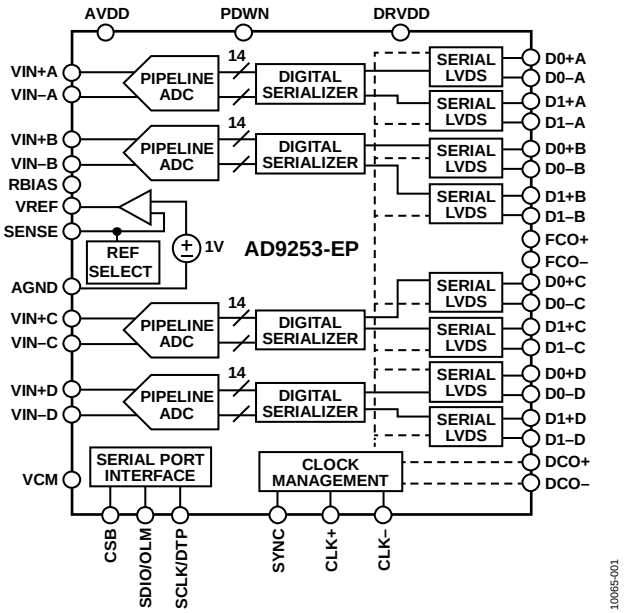

Figure 1.

designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9253-EP is available in a RoHS-compliant, 48-lead LFCSP and is specified over an extended temperature range of −55°C to +125°C. This product is protected by a U.S. patent. Additional application and technical information can be found in the AD9253 data sheet.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 110 mW/channel at 125 MSPS with scalable power options.
3. Ease of Use. A DCO operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
4. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. PrA
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REVISION HISTORY

10/12—PrA: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.8	−0.3	+0.1	% FSR
Offset Matching	Full	−0.6	+0.2	+0.6	% FSR
Gain Error	Full	−12	−3	+2	% FSR
Gain Matching	Full		1.1	1.6	% FSR
Differential Nonlinearity (DNL)	Full	−0.8		+1.9	LSB
	25°C		±0.8		LSB
Integral Nonlinearity (INL)	Full	−4.5		+4.5	LSB
	25°C		±2.0		LSB
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	Full		2		mV
Input Resistance	Full		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		0.94		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Differential Input Resistance			5.2		kΩ
Differential Input Capacitance	Full		3.5		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[2]	Full		183	205	mA
I_{DRVDD} (ANSI-644 Mode)[2]	Full		61	63	mA
I_{DRVDD} (Reduced Range Mode)[2]	25°C		53		mA
TOTAL POWER CONSUMPTION					
DC Input	Full		403		mW
Sine Wave Input (Four Channels Including Output Drivers ANSI-644 Mode)	Full		440	480	mW
Sine Wave Input (Four Channels Including Output Drivers Reduced Range Mode)	25°C		425		mW
Power-Down Mode	Full		2		mW
Standby Mode[3]	Full		235		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] It can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		75.3		dBFS
f_{IN} = 30.5 MHz	25°C		75.2		dBFS
f_{IN} = 70 MHz	Full	72	74.1		dBFS
f_{IN} = 140 MHz	25°C		72.2		dBFS
f_{IN} = 200 MHz	25°C		70.7		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		75.2		dBFS
f_{IN} = 30.5 MHz	25°C		75.1		dBFS
f_{IN} = 70 MHz	Full	71.7	74.0		dBFS
f_{IN} = 140 MHz	25°C		71.9		dBFS
f_{IN} = 200 MHz	25°C		70.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.2		Bits
f_{IN} = 30.5 MHz	25°C		12.2		Bits
f_{IN} = 70 MHz	Full		12.0		Bits
f_{IN} = 140 MHz	25°C		11.7		Bits
f_{IN} = 200 MHz	25°C		11.4		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		98		dBc
f_{IN} = 30.5 MHz	25°C		92		dBc
f_{IN} = 70 MHz	Full	76	90		dBc
f_{IN} = 140 MHz	25°C		85		dBc
f_{IN} = 200 MHz	25°C		83		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−98		dBc
f_{IN} = 30.5 MHz	25°C		−92		dBc
f_{IN} = 70 MHz	Full		−90	−76	dBc
f_{IN} = 140 MHz	25°C		−85		dBc
f_{IN} = 200 MHz	25°C		−83		dBc
WORST OTHER HARMONIC (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−101		dBFS
f_{IN} = 30.5 MHz	25°C		−100		dBFS
f_{IN} = 70 MHz	Full		−95	−83	dBFS
f_{IN} = 140 MHz	25°C		−96		dBFS
f_{IN} = 200 MHz	25°C		−92		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		86		dBc
CROSSTALK[2]	Full		−95		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−89		dB
POWER SUPPLY REJECTION RATIO (PSRR)[4]					
AVDD	25°C		48		dB
DRVDD	25°C		75		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with an −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] The overrange condition is specified with 3 dB of the full-scale input range.
[4] PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO/OLM)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO/OLM)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	290	345	400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0±x, D1±x), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	160	200	230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Temp	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	10		1000	MHz
Conversion Rate	Full	10		125	MSPS
Clock Pulse Width High (t_{EH})	Full		4.00		ns
Clock Pulse Width Low (t_{EL})	Full		4.00		ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})	Full		2.3		ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO-to-Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
DCO-to-FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Lane Delay (t_{LD})			90		ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)[5]	25°C		375		µs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1		ns
Aperture Uncertainty (Jitter, t_J)	25°C		135		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.
[4] t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. t_{SAMPLE} = 1/f_S.
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB to AGND	−0.3 V to +2.0 V
SYNC, PDWN to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−55°C to +125°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

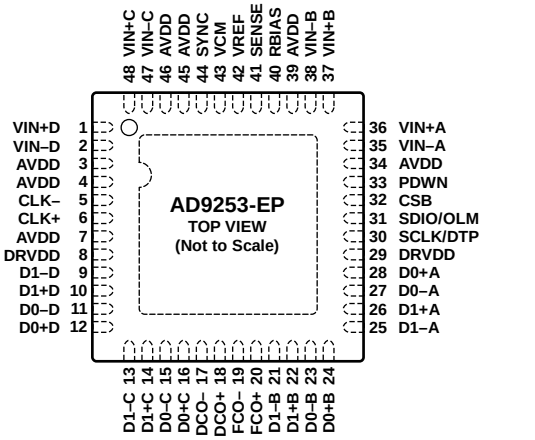
Package Type	Air Flow Velocity (m/sec)	θ_{JA}[1]	Ψ_{JT}	Ψ_{JB}	$\theta_{JC\ TOP}$	$\theta_{JC\ BOTTOM}$	Unit
48-Lead LFCSP	0.0	20.3	0.10	5.9	6.1	1.0	°C/W
	1.0	17.6	0.16	N/A[2]	N/A[2]	N/A[2]	°C/W
	2.5	16.5	0.20	N/A[2]	N/A[2]	N/A[2]	°C/W

[1] θ_{JA} for a 4-layer printed circuit board (PCB) with solid ground plane (simulated). Exposed pad soldered to PCB.
[2] N/A = not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 2. Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Analog Input True.
2	VIN−D	ADC D Analog Input Complement.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
5, 6	CLK−, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8, 29	DRVDD	Digital Output Driver Supply.
9	D1−D	Channel D Digital Output 1 Complement.
10	D1+D	Channel D Digital Output 1 True.
11	D0−D	Channel D Digital Output 0 Complement.
12	D0+D	Channel D Digital Output 0 True.
13	D1−C	Channel C Digital Output 1 Complement.
14	D1+C	Channel C Digital Output 1 True.
15	D0−C	Channel C Digital Output 0 Complement.
16	D0+C	Channel C Digital Output 0 True.
17	DCO−	Data Clock Output Complement.
18	DCO+	Data Clock Output True.
19	FCO−	Frame Clock Output Complement.
20	FCO+	Frame Clock Output True.
21	D1−B	Channel B Digital Output 1 Complement.
22	D1+B	Channel B Digital Output 1 True.
23	D0−B	Channel B Digital Output 0 Complement.
24	D0+B	Channel B Digital Output 0 True.
25	D1−A	Channel A Digital Output 1 Complement.
26	D1+A	Channel A Digital Output 1 True.
27	D0−A	Channel A Digital Output 0 Complement.
28	D0+A	Channel A Digital Output 0 True.

Pin No.	Mnemonic	Description
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation.
35	VIN−A	ADC A Analog Input Complement.
36	VIN+A	ADC A Analog Input True.
37	VIN+B	ADC B Analog Input True.
38	VIN−B	ADC B Analog Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.
43	VCM	Analog Input Common-Mode Voltage.
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN−C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

OUTLINE DIMENSIONS

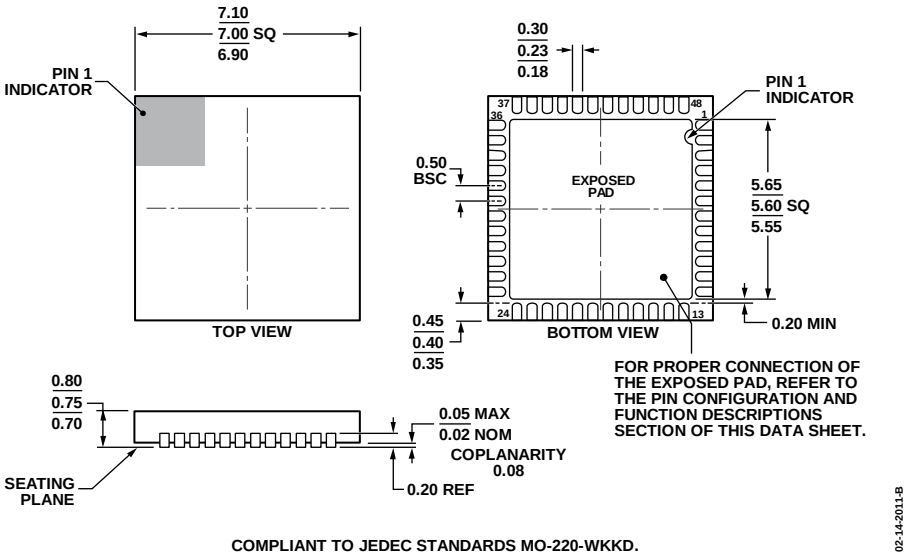


Figure 3. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9253-TCPZ-125EP	−55°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
AD9253-TCPZR7-125EP	−55°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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