4-Channel, 200 kSPS 12-Bit ADC with Sequencer in 16-Lead TSSOP

Enhanced Product

AD7923-EP

FEATURES

Fast throughput rate: 200 kSPS
Specified for AV_{DD} of 2.7 V to 5.25 V
Low power
3.6 mW max at 200 kSPS with 3 V supply
7.5 mW max at 200 kSPS with 5 V supply
4 (single-ended) inputs with sequencer
Wide input bandwidth
70 dB min SNR at 50 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface SPI®-/QSPI™-/
MICROWIRE™-/DSP-compatible
Shutdown mode: 0.5 µA max
16-lead TSSOP package
Support defense and aerospace applications (AQEC)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

GENERAL DESCRIPTION

The AD7923-EP is a 12-bit, high speed, low power, 4-channel, successive approximation (SAR) ADC. It operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 200 kSPS. It contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz.

The conversion process and data acquisition are controlled by $\overline{CS}$ and the serial clock, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$; the conversion is also initiated at this point.

The AD7923-EP uses advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, it consumes 1.2 mA maximum with 3 V supplies and 1.5 mA maximum with 5 V supplies.

Through the configuration of the control register, the analog input range can be selected as 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, with either straight binary or twos complement output coding. The AD7923-EP features four single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time for the AD7923-EP is determined by the serial clock, SCLK, frequency, since this is used as the master clock to control the conversion. The conversion time can be as short as 800 ns with a 20 MHz SCLK.

Additional application and technical information can be found in the AD7923 data sheet.

FUNCTIONAL BLOCK DIAGRAM

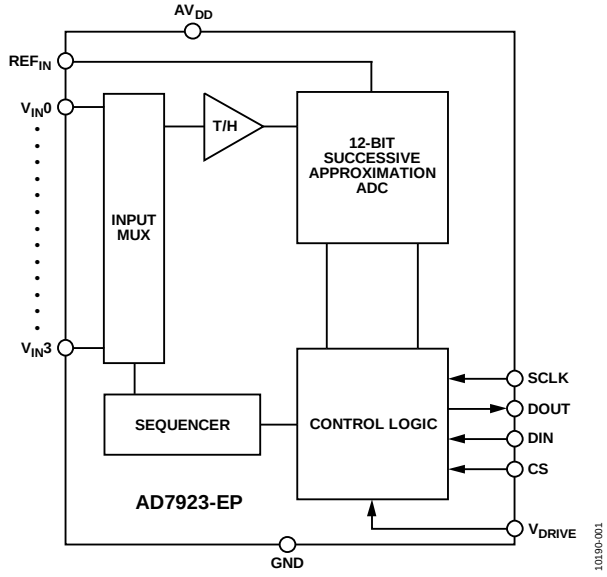

Figure 1.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption.
   The AD7923-EP offers up to 200 kSPS throughput rates. At the maximum throughput rate with 3 V supplies, the AD7923-EP dissipates just 3.6 mW of power.
2. Four Single-Ended Inputs with a Channel Sequencer.
3. Single-Supply Operation with V_{DRIVE} Function.
   The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of AV_{DD}.
4. Flexible Power/Serial Clock Speed Management.
   The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The part also features various shutdown modes to maximize power efficiency at lower throughput rates. Current consumption is 0.5 µA maximum when in full shutdown.
5. No Pipeline Delay.
   The part features a SAR ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range (EP version): −55°C to +125°C.

Table 1.

Parameter	EP Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)	70	dB min	@ 5 V, −40°C to +85°C
	69	dB min	@ 5 V, 85°C to 125°C, typ 70 dB
	69	dB min	@ 3 V typ 70 dB, −40°C to +125°C
Signal-to-Noise (SNR)	70	dB min	
Total Harmonic Distortion (THD)	−77	dB max	@ 5 V typ, −84 dB
	−73	dB max	@ 3 V typ,−77 dB
Peak Harmonic or Spurious Noise	−78	dB max	@ 5 V typ, −86 dB
(SFDR)	−76	dB max	@ 3 V typ, −80 dB
Intermodulation Distortion (IMD)			f_A = 40.1 kHz, f_B = 41.5 kHz
Second Order Terms	−90	dB typ	
Third Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±8	LSB max	Typ ±0.5 LSB
Offset Error Match	±0.5	LSB max	
Gain Error	±1.5	LSB max	
Gain Error Match	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±1.5	LSB max	
Positive Gain Error Match	±0.5	LSB max	
Zero-Code Error	±8	LSB max	Typ ±0.8 LSB
Zero-Code Error Match	±0.5	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	Range bit set to 1
	0 to 2 × REF_{IN}	V	Range bit set to 0, AV_{DD} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 200 kSPS

Parameter	EP Version[1]	Unit	Test Conditions/Comments
LOGIC INPUTS			
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$	V min	
Input Low Voltage, V_{INL}	$0.3 \times V_{DRIVE}$	V max	
Input Current, I_{IN}	±1	µA max	Typ 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[2]	1	pF max	
Output Coding	Twos Complement		Coding bit set to 0
	Straight (Natural) Binary		Coding bit set to 1
CONVERSION RATE			
Conversion Time			
Track-and-Hold Acquisition Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
	300	ns max	Sinewave input
	300	ns max	Full-scale step Input
Throughput Rate	200	kSPS max	
POWER REQUIREMENTS			
AV_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DRIVE}
During Conversion	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2.0	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational) f_{SAMPLE} = 200 kSPS	1.5	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	1.2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Using Auto Shutdown Mode f_{SAMPLE} = 200 kSPS	900	µA typ	AV_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 200 kSPS
	650	µA typ	AV_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 200 kSPS
Auto Shutdown (Static)	0.5	µA max	SCLK on or off (20 nA typ)
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation			
Normal Mode (Operational) f_{SAMPLE} = 200 kSPS	7.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	3.6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature range: EP Version: −55°C to +125°C.
[2] Sample tested @ 25°C to ensure compliance.

TIMING SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V, $V_{DRIVE} \leq AV_{DD}$, REF_{IN} = 2.5 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.[1]

Table 2.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**AV_{DD} = 3 V**	**AV_{DD} = 5 V**	**Unit**	**Description**
f_{SCLK}[2]	10	10	kHz min	
	20	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between $\overline{CS}$ rising edge and start of next conversion
t_2	10	10	ns min	$\overline{CS}$ to SCLK set-up time
t_3[3]	35	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4[3]	40	40	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	10	10	ns min	SCLK to DOUT valid hold time
t_8[4]	15/45	15/35	ns min/max	SCLK falling edge to DOUT high impedance
t_9	10	10	ns min	DIN set-up time prior to SCLK falling edge
t_{10}	5	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	20	ns min	Sixteenth SCLK falling edge to $\overline{CS}$ high
t_{12}	1	1	µs max	Power-Up time from full power-down/auto shutdown mode

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of AV_{DD}) and timed from a voltage level of 1.6 V. See Figure 2. The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.
[2] The mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 0.7 × V_{DRIVE}.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, quoted in the timing characteristics t_8, is the true bus relinquish time of the part and is independent of the bus loading.

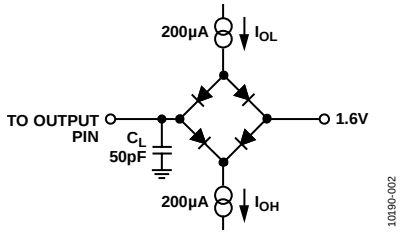


Figure 2. Load Circuit for Digital Output Timing Specification

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to AGND	−0.3 V to +7 V
Digital Output Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
REF_{IN} to AGND	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range(EP Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	150.4°C/W (TSSOP)
θ_{JC} Thermal Impedance	27.6°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Pb-free Temperature, Soldering	
Reflow	260(+0)°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latchup.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

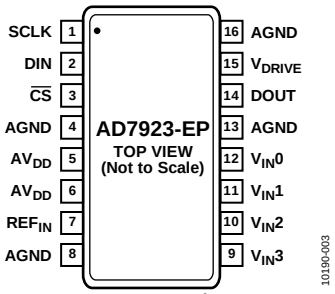


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input. SCLK provides the serial clock for accessing data for the part. This clock input is also used as the clock source for the AD7923-EP conversion process.
2	DIN	Data In. Logic Input. Data to be written to the control register is provided on this input and is clocked into the register on the falling edge of SCLK.
3	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7923-EP and framing the serial data transfer.
4, 8, 13, 16	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7923-EP. All analog input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
5, 6	AV_{DD}	Analog Power Supply Input. The AV_{DD} range for the AD7923-EP is from 2.7 V to 5.25 V. For the 0 V to 2 × REF_{IN} range, AV_{DD} should be from 4.75 V to 5.25 V.
7	REF_{IN}	Reference Input for the AD7923-EP. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
12 to 9	$V_{IN}0$ to $V_{IN}3$	Analog Input 0 through Analog Input 3. Four single-ended analog input channels that are multiplexed into the on-chip track-and-hold. The analog input channel to be converted is selected by using the Address Bits ADD1 and ADD0 of the control register. The address bits in conjunction with the SEQ1 and SEQ0 bits allow the sequencer to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or from 0 V to 2 × REF_{IN} as selected via the range bit in the control register. Any unused input channels must be connected to AGND to avoid noise pickup.
14	DOUT	Data Out. Logic Output. The conversion result from the AD7923-EP is provided on this output pin as a serial data stream. The AD7923-EP serial data stream consists of two leading 0s, and two address bits indicating which channel the conversion result corresponds to, followed by 12 bits of conversion data, MSB first. The output coding can be selected as straight binary or twos complement via the coding bit in the control register. The data bits are clocked out of the AD7923-EP on the SCLK falling edge.
15	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at which voltage the serial interface operates.

TYPICAL PERFORMANCE CHARACTERISTICS

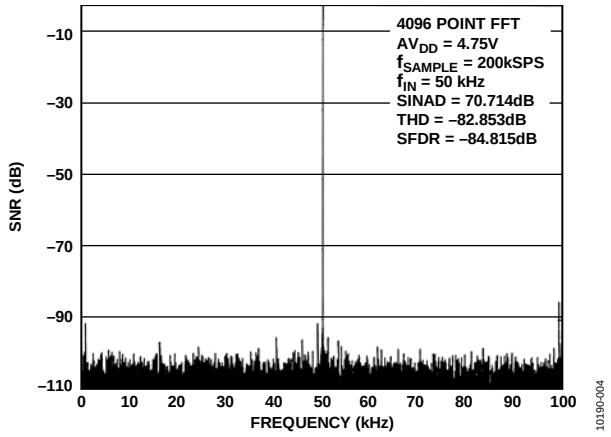


Figure 4. Dynamic Performance at 200 kSPS

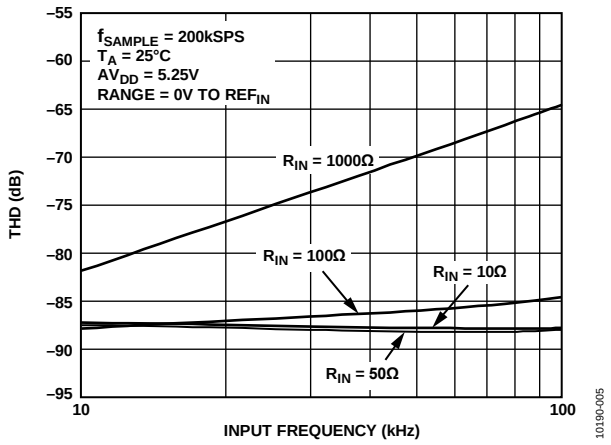


Figure 5. THD vs. Analog Input Frequency for Various Source Impedances

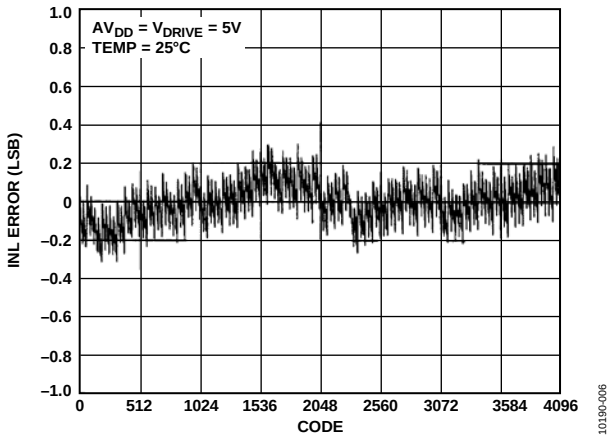


Figure 6. Typical INL

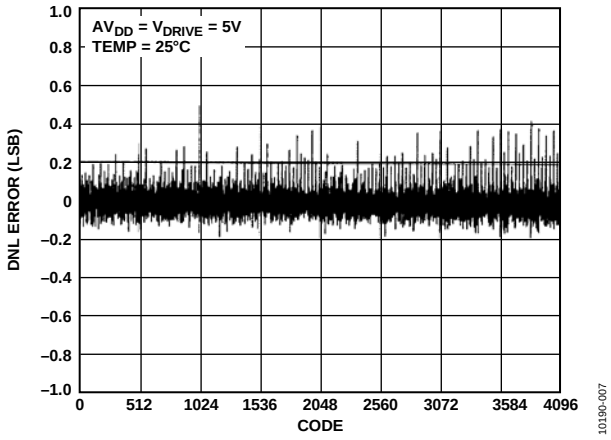
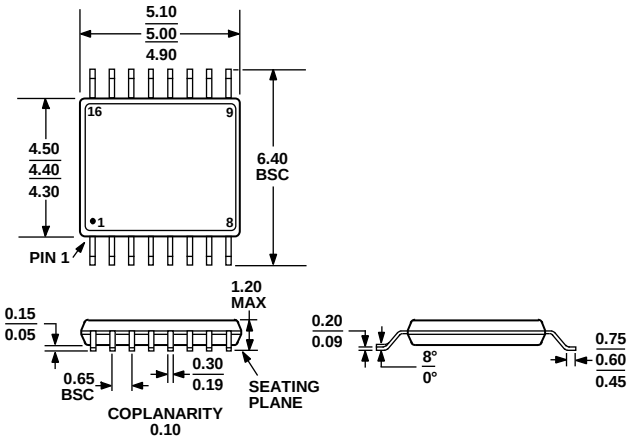


Figure 7. Typical DNL

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 8. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option
AD7923SRU-EP	−55°C to +125°C	±1	16-Lead TSSOP	RU-16
AD7923SRU-EP-RL7	−55°C to +125°C	±1	16-Lead TSSOP	RU-16

[1] Linearity error refers to integral linearity error.

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