Low Cost, 4-Channel, 16-Bit 1 MSPS PulSAR ADC

AD7655-EP

FEATURES

4-channel, 16-bit resolution ADC
2 track-and-hold amplifiers
Throughput
- **1 MSPS (normal mode)**
- **888 kSPS (impulse mode)**

Analog input voltage range: 0 V to 5 V
No pipeline delay
Parallel and serial 5 V/3 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
Single 5 V supply operation
Power dissipation
- **120 mW typical**
- **2.6 mW @ 10 kSPS**

48-lead frame chip scale package (LFCSP)
Pin-to-pin compatible with the AD7654
Low cost
Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
Enhanced product change notification
Qualification data available on request

APPLICATIONS

AC motor control
- **3-phase power control**
- **4-channel data acquisition**
- **Uninterrupted power supplies**
- **Communications**

GENERAL DESCRIPTION

The AD7655-EP is a low cost, simultaneous sampling, dual-channel, 16-bit, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. It contains two low noise, wide bandwidth, track-and-hold amplifiers that allow simultaneous sampling, a high speed 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. Each track-and-hold has a multiplexer in front to provide a 4-channel input ADC. The A0 multiplexer control input allows the choice of simultaneously sampling input pairs INA1/INB1 (A0 = low) or INA2/ INB2 (A0 = high). The part features a very high sampling rate mode (normal) and, for low power applications, a reduced power mode (impulse) where the power is scaled with the throughput. Operation is specified from −55°C to +125°C.

Full details about this enhanced product are available in the AD7655 data sheet, which should be consulted in conjunction with this data sheet.

FUNCTIONAL BLOCK DIAGRAM

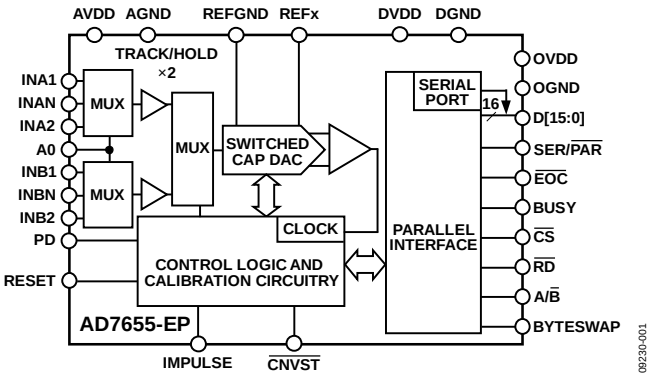

Figure 1.

Table 1. PulSAR® Selection

Type/kSPS	100 to 250	500 to 570	800 to 1000	>1000
Pseudo Differential	AD7660/ AD7661	AD7650/ AD7652 AD7664/ AD7666	AD7653 AD7667	
True Bipolar	AD7663	AD7665	AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621 AD7623
18 Bit	AD7678	AD7679	AD7674	AD7641
Multichannel/ Simultaneous		AD7654	AD7655	

PRODUCT HIGHLIGHTS

1. Multichannel ADC.
   The AD7655-EP features 4-channel inputs with two sample-and-hold circuits that allow simultaneous sampling.
2. Fast Throughput.
   The AD7655-EP is a 1 MSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
3. Single-Supply Operation.
   The AD7655-EP operates from a single 5 V supply. In impulse mode, its power dissipation decreases with throughput.
4. Serial or Parallel Interface.
   Versatile parallel or 2-wire serial interface arrangements are compatible with both 3 V and 5 V logic.

Rev. A

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REVISION HISTORY

2/11—Rev. 0 to Rev. A

Removed LQFP from Features Section 1
Removed Internal Power Dissipation (700 mW) from Table 5 .. 7

7/10—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{INx} - V_{INxN}$	0		2 V_{REF}	V
Common-Mode Input Voltage	V_{INxN}	−0.1		+0.5	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	1 MSPS throughput		45		µA
Input Impedance					
THROUGHPUT SPEED					
Complete Cycle (2 Channels)	Normal mode			2	µs
Throughput Rate	Normal mode	0		1	MSPS
Complete Cycle (2 Channels)	Impulse mode			2.25	µs
Throughput Rate	Impulse mode	0		888	kSPS
DC ACCURACY					
Integral Linearity Error[1]		−6		+6	LSB[2]
No Missing Codes		15			Bits
Transition Noise			0.8		LSB
Full-Scale Error	T_{MIN} to T_{MAX}		±0.25	±0.5	% of FSR
Full-Scale Error Drift			±2		ppm/°C
Unipolar Zero Error	T_{MIN} to T_{MAX}			±0.25	% of FSR
Unipolar Zero Error Drift			±0.8		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.8		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		86		dB[3]
Spurious-Free Dynamic Range	f_{IN} = 100 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 100 kHz		−96		dB
Signal-to-Noise and Distortion	f_{IN} = 100 kHz		86		dB
	f_{IN} = 100 kHz, −60 dB input		30		dB
Channel-to-Channel Isolation	f_{IN} = 100 kHz		−92		dB
−3 dB Input Bandwidth			10		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Delay Matching			30		ps
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD/2	V
External Reference Current Drain	1 MSPS throughput		180		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.8	V
V_{IH}		+2.0		DVDD + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[4]					
Pipeline Delay[5]					
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.2			V

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[6]	V
Operating Current[7]	1 MSPS throughput				
AVDD			15.5		mA
DVDD			8.5		mA
OVDD			100		µA
Power Dissipation	1 MSPS throughput[7]		120	135	mW
	20 kSPS throughput[8]		2.6		mW
	888 kSPS throughput[8]		114	125	mW
TEMPERATURE RANGE[9]					
Specified Performance	T_{MIN} to T_{MAX}	−55		+125	°C

[1] Linearity is tested using endpoints, not best fit.
[2] LSB means least significant bit. With the 0 V to 5 V input range, 1 LSB is 76.294 µV.
[3] All specifications in dB are referred to as full-scale input, FS. Tested with an input signal at 0.5 dB below full scale unless otherwise specified.
[4] Parallel or serial 16 bit.
[5] Conversion results are available immediately after completed conversion.
[6] The maximum should be the minimum of 5.25 V and DVDD + 0.3 V.
[7] In normal mode; tested in parallel reading mode.
[8] In impulse mode; tested in parallel reading mode.
[9] Consult sales for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND RESET					
Convert Pulse Width	t_1	5			ns
Time Between Conversions					
(Normal Mode/Impulse Mode)	t_2	2/2.25			µs
$\overline{CNVST}$ Low to BUSY High Delay	t_3			32	ns
BUSY High All Modes Except in Master Serial Read After Convert Mode					
(Normal Mode/Impulse Mode)	t_4			1.75/2	µs
Aperture Delay	t_5		2		ns
End of Conversions to BUSY Low Delay	t_6	10			ns
Conversion Time					
(Normal Mode/Impulse Mode)	t_7			1.75/2	µs
Acquisition Time	t_8	250			ns
RESET Pulse Width	t_9	10			ns
$\overline{CNVST}$ Low to $\overline{EOC}$ High Delay	t_{10}			30	ns
$\overline{EOC}$ High for Channel A Conversion					
(Normal Mode/Impulse Mode)	t_{11}			1/1.25	µs
$\overline{EOC}$ Low after Channel A Conversion	t_{12}	45			ns
$\overline{EOC}$ High for Channel B Conversion	t_{13}			0.75	µs
Channel Selection Setup Time	t_{14}	250			ns
Channel Selection Hold Time	t_{15}			30	ns
PARALLEL INTERFACE MODES					
$\overline{CNVST}$ Low to DATA Valid Delay	t_{16}			1.75/2	µs
DATA Valid to BUSY Low Delay	t_{17}	14			ns
Bus Access Request to DATA Valid	t_{18}			40	ns
Bus Relinquish Time	t_{19}	5		15	ns
A/$\overline{B}$ Low to Data Valid Delay	t_{20}			40	ns
MASTER SERIAL INTERFACE MODES					
$\overline{CS}$ Low to SYNC Valid Delay	t_{21}			10	ns
$\overline{CS}$ Low to Internal SCLK Valid Delay[1]	t_{22}			10	ns
$\overline{CS}$ Low to SDOUT Delay	t_{23}			10	ns
$\overline{CNVST}$ Low to SYNC Delay, Read During Convert					
(Normal Mode/Impulse Mode)	t_{24}		250/500		ns
SYNC Asserted to SCLK First Edge Delay	t_{25}	3			ns
Internal SCK Period[2]	t_{26}	23		40	ns
Internal SCLK High[2]	t_{27}	12			ns
Internal SCLK Low[2]	t_{28}	7			ns
SDOUT Valid Setup Time[2]	t_{29}	4			ns
SDOUT Valid Hold Time[2]	t_{30}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{31}	1			ns
$\overline{CS}$ High to SYNC High-Z	t_{32}			10	ns
$\overline{CS}$ High to Internal SCLK High-Z	t_{33}			10	ns
$\overline{CS}$ High to SDOUT High-Z	t_{34}			10	ns
BUSY High in Master Serial Read after Convert[2]	t_{35}		See Table 4		
$\overline{CNVST}$ Low to SYNC Asserted Delay					
(Normal Mode/Impulse Mode)	t_{36}		0.75/1		µs
SYNC Deasserted to BUSY Low Delay	t_{37}		25		ns

Parameter	Symbol	Min	Typ	Max	Unit
SLAVE SERIAL INTERFACE MODES					
External SCLK Setup Time	t_{38}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{39}	3		18	ns
SDIN Setup Time	t_{40}	5			ns
SDIN Hold Time	t_{41}	5			ns
External SCLK Period	t_{42}	25			ns
External SCLK High	t_{43}	10			ns
External SCLK Low	t_{44}	10			ns

[1] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise C_L is 60 pF maximum.
[2] In serial master read during convert mode. See Table 4 for serial master read after convert mode.

Table 4. Serial Clock Timings in Master Read After Convert

DIVSCLK[1]		**0**	**0**	**1**	**1**	
DIVSCLK[0]	**Symbol**	**0**	**1**	**0**	**1**	**Unit**
SYNC to SCLK First Edge Delay Minimum	t_{25}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{26}	25	50	100	200	ns
Internal SCLK Period Typical	t_{26}	40	70	140	280	ns
Internal SCLK High Minimum	t_{27}	12	22	50	100	ns
Internal SCLK Low Minimum	t_{28}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{29}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{30}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{31}	1	3	30	80	ns
Busy High Width Maximum (Normal)	t_{35}	3.25	4.25	6.25	10.75	µs
Busy High Width Maximum (Impulse)	t_{35}	3.5	4.5	6.5	11	µs

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Values
Analog Input	
INAx, INBx, REFx, INxN, REFGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	–0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	–0.3 V to +7 V
Digital Inputs	–0.3 V to DVDD + 0.3 V
Internal Power Dissipation[1]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Specification is for device in free air: 48-lead LFCSP, θ_{JA} = 26°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

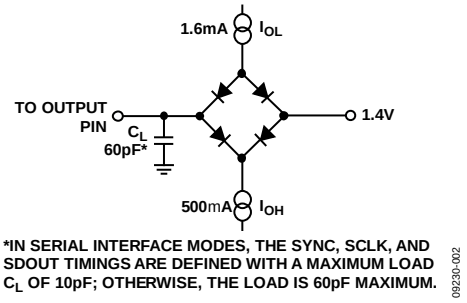


Figure 2. Load Circuit for Digital Interface Timing

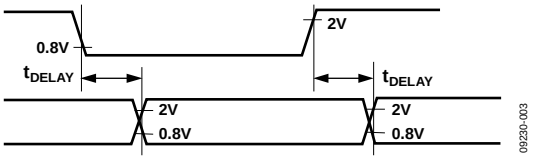
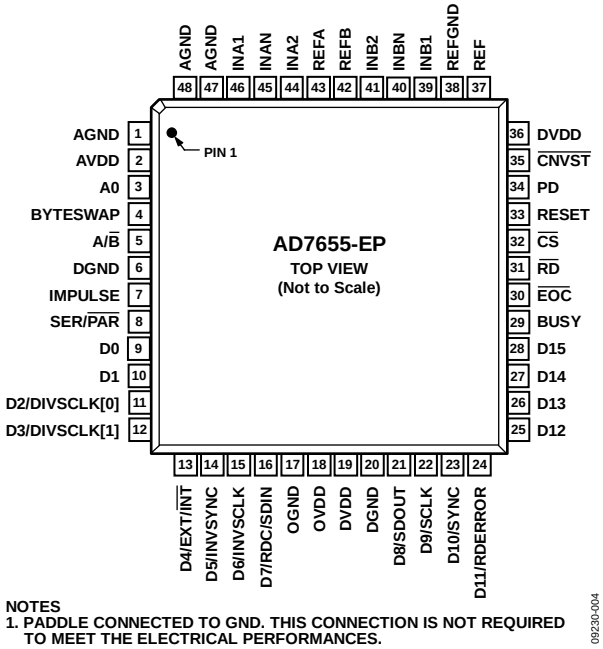


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PADDLE CONNECTED TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES.

Figure 4. 48-Lead LFCSP (CP-48-1)

Table 6. Pin Function Descriptions

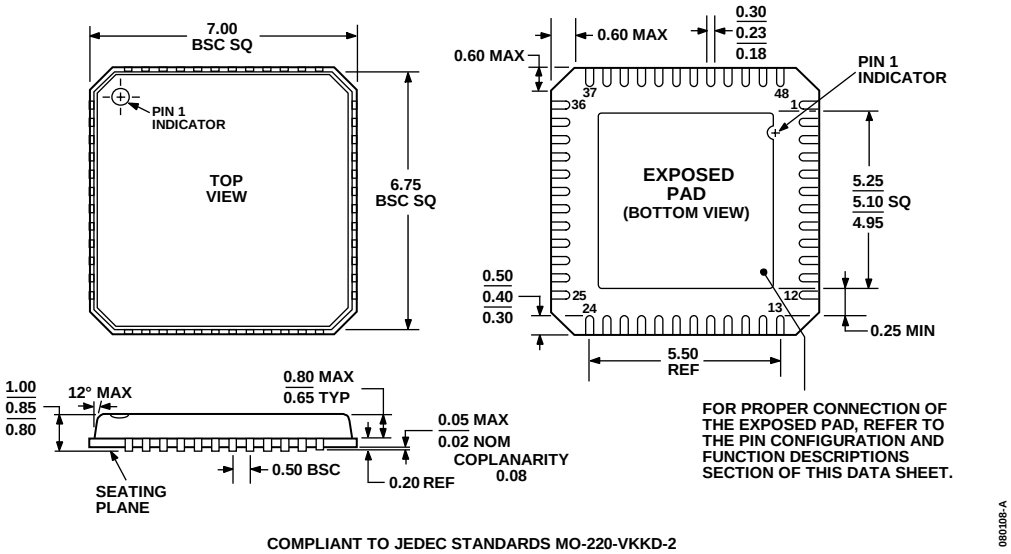
Pin No.	Mnemonic	Type[1]	Description
1, 47, 48	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3	A0	DI	Multiplexer Select. When LOW, the analog inputs INA1 and INB1 are sampled simultaneously, then converted. When HIGH, the analog inputs INA2 and INB2 are sampled simultaneously, then converted.
4	BYTESWAP	DI	Parallel Mode Selection (8 Bit, 16 Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	A/$\overline{B}$	DI	Data Channel Selection. In parallel mode, when LOW, the data from Channel B is read. When HIGH, the data from Channel A is read. In serial mode, when HIGH, Channel A is output first followed by Channel B. When LOW, Channel B is output first followed by Channel A.
6, 20	DGND	P	Digital Power Ground.
7	IMPULSE	DI	Mode Selection. When HIGH, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which is the serial master read after convert mode. These inputs, part of the serial port, are used to slow down the internal serial clock that clocks the data output. In the other serial modes, these inputs are not used.
13	D[4] or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock called, respectively, master and slave mode. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D[5] or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal in Master modes. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.

Pin No.	Mnemonic	Type[1]	Description
15	D[6]	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 6 of the parallel port data output bus.
	or INVSCLK		When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave modes.
16	D[7]	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus.
	or RDC/SDIN		When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input, depending on the state of EXT/$\overline{\text{INT}}$.
			When EXT/$\overline{\text{INT}}$ is HIGH, RDC/SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 32 SCLK periods after the initiation of the read sequence.
			When EXT/$\overline{\text{INT}}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19, 36	DVDD	P	Digital Power. Nominally at 5 V.
21	D[8]	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus.
	or SDOUT		When SER/$\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in a 32-bit on-chip register. The AD7655-EP provides the two conversion results, MSB first, from its internal shift register. The order of channel outputs is controlled by A/$\overline{\text{B}}$. In serial mode, when EXT/$\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK.
			In serial mode, when EXT/$\overline{\text{INT}}$ is HIGH:
			If INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and valid on the next falling edge.
			If INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and valid on the next rising edge.
22	D[9]	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus.
	or SCLK		When SER/$\overline{\text{PAR}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, depends upon the logic state of the EXT/$\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin.
23	D[10]	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus.
	or SYNC		When SER/$\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{\text{INT}}$ = Logic LOW).
			When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and frames SDOUT. After the first channel is output, SYNC is pulsed LOW. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid. After the first channel is output, SYNC is pulsed HIGH.
24	D[11]	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus.
	or RDERROR		When SER/$\overline{\text{PAR}}$ is HIGH and EXT/$\overline{\text{INT}}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started but not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25 to 28	D[12:15]	DO	Bit 12 to Bit 15 of the parallel port data output bus. When SER/$\overline{\text{PAR}}$ is HIGH, these outputs are in high impedance.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the two conversions are complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal.
30	$\overline{\text{EOC}}$	DO	End of Convert Output. Goes LOW at each channel conversion.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7655-EP. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current conversion is completed.

Pin No.	Mnemonic	Type[1]	Description
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample-and-hold into the hold state and initiates a conversion. In impulse mode (IMPULSE = HIGH), if $\overline{\text{CNVST}}$ is held LOW when the acquisition phase (t_8) is complete, the internal sample-and-hold is put into the hold state and a conversion is immediately started.
37	REF	AI	This input pin is used to provide a reference to the converter.
38	REFGND	AI	Reference Input Analog Ground.
39, 41	INB1, INB2	AI	Channel B Analog Inputs.
40, 45	INBN, INAN	AI	Analog Inputs Ground Senses. Allow to sense each channel ground independently.
42, 43	REFB, REFA	AI	These inputs are the references applied to Channel A and Channel B, respectively.
44, 46	INA2, INA1	AI	Channel A Analog Inputs.

[1] AI = input; DI = digital input; DO = digital output; DI/O = bidirectional digital; P = power.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 5. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7655SCP-EP-RL	−55°C to +125°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-1

NOTES