1 ppm, 20-Bit, ±1 LSB INL, Voltage Output DAC

Enhanced Product

AD5791-EP

FEATURES

- **1 ppm resolution**
- **1 ppm INL**
- **7.5 nV/√Hz noise spectral density**
- **0.19 LSB long-term linearity stability**
- **<0.05 ppm/°C temperature drift**
- **1 µs settling time**
- **1.4 nV-sec glitch impulse**
- **20-lead TSSOP package**
- **Wide power supply range up to ±16.5 V**
- **35 MHz Schmitt triggered digital interface**
- **1.8 V compatible digital interface**
- **Extended automotive operating temperature range: −55°C to +125°C**

ENHANCED PRODUCT FEATURES

- **Supports defense and aerospace applications (AQEC standard)**
- **Military temperature range (−55°C to +125°C)**
- **Controlled manufacturing baseline**
- **One assembly/test site**
- **One fabrication site**
- **Enhanced product change notification**
- **Qualification data available on request**

APPLICATIONS

- **Medical instrumentation**
- **Test and measurement**
- **Industrial control**
- **High end scientific and aerospace instrumentation**

FUNCTIONAL BLOCK DIAGRAM

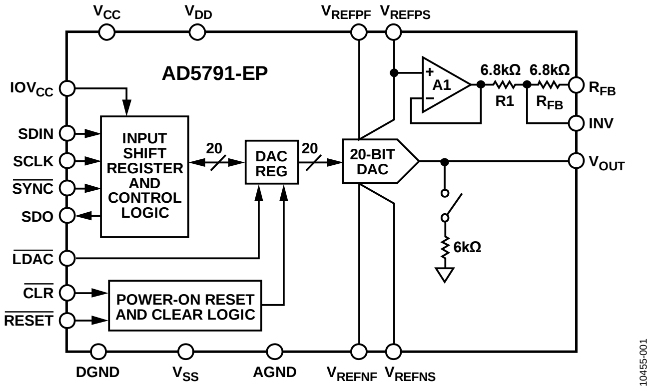

Figure 1.

COMPANION PRODUCTS

Ultra precision op amps: AD8675, AD8676
High voltage op amp: ADA4898-1
Additional companion products on the AD5791 product page

Table 1. Related Device

Part No.	Description
AD5781	18-bit, 0.5 LSB INL, voltage output DAC

GENERAL DESCRIPTION

The AD5791-EP[1] is a single 20-bit, unbuffered voltage-output DAC that operates from a bipolar supply of up to 33 V. The AD5791 accepts a positive reference input in the range 5 V to V_{DD} − 2.5 V and a negative reference input in the range V_{SS} + 2.5 V to 0 V. The AD5791-EP offers a relative accuracy specification of ±1 LSB max, and operation is guaranteed monotonic with a ±1 LSB DNL maximum specification.

The part uses a versatile 3-wire serial interface that operates at clock rates up to 35 MHz and that is compatible with standard SPI, QSPI™, MICROWIRE™, and DSP interface standards. The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V in a known output impedance state and remains in this state until a valid write to the device takes place. The part provides an output clamp feature that places the output in a defined load state.

The AD5791-EP is available in a compact, 20-lead TSSOP package and operates at the extended automotive temperature range of −55°C to +125°C. Additional application and technical information can be found in the AD5791 data sheet.

PRODUCT HIGHLIGHTS

1. 1 ppm Accuracy.
2. Wide Power Supply Range up to ±16.5 V.
3. Operating Temperature Range: −55°C to +125°C.
4. Low 7.5 nV/√Hz Noise Spectral Density.
5. Low 0.05 ppm/°C Temperature Drift.

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[1] Protected by U.S. Patents No. 7,884,747 and 8,089,380. Other patents pending.

Rev. A **Document Feedback**

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2/12—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 12.5 V to 16.5 V, V_{SS} = −16.5 V to −12.5 V, V_{REFP} = 10 V, V_{REFN} = −10 V, V_{CC} = 2.7 V to +5.5 V, IOV_{CC} = 1.71 V to 5.5 V, R_L = unloaded, C_L = unloaded, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	20			Bits	
Integral Nonlinearity Error (Relative Accuracy)	−1	±0.25	+1	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V, T_A = 0°C to 105°C
	−1.5	±0.25	+1.5	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V
	−1.5	±0.5	+1.5	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3]
	−3	±1	+3	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3]
Differential Nonlinearity Error	−1	±0.5	+1	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V
	−1.5	±0.75	+1.5	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V
	−2.5	±1	+2.5	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V
Linearity Error Long-Term Stability[4]		0.16		LSB	After 500 hours at T_A = 125°C
		0.19		LSB	After 1000 hours at T_A = 125°C
		0.11		LSB	After 1000 hours at T_A = 100°C
Full-Scale Error	−7	±0.1	+7	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−11	±0.25	+11	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3]
	−21	±0.8	+21	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3]
	−4	±0.1	+4	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3], T_A = 0°C to 105°C
	−4	±0.25	+4	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
	−6	±0.8	+6	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
Full-Scale Error Temperature Coefficient		±0.02		ppm FSR/°C	
Zero-Scale Error	−7	±0.1	+7	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−10	±0.15	+10	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3]
	−21	±0.75	+21	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3]
	−4	±0.1	+4	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3], T_A = 0°C to 105°C
	−4	±0.15	+4	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
	−6	±0.75	+6	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
Zero-Scale Error Temperature Coefficient[3]		±0.04		ppm FSR/°C	
Gain Error	−6	±0.3	+6	ppm FSR	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−10	±0.4	+10	ppm FSR	V_{REFP} = 10 V, V_{REFN} = 0 V[3]
	−20	±0.4	+20	ppm FSR	V_{REFP} = 5 V, V_{REFN} = 0 V[3]
	−6	±0.3	+6	ppm FSR	V_{REFP} = +10 V, V_{REFN} = −10 V[3], T_A = 0°C to 105°C
	−6	±0.4	+6	ppm FSR	V_{REFP} = 10 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
	−7	±0.4	+7	ppm FSR	V_{REFP} = 5 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
Gain Error Temperature Coefficient[3]		±0.04		ppm FSR/°C	
R1, R_{FB} Matching		0.01		%	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	V_{REFN}		V_{REFP}	V	
Output Slew Rate		50		V/µs	
Output Voltage Settling Time		1		µs	10 V step to 0.02%, using the AD845 buffer in unity-gain mode
		1		µs	500 code step to ±1 LSB[5]
Output Noise Spectral Density		7.5		nV/√Hz	at 1 kHz, DAC code = midscale
		7.5		nV/√Hz	at 10 kHz, DAC code = midscale
		7.5		nV/√Hz	At 100 kHz, DAC code = midscale
Output Voltage Noise		1.1		µV p-p	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth[6]

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Midscale Glitch Impulse[7]		3.1		nV-sec	$V_{REFP} = +10$ V, $V_{REFN} = −10$ V
		1.7		nV-sec	$V_{REFP} = 10$ V, $V_{REFN} = 0$ V
		1.4		nV-sec	$V_{REFP} = 5$ V, $V_{REFN} = 0$ V
MSB Segment Glitch Impulse[7]		9.1		nV-sec	$V_{REFP} = +10$ V, $V_{REFN} = −10$ V, see Figure 42
		3.6		nV-sec	$V_{REFP} = 10$ V, $V_{REFN} = 0$ V, see Figure 43
		1.9		nV-sec	$V_{REFP} = 5$ V, $V_{REFN} = 0$ V, see Figure 44
Output Enabled Glitch Impulse		45		nV-sec	On removal of output ground clamp
Digital Feedthrough		0.4		nV-sec	
DC Output Impedance (Normal Mode)		3.4		kΩ	
DC Output Impedance (Output Clamped to Ground)		6		kΩ	
Spurious Free Dynamic Range		100		dB	1 kHz tone, 10 kHz sample rate
Total Harmonic Distortion		97		dB	1 kHz tone, 10 kHz sample rate
REFERENCE INPUTS[3]					
V_{REFP} Input Range	5		$V_{DD} − 2.5$ V	V	
V_{REFN} Input Range	$V_{SS} + 2.5$ V		0		
DC Input Impedance	5	6.6		kΩ	V_{REFP}, V_{REFN}, code dependent, typical at midscale code
Input Capacitance		15		pF	V_{REFP}, V_{REFN}
LOGIC INPUTS[3]					
Input Current[8]	−1		+1	µA	
Input Low Voltage, V_{IL}			$0.3 \times IOV_{CC}$	V	$IOV_{CC} = 1.71$ V to 5.5 V
Input High Voltage, V_{IH}	$0.7 \times IOV_{CC}$			V	$IOV_{CC} = 1.71$ V to 5.5 V
Pin Capacitance		5		pF	
LOGIC OUTPUT (SDO)[3]					
Output Low Voltage, V_{OL}			0.4	V	$IOV_{CC} = 1.71$ V to 5.5 V, sinking 1 mA
Output High Voltage, V_{OH}	$IOV_{CC} − 0.5$ V			V	$IOV_{CC} = 1.71$ V to 5.5 V, sourcing 1 mA
High Impedance Leakage Current			±1	µA	
High Impedance Output Capacitance		3		pF	
POWER REQUIREMENTS					All digital inputs at DGND or IOV_{CC}
V_{DD}	7.5		$V_{SS} + 33$	V	
V_{SS}	$V_{DD} − 33$		−2.5	V	
V_{CC}	2.7		5.5	V	
IOV_{CC}	1.71		5.5	V	$IOV_{CC} \leq V_{CC}$
I_{DD}		4.2	5.2	mA	
I_{SS}		4	4.9	mA	
I_{CC}		600	900	µA	
IOI_{CC}		52	140	µA	SDO disabled
DC Power Supply Rejection Ratio[3, 9]		±0.6		µV/V	V_{DD} ± 10%, $V_{SS} = 15$ V
		±0.6		µV/V	V_{SS} ± 10%, $V_{DD} = 15$ V
AC Power Supply Rejection Ratio[3]		95		dB	V_{DD} ± 200 mV, 50 Hz/60 Hz, $V_{SS} = −15$ V
		95		dB	ΔV_{SS} ± 200 mV, 50 Hz/60 Hz, $V_{DD} = 15$ V

[1] Temperature range: −55°C to +125°C, typical at +25°C and $V_{DD} = +15$ V, $V_{SS} = −15$ V, $V_{REFP} = +10$ V, $V_{REFN} = −10$ V.

[2] Performance characterized with AD8676BRZ voltage reference buffers and AD8675ARZ output buffer.

[3] Guaranteed by design and characterization; not production tested.

[4] Linearity error refers to both INL error and DNL error, either parameter can be expected to drift by the amount specified after the length of time specified.

[5] AD5791-EP configured in ×2 gain mode, 25 pF compensation capacitor on AD797.

[6] Includes noise contribution from AD8676BRZ voltage reference buffers.

[7] The AD5791-EP is configured in bias compensation mode with a low-pass RC filter on the output. R = 300 Ω, C = 143 pF (total capacitance seen by the output buffer, lead capacitance, and so forth).

[8] Current flowing in an individual logic pin.

[9] Includes PSRR of AD8676BRZ voltage reference buffers.

TIMING CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit[1]		Unit	Test Conditions/Comments
	IOV_{CC} = 1.71 V to 3.3 V	IOV_{CC} = 3.3 V to 5.5 V		
t_1[2]	40	28	ns min	SCLK cycle time
	92	60	ns min	SCLK cycle time (readback mode)
t_2	15	10	ns min	SCLK high time
t_3	9	5	ns min	SCLK low time
t_4	5	5	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	2	2	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge hold time
t_6	48	40	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_7	8	6	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore
t_8	9	7	ns min	Data setup time
t_9	12	7	ns min	Data hold time
t_{10}	13	10	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge
t_{11}	20	16	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{12}	14	11	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{13}	130	130	ns typ	$\overline{\text{LDAC}}$ falling edge to output response time
t_{14}	130	130	ns typ	$\overline{\text{SYNC}}$ rising edge to output response time ($\overline{\text{LDAC}}$ tied low)
t_{15}	50	50	ns min	$\overline{\text{CLR}}$ pulse width low
t_{16}	140	140	ns typ	$\overline{\text{CLR}}$ pulse activation time
t_{17}	0	0	ns min	$\overline{\text{SYNC}}$ falling edge to first SCLK rising edge
t_{18}	65	60	ns max	$\overline{\text{SYNC}}$ rising edge to SDO tristate (C_L = 50 pF)
t_{19}	62	45	ns max	SCLK rising edge to SDO valid (C_L = 50 pF)
t_{20}	0	0	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK rising edge ignore
t_{21}	35	35	ns typ	$\overline{\text{RESET}}$ pulse width low
t_{22}	150	150	ns typ	$\overline{\text{RESET}}$ pulse activation time

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

[2] Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

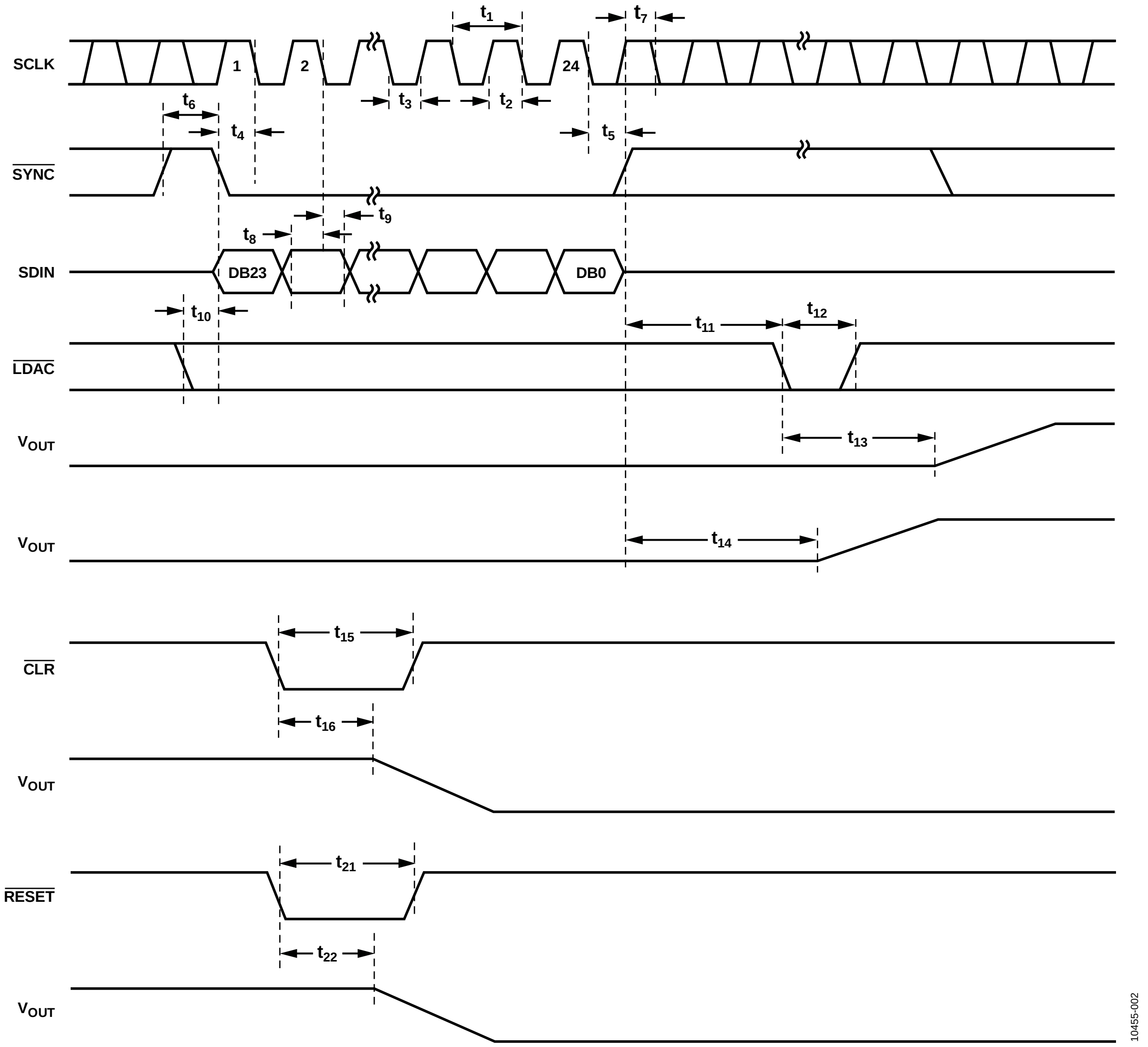


Figure 2. Write Mode Timing Diagram

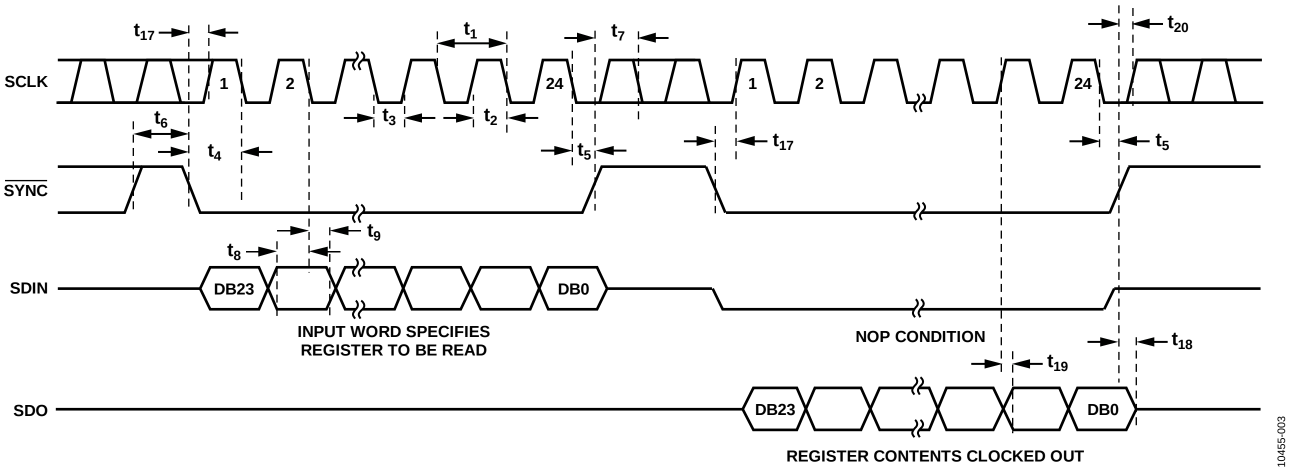


Figure 3. Readback Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	−34 V to +0.3 V
V_{DD} to V_{SS}	−0.3 V to +34 V
V_{CC} to DGND	−0.3 V to +7 V
IOV_{CC} to DGND	−0.3 V to V_{CC} + 0.3 V or +7 V (whichever is less)
Digital Inputs to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFPF} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFPS} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFNF} to AGND	V_{SS} − 0.3 V to + 0.3 V
V_{REFNS} to AGND	V_{SS} − 0.3 V to + 0.3 V
DGND to AGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A	
Industrial	−55°C to + 125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature, T_J max	150°C
Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	1.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of 1.5 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

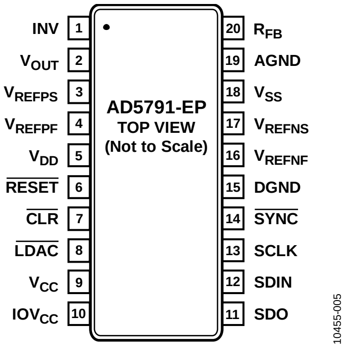


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INV	Connection to Inverting Input of External Amplifier.
2	V_{OUT}	Analog Output Voltage.
3	V_{REFPS}	Positive Reference Sense Voltage Input. A voltage range of 5 V to V_{DD} − 2.5 V can be connected. A unity gain amplifier must be connected at this pin in conjunction with the V_{REFPF} pin.
4	V_{REFPF}	Positive Reference Force Voltage Input. A voltage range of 5 V to V_{DD} − 2.5 V can be connected. A unity gain amplifier must be connected at this pin in conjunction with the V_{REFPS} pin.
5	V_{DD}	Positive Analog Supply Connection. A voltage range of 7.5 V to 16.5 V can be connected; V_{DD} should be decoupled to AGND.
6	$\overline{\text{RESET}}$	Active Low Reset Logic Input Pin. Asserting this pin returns the AD5791-EP to its power-on status.
7	$\overline{\text{CLR}}$	Active Low Clear Logic Input Pin. Asserting this pin sets the DAC register to a user defined value and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	$\overline{\text{LDAC}}$	Active Low Load DAC Logic Input Pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the input register is updated, but the output update is held off until the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin should not be left unconnected.
9	V_{CC}	Digital Supply Connection. A voltage range of 2.7 V to 5.5 V can be connected. V_{CC} should be decoupled to DGND.
10	IOV_{CC}	Digital Interface Supply Pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage in the range of 1.71 V to 5.5 V can be connected. IOV_{CC} should not be allowed to exceed V_{CC}.
11	SDO	Serial Data Output Pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial Data Input Pin. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	$\overline{\text{SYNC}}$	Active Low Digital Interface Synchronization Input Pin. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$.
15	DGND	Ground Reference Pin for Digital Circuitry.
16	V_{REFNF}	Negative Reference Force Voltage Input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin in conjunction with the V_{REFNS} pin.
17	V_{REFNS}	Negative Reference Sense Voltage Input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin in conjunction with the V_{REFNF} pin.
18	V_{SS}	Negative Analog Supply Connection. A voltage range of −16.5 V to −2.5 V can be connected. V_{SS} should be decoupled to AGND.
19	AGND	Ground Reference Pin for Analog Circuitry.
20	R_{FB}	Feedback Connection for External Amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

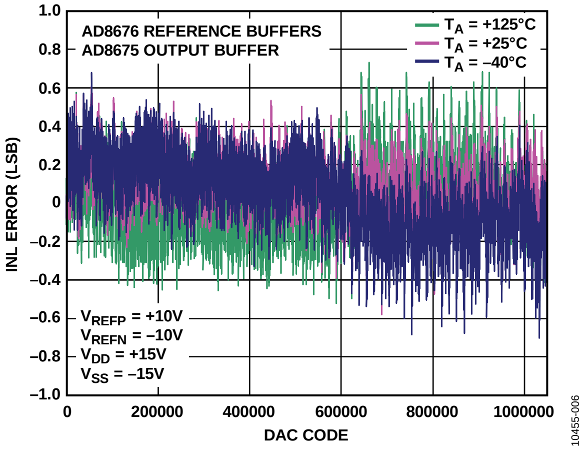


Figure 5. Integral Nonlinearity Error vs. DAC Code, ±10 V Span

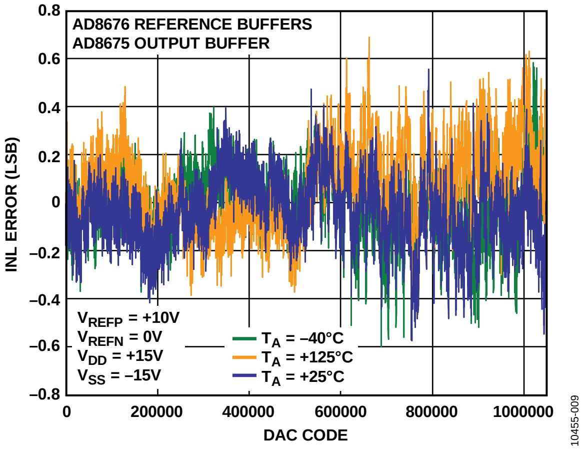


Figure 8. Integral Nonlinearity Error vs. DAC Code, ±10 V Span, ×2 Gain Mode

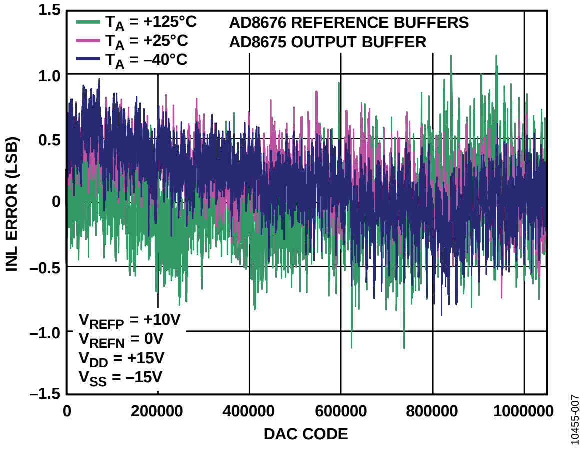


Figure 6. Integral Nonlinearity Error vs. DAC Code, 10 V Span

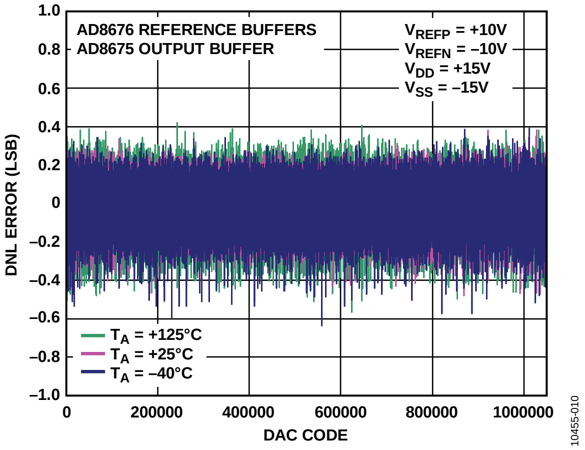


Figure 9. Differential Nonlinearity Error vs. DAC Code, ±10 V Span

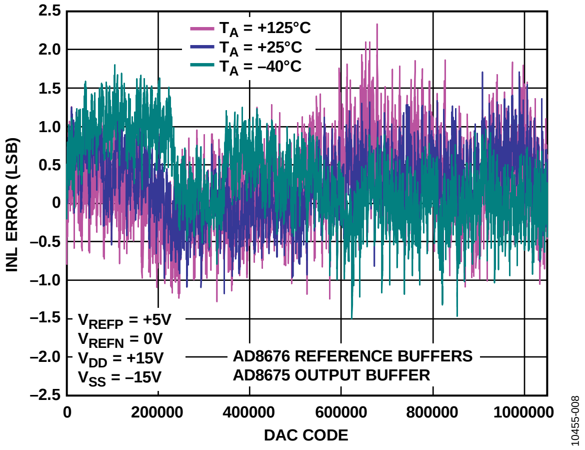


Figure 7. Integral Nonlinearity Error vs. DAC Code, 5 V Span

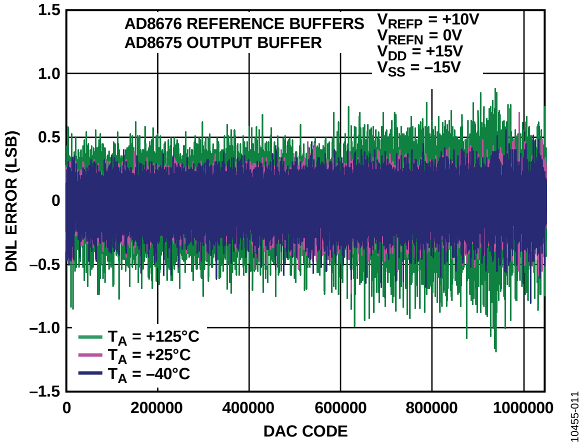


Figure 10. Differential Nonlinearity Error vs. DAC Code, 10 V Span

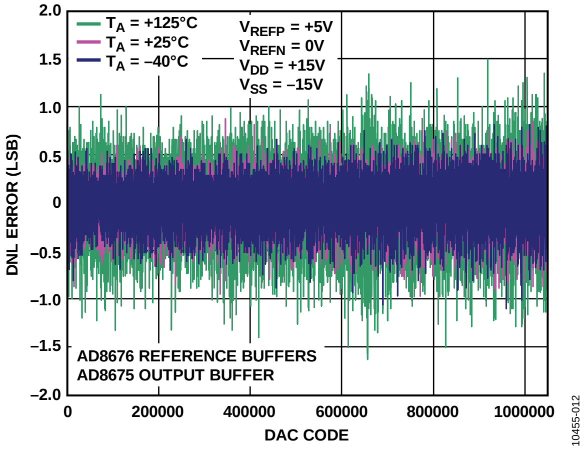


Figure 11. Differential Nonlinearity Error vs. DAC Code, 5 V Span

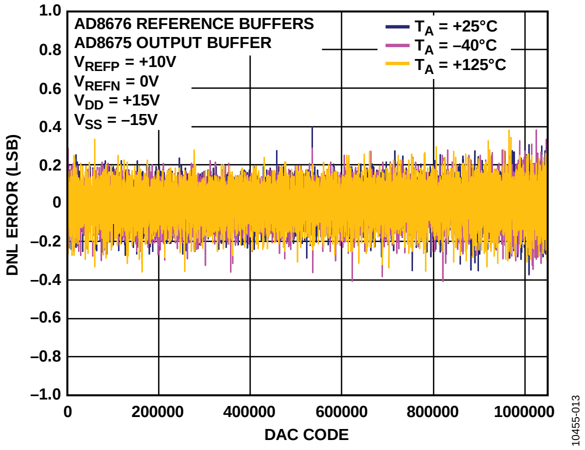


Figure 12. Differential Nonlinearity Error vs. DAC Code, ±10 V Span, ×2 Gain Mode

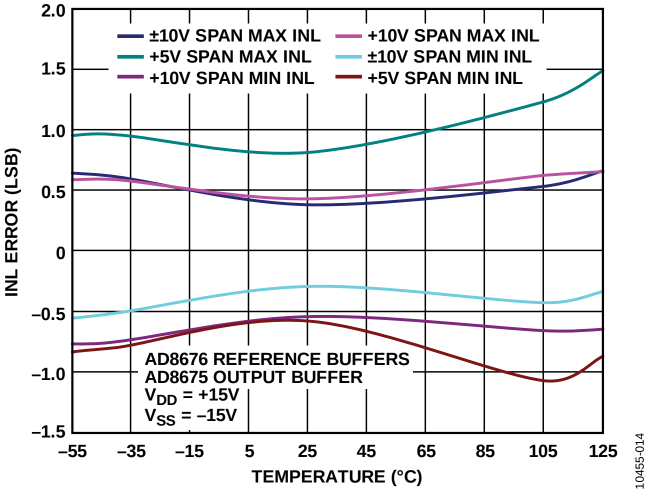


Figure 13. Integral Nonlinearity Error vs. Temperature

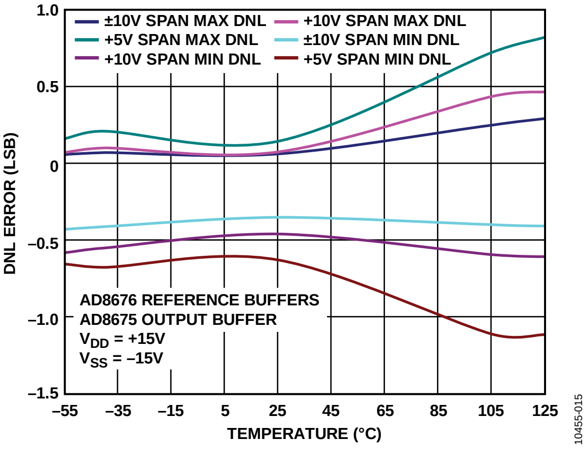


Figure 14. Differential Nonlinearity Error vs. Temperature

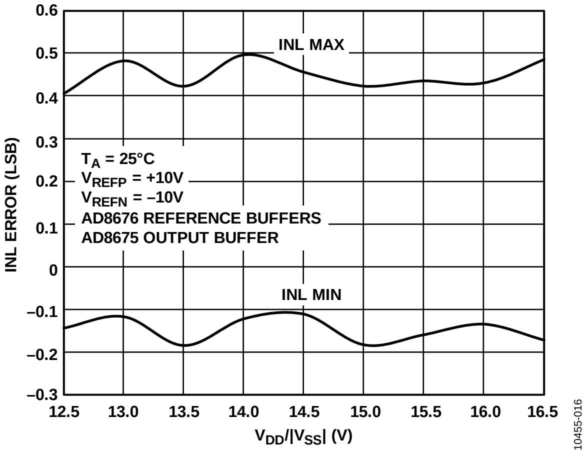


Figure 15. Integral Nonlinearity Error vs. Supply Voltage, ±10 V Span

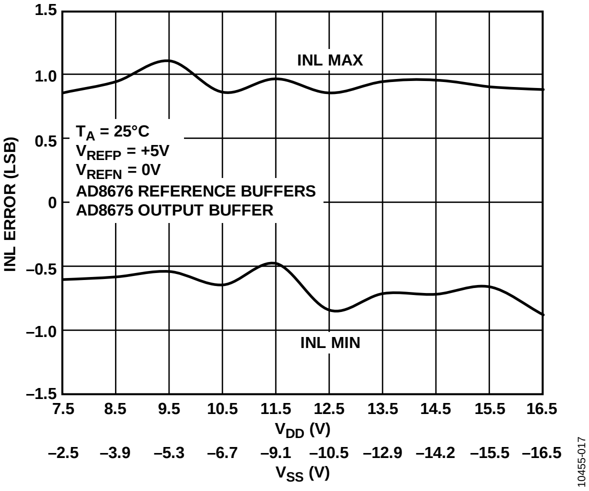


Figure 16. Integral Nonlinearity Error vs. Supply Voltage, 5 V Span

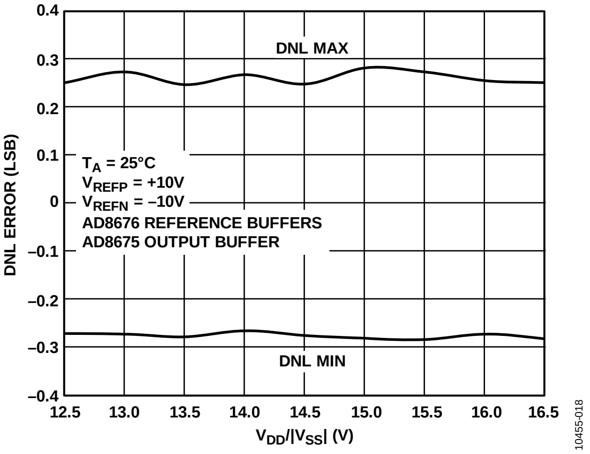


Figure 17. Differential Nonlinearity Error vs. Supply Voltage, ±10 V Span

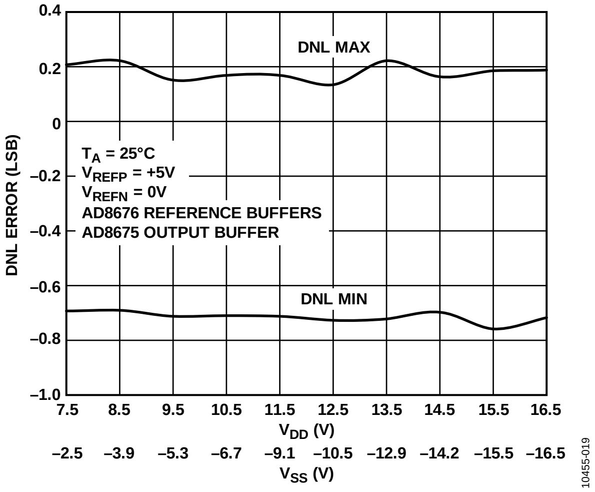


Figure 18. Differential Nonlinearity Error vs. Supply Voltage, 5 V Span

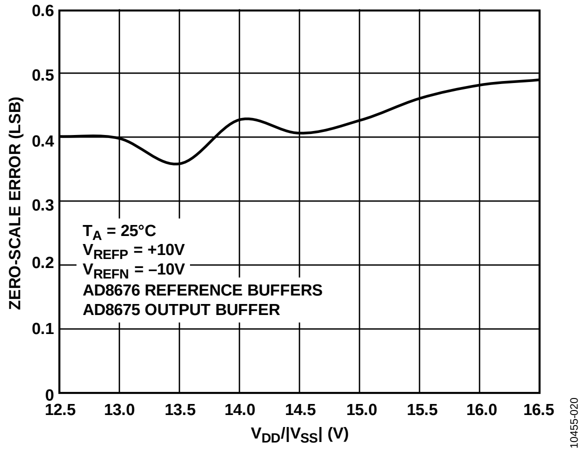


Figure 19. Zero-Scale Error vs. Supply Voltage, ±10 V Span

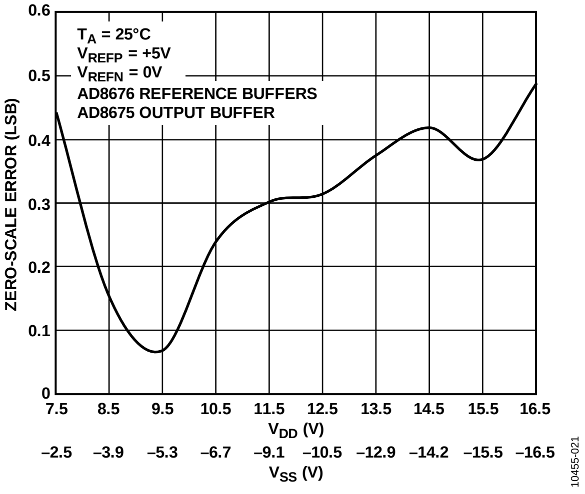


Figure 20. Zero-Scale Error vs. Supply Voltage, 5 V Span

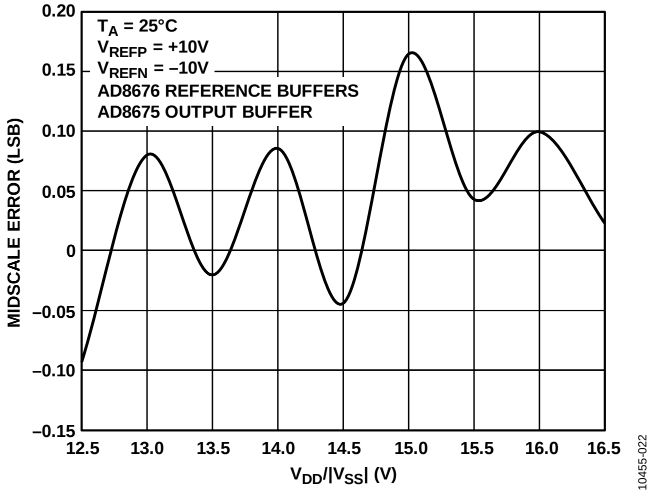


Figure 21. Midscale Error vs. Supply Voltage, ±10 V Span

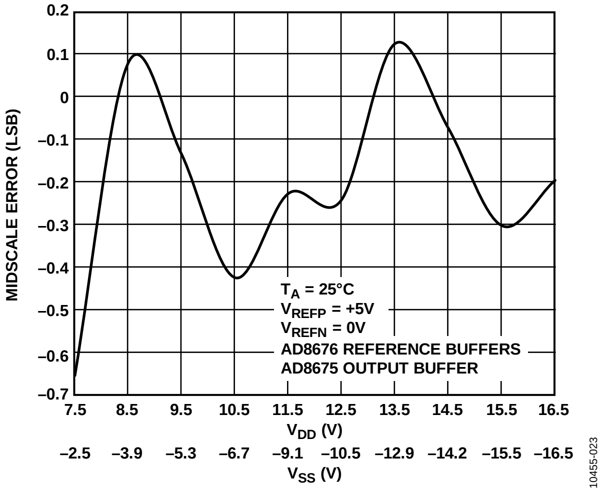


Figure 22. Midscale Error vs. Supply Voltage, 5 V Span

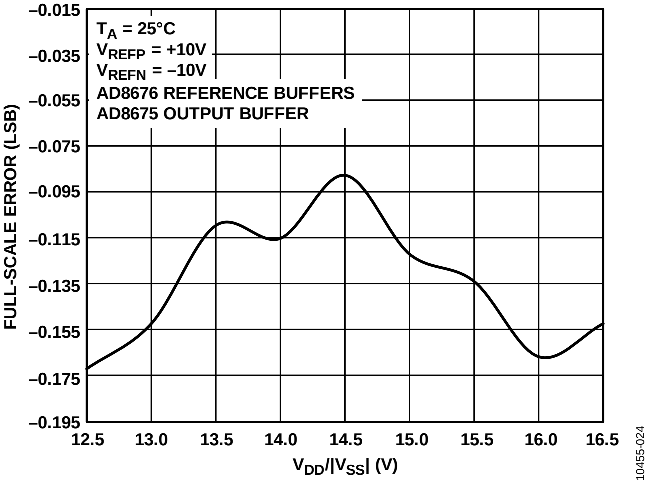


Figure 23. Full-Scale Error vs. Supply Voltage, ±10 V Span

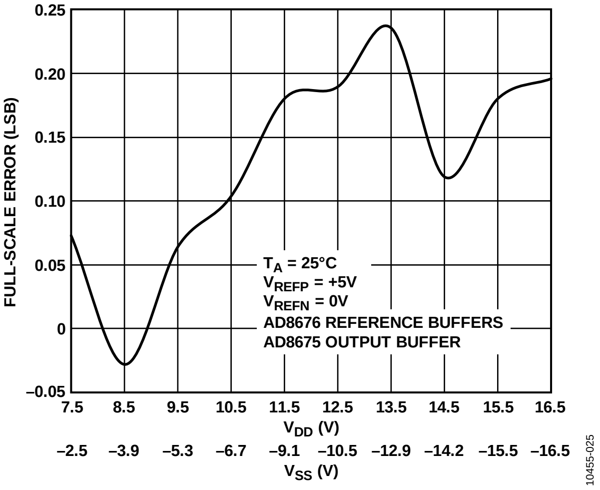


Figure 24. Full-Scale Error vs. Supply Voltage, 5 V Span

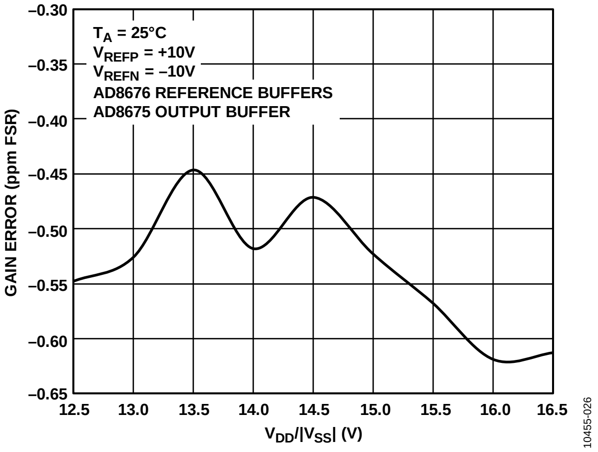


Figure 25. Gain Error vs. Supply Voltage, ±10 V Span

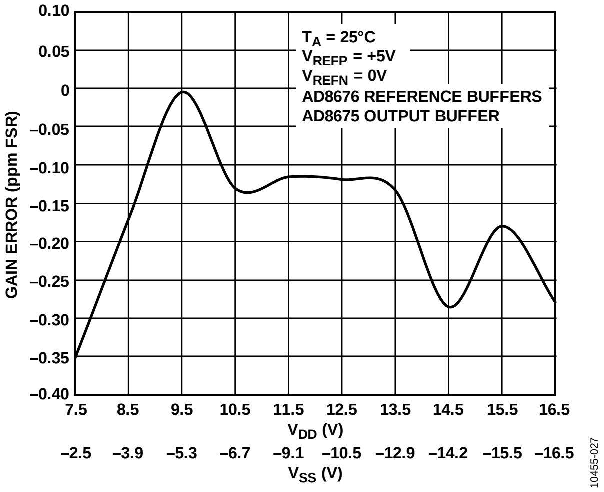


Figure 26. Gain Error vs. Supply Voltage, 5 V Span

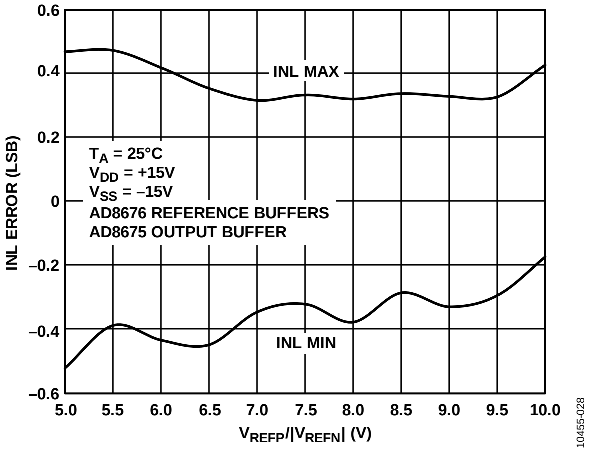


Figure 27. Integral Nonlinearity Error vs. Reference Voltage

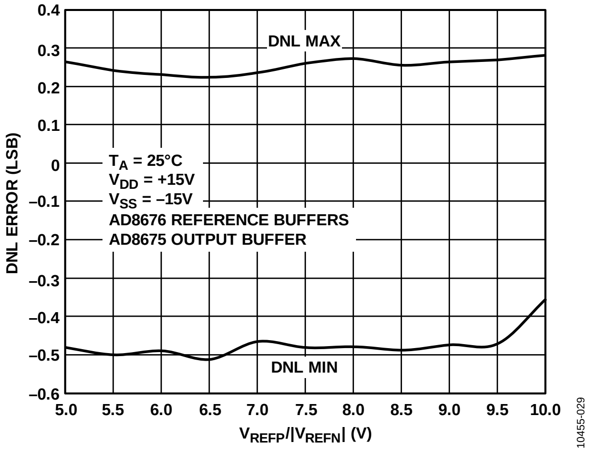


Figure 28. Differential Nonlinearity Error vs. Reference Voltage

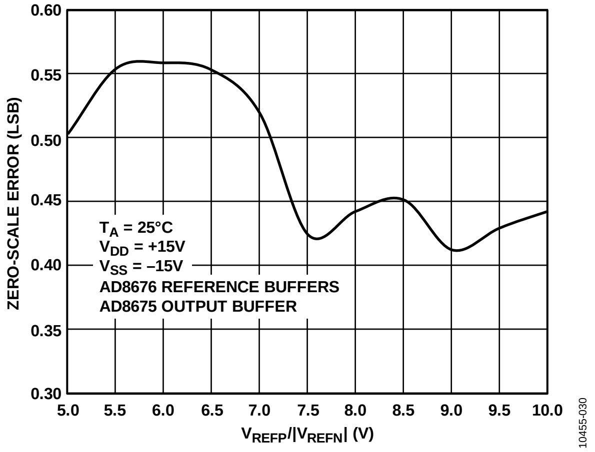


Figure 29. Zero-Scale Error vs. Reference Voltage

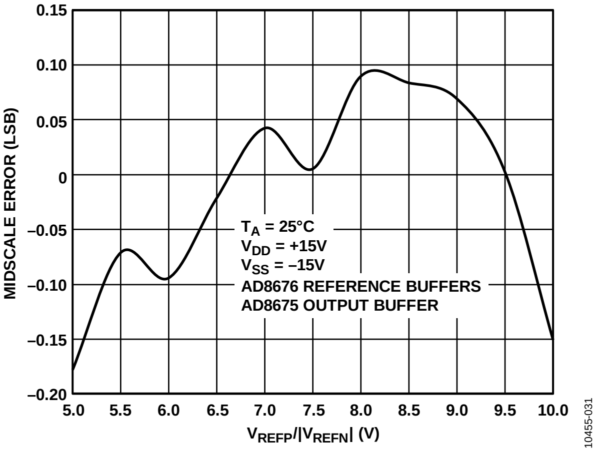


Figure 30. Midscale Error vs. Reference Voltage

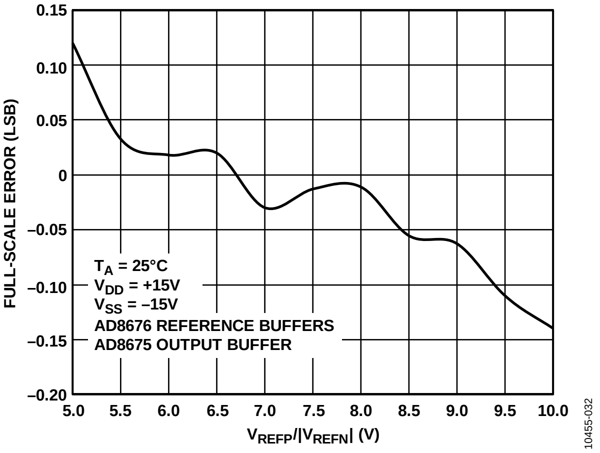


Figure 31. Full-Scale Error vs. Reference Voltage

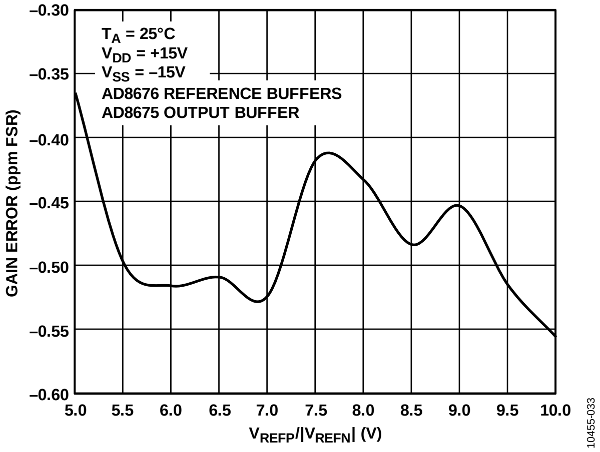


Figure 32. Gain Error vs. Reference Voltage

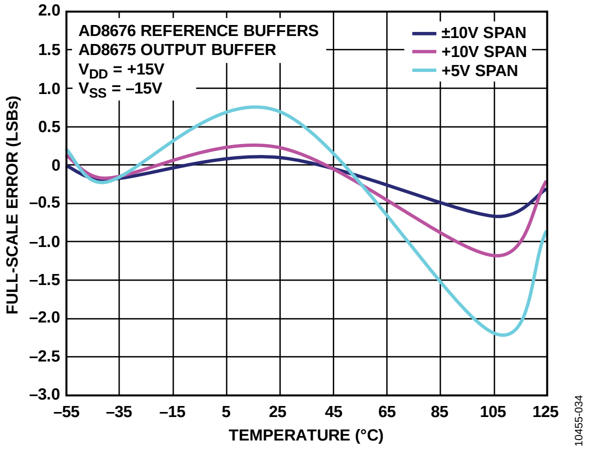


Figure 33. Full-Scale Error vs. Temperature

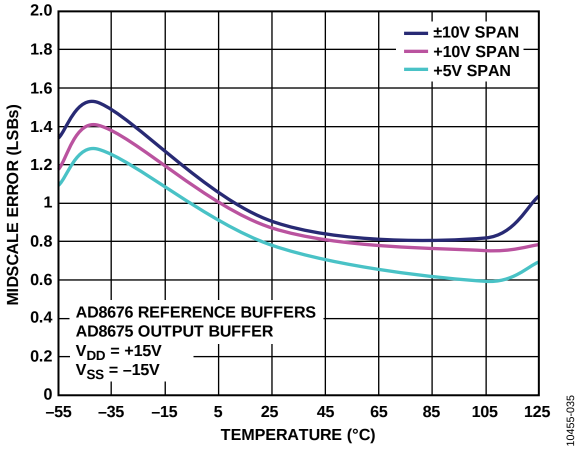


Figure 34. Midscale Error vs. Temperature

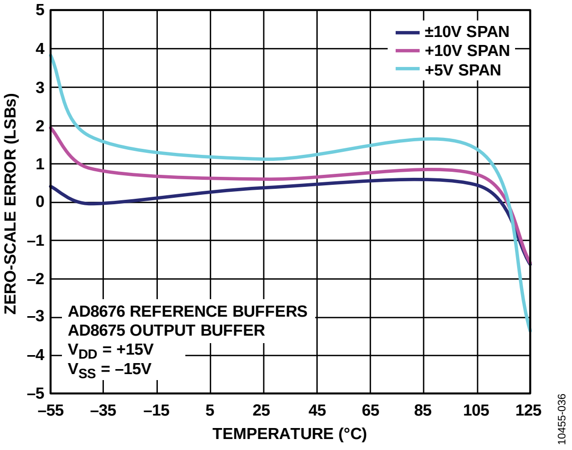


Figure 35. Zero-Scale Error vs. Temperature

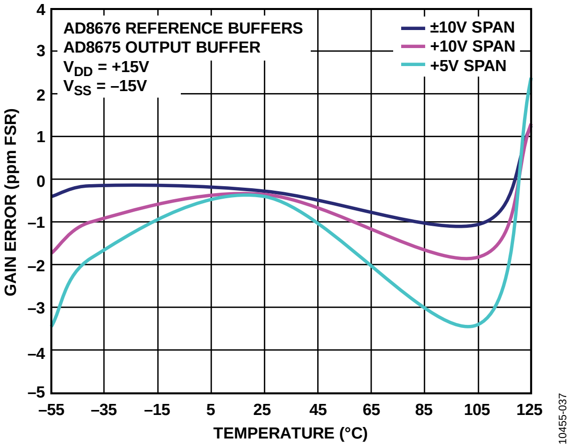


Figure 36. Gain Error vs. Temperature

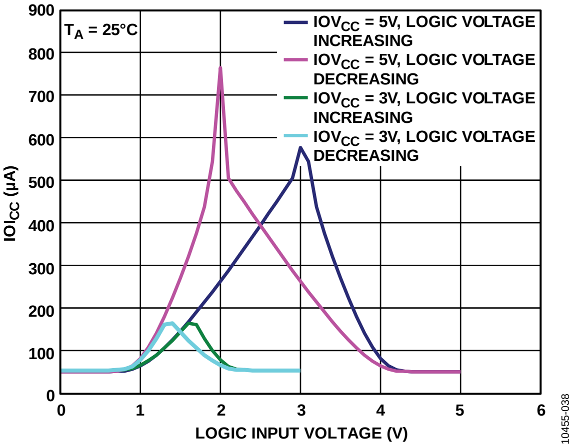


Figure 37. IOI$_{CC}$ vs. Logic Input Voltage

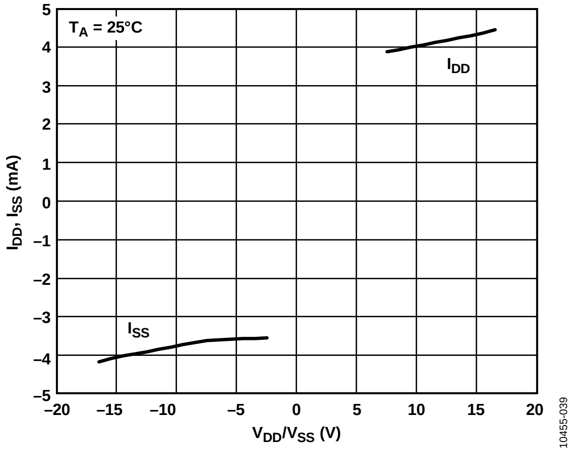


Figure 38. Power Supply Currents vs. Power Supply Voltages

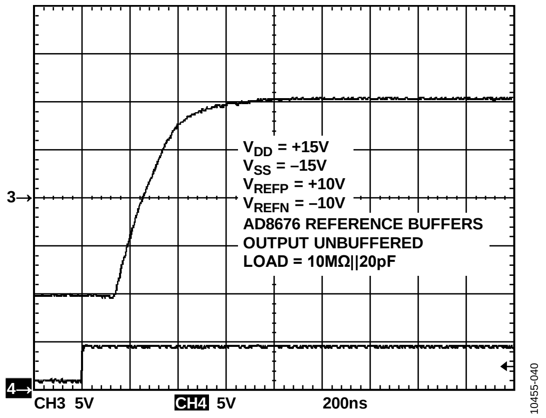


Figure 39. Rising Full-Scale Voltage Step

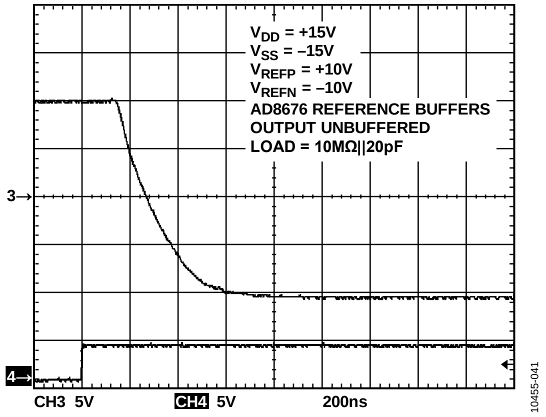


Figure 40. Falling Full-Scale Voltage Step

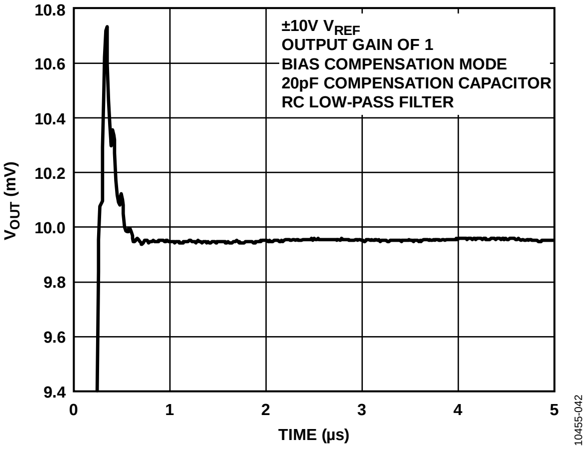


Figure 41. 500 Code Step Settling Time

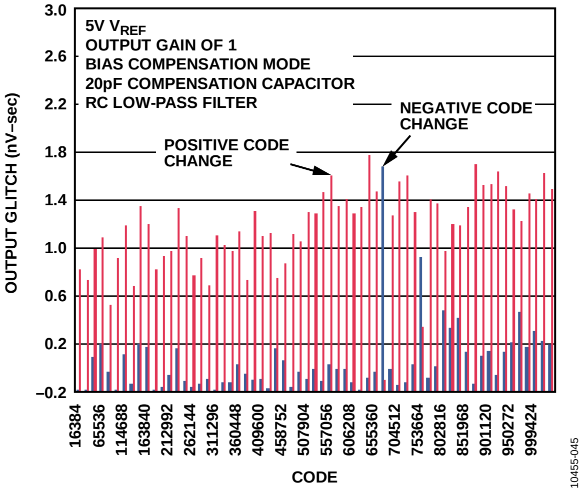


Figure 44. 6 MSB Segment Glitch Energy for +5 V V_{REF}

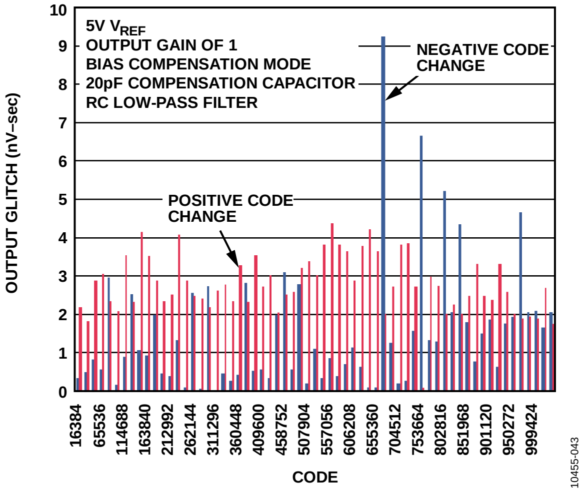


Figure 42. 6 MSB Segment Glitch Energy for ±10 V V_{REF}

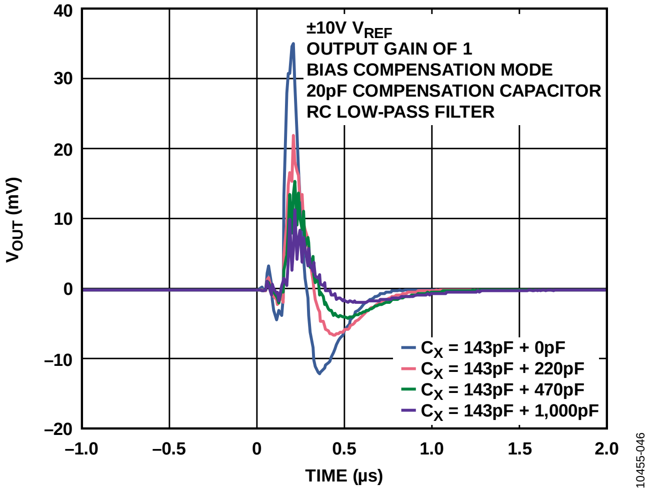


Figure 45. Midscale Peak-to-Peak Glitch for ±10 V

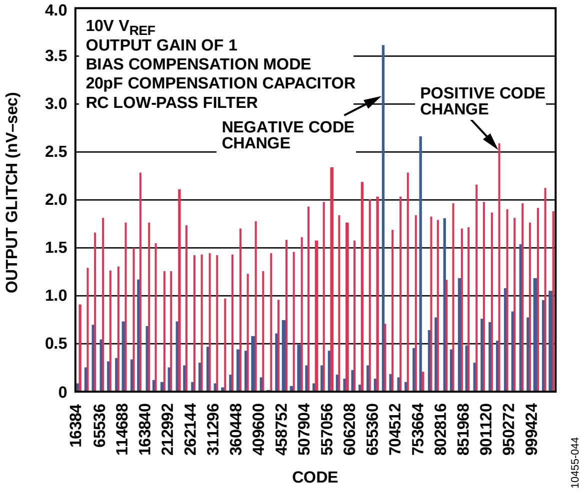


Figure 43. 6 MSB Segment Glitch Energy for +10 V V_{REF}

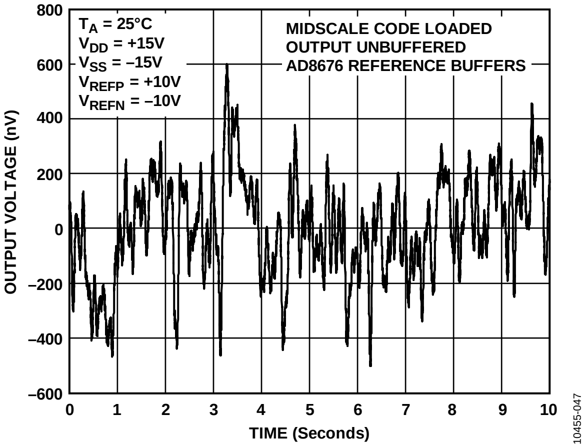


Figure 46. Voltage Output Noise, 0.1 Hz to 10 Hz Bandwidth

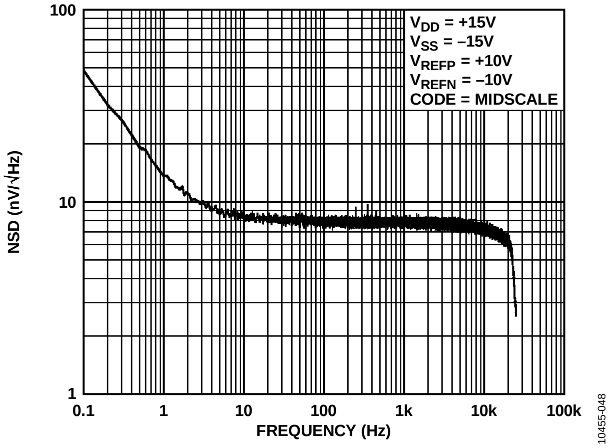


Figure 47. Noise Spectral Density vs. Frequency

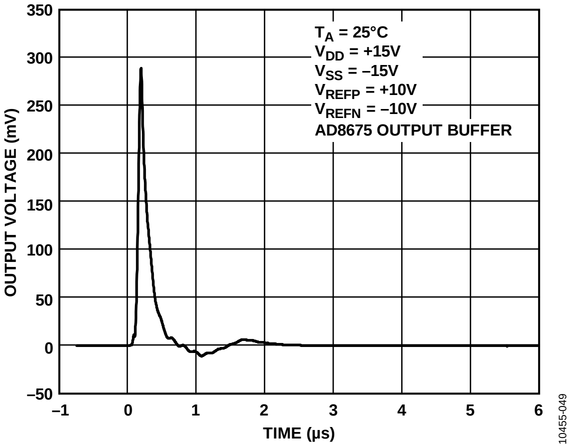
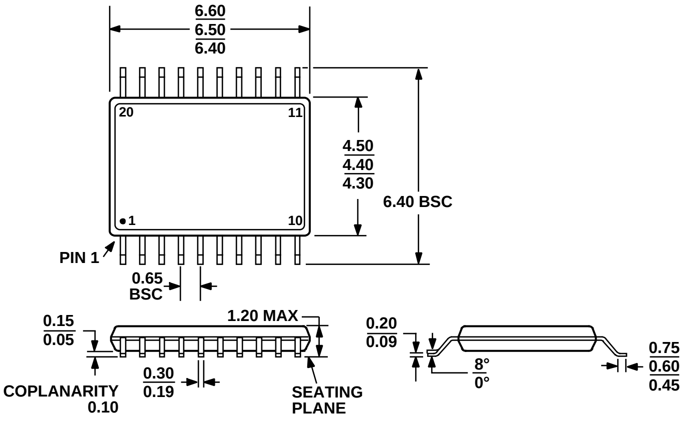


Figure 48. Glitch Impulse on Removal of Output Clamp

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 49. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	INL	Package Description	Package Option
AD5791SRU-EP	−55°C to +125°C	±1.5 LSB	20-Lead TSSOP	RU-20

NOTES

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