NCP1216AFORWGEVB

Implementing a DC/DC Single-ended Forward Converter with the NCP1216A Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

This document describes how the NCP1216A controller can be used to design a DC/DC single-ended forward converter suitable for telecommunication applications. The requirements for the converter are as follows:

- Input Voltage Range from 36 V to 72 VDC
- Continuous Output Power Greater than 30 W for a 12 V Output Voltage
- Small PCB Dimensions
- Efficiency Greater then 85%
- Input to Output Isolation Voltage of 1500 V

The NCP1216A controller is an attractive solution for this application, due to the following features:

- **50% Maximum Duty Cycle Operation**
  Forward converters usually limit the maximum duty cycle to 50%. Since the voltage reset is constrained to be equal to the input voltage (1:1 reset ratio), it is not desirable to exceed 50% DC to avoid saturating the transformer core.
- **No Auxiliary Winding Operation**
  The DSS (Dynamic Self-supply) function allows the NCP1216A derive power directly from the HV line without having to supply V_{CC} either from the secondary output inductance (creepage distance and isolation issues) or via an auxiliary winding delivering a variable voltage of $N \times V_{in}$.
- **500 mA Peak Current Capability**
  The NCP1216A can drive a MOSFET directly without any additional driver stage. If the selected MOSFET gate charge would overload the DSS capability, then an auxiliary winding could be used solely to supply the driver pulses.
- **Current-mode Operation**
  Cycle-by-cycle primary current monitoring eliminates any overcurrent situations, e.g. resulting from a secondary short-circuit.
- **Direct Optocoupler Connection**
  In applications where the input to output isolation is required, a direct connection eases the design stage, saving external components.
- **Extremely Low No-load Power Consumption**
  Extremely low consumption in no-load operation is a great advantage of the NCP1216A controller. Today's maximum stand-by consumption standards can be easily met if this function is used.
- **Short-circuit Protection**
  By monitoring the activity on the feedback line, the NCP1216A simplifies the task of secondary side short-circuit protection. Coupling problems are eliminated thanks to this feature and the DSS implementation.

The 35 W DC/DC Converter Board Specifications

The schematic of the proposed converter is shown in Figure 1. This converter has the following specifications:

Minimum Input Voltage	36 VDC
Maximum Input Voltage	72 VDC
Output Voltage	12 VDC
Continued Output Current	3.0 A
Operating Frequency	100 kHz
No-load Consumption at 48 V	1.8 mA
Maximum Ambient Temperature	70°C

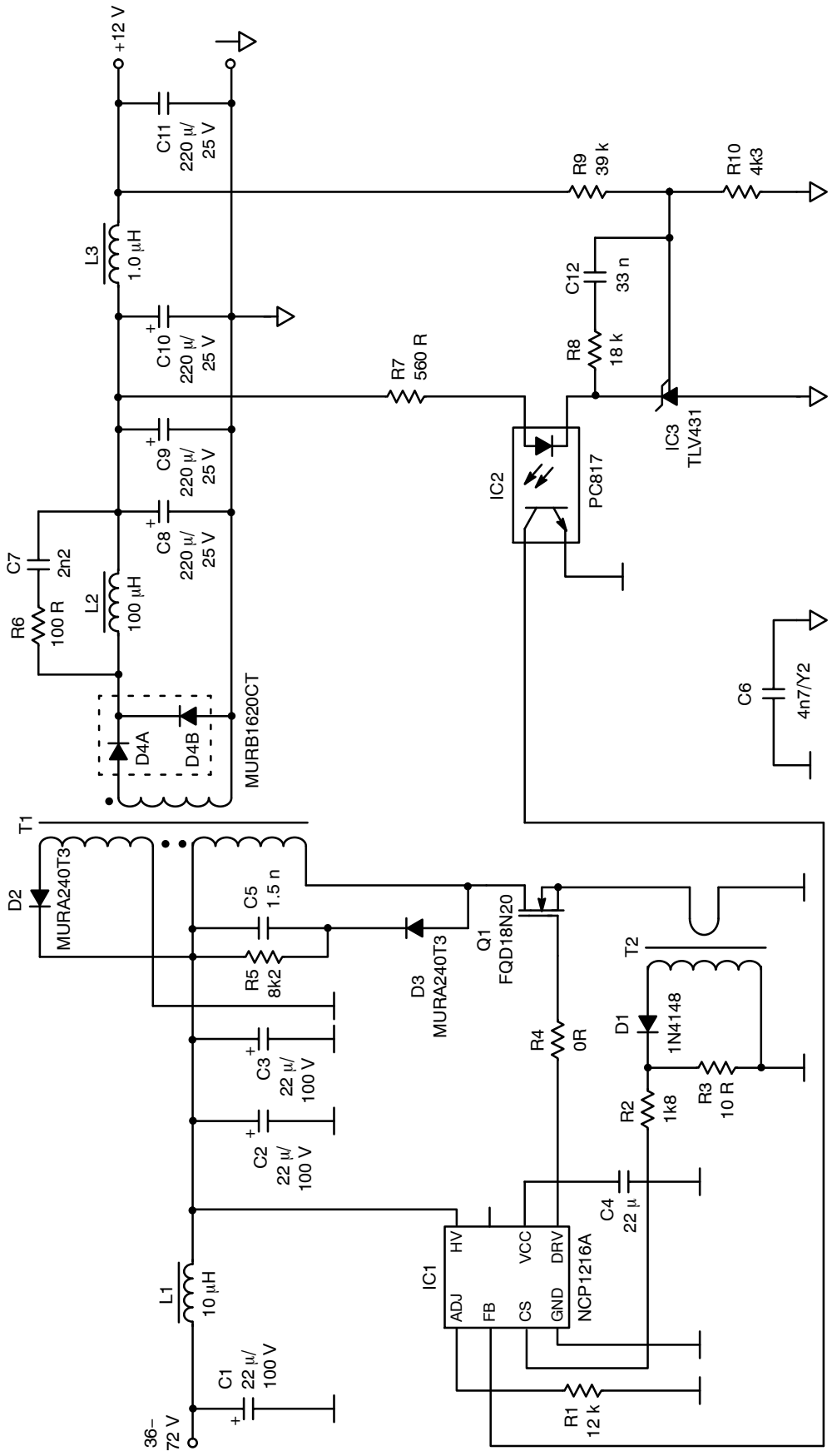

Figure 1. Schematic Diagram

Description of Converter Connection

Capacitors C1, C2, C3 and inductor L1 form the input filter. Diode D3, capacitor C5 and resistor R5 provide the primary clamping network which combats leakage inductance between the reset winding and the primary winding. The link between both windings occurs via D2 when the switch is off. Transformer T2 with diode D1 and resistors R2, R3 serve as the primary current sensing circuit. Thanks to low insertion losses, the final efficiency of the converter benefits greatly from this configuration. IC1 is the main driving circuit of the power converter. The secondary circuitry has D4A as the forward diode and D4B as the freewheeling diode. Capacitor C6 offers a path for common-mode (CM) currents circulating via the various transformer stray capacitances during switching events. Resistors R7, R8, R9, and R10 together with capacitor C12, shunt regulator IC3, and optocoupler IC2 form an isolated feedback circuit for output voltage regulation. A snubber network (R6, C7) is connected across inductor L2 in order to damp high frequency oscillations. L2, C8, C9 and C10 form the basic LC output filter. L3 and C11 form an additional output filter to reduce high frequency noise.

Design considerations for various sections of the converter are described below.

Transformer Design

In a forward converter, the core magnetization is ensured by applying a voltage V_{in} on the primary side. This action creates the core flux ϕ which links both primary and secondary windings. Using Faraday's law, we can write that $E = N.d\phi/dt$, where E is the voltage generated by a winding of N turns, energized by a flux ϕ. By integrating this formula, and rearranging it in terms of the input voltage V_{in} and the on time *ton*, we can see that the internal flux depends on the volt-second product:

$$V_{in} \cdot t_{on} = N \cdot \phi = N \cdot A_e \cdot B \qquad \text{(eq. 1)}$$

where:

A_e is the total core area
B is the core flux density

Thus, the maximum core flux density ΔB_{MAX} and the peak primary magnetization current I_{PKMAG} of the transformer are given by the primary inductance value *L1* and the maximum input voltage according to equations (2) and (3):

$$I_{PKMAG} = \frac{V_{in\ max}}{L_1} \cdot \frac{1}{f_{op}} \cdot \delta_{max} \qquad \text{(eq. 2)}$$

$$\Delta B_{MAX} = \frac{V_{in\ max} \cdot \delta_{max}}{N_p \cdot f_{op} \cdot A_e} \qquad \text{(eq. 3)}$$

where:

$V_{in\ max}$ is the maximum input voltage
L_1 is the primary winding inductance
f_{op} is the operating frequency
δ_{max} is the maximum duty cycle
N_p is the count of the primary turns

The primary magnetization current does not directly participate in the energy transfer and cause additive losses on the power switch and the primary winding. When the switch is off, the transformer core must be reset in order to let the internal flux return to zero. This is done via a dedicated reset circuit. Consequently the magnetizing current *Imag* must be kept smaller than the productive component of the primary current.

The core flux density excursion ΔB has to be chosen with respect to the characteristics of the core material: the saturation flux density *Bmax* or *Bsat*, the residual flux density *Br*, hysteretic losses and the core temperature behavior. With respect to these characteristics, the flux density excursion in high frequency converters should be between 0.15 T and 0.2 T. If a higher value is chosen, greater losses will be generated. The primary turn count N_p can be calculated by rearranging equation 4:

$$N_p = \frac{V_{in\ max} \cdot \delta_{max}}{\Delta B_{MAX} \cdot f_{op} \cdot A_e} \qquad \text{(eq. 4)}$$

For an EFD25 core with a total core area of 58 mm^2 (ΔB_{max} = 0.2 T, $V_{in\ max}$ = 80 V, f_{op} = 100 kHz and maximum duty cycle δ_{max} = 0.5) then the number of primary turns N_p = 35.

The number of reset winding turns depends on design tradeoffs. When the number of turns of the reset winding is lower than the that of the primary winding, the reflected voltage on the power switch drain will be lower than $2 \times V_{in\ max}$. However, this limits the maximum duty cycle excursion to less than 50%. Conversely, if the reset turns are larger than the primary turns, the maximum allowed duty cycle will increase but the MOSFET voltage stress will exceed $2 \times V_{in\ max}$. Due to these issues, the practical number of turns for the reset winding is usually chosen to be the same as the primary winding, or a 1:1 ratio. It is important to provide a very good coupling between these two windings. A high leakage inductance between these windings would require a hard voltage clamp that would hurt the converter efficiency.

The number of turns on the secondary winding N_s can be obtained from equation 5:

$$N_s = N_p \cdot \frac{\frac{V_{out}}{\delta_{max}} + V_f}{V_{in\ min}} \qquad \text{(eq. 5)}$$

where:

V_{out} is the desired output voltage
V_f is the voltage drop of the output rectifier
$V_{in\ min}$ is the minimum input voltage

In the example using the EFD 25, equation (5) gives N_s = 25 turns.

The primary and the secondary windings must be wound to limit the skin effect. This can be done by using several wires wound in parallel. The maximum diameter D_{max} (in mm) of each single wire in the winding is given by equation 6:

$$D_{max} = 2 \cdot \frac{75}{\sqrt{f_{op}}} \quad \text{(eq. 6)}$$

The total area of the selected wire for primary and secondary windings is a tradeoff between the desired output power, allowable conduction losses in the windings and thermal considerations. The current density in the transformer winding can generally range from 2 to 3.5 A/mm^2. If a cooling fan is used, the current density can be increased.

The reset winding can be made with a single wire technique, given the low magnetization current flowing into it.

In some cases, a small air gap can be inserted into the magnetic circuit of the forward transformer. This solution brings the residual flux density *Br* to a lower value than without a gap. The main drawback lies in the primary inductance decrease which forces a higher magnetizing current.

Output Inductor Design

The value of the output inductor selected depends on the acceptable level of ripple current. For a small ripple current, a large inductance is needed. On the other hand, when the current ripple is high, large output capacitors must be used to reduce the voltage ripple. In practice, it is usual to limit the current ripple to about 10−20% of the average current of the inductor. The maximum current ripple ΔI_{max} in a forward converter occurs at 50% duty cycle. Its value can be found via equation (7):

$$\Delta I_{max} = \frac{V_{sec\ max}}{4 \cdot f_{op} \cdot L_2} \quad \text{(eq. 7)}$$

where:

$V_{sec\ max}$ is the maximum secondary voltage
L_2 is the inductance of inductor L2

In the NCP1216A demo board, where a 100 μH inductor is used, the maximum output ripple will be ΔI_{max} = 2.0 A. This is rather high, but the allowable dimensions of the inductor limit a higher inductance value selection.

The values and types of output capacitors must be chosen with respect to the maximum allowable output voltage excursion as well as the RMS current that will flow in them.

Current Sense Transformer Design

The current sense transformer is used to reduce power losses traditionally found in the standard current sense resistor configuration. If a classical current sense resistor were used in this application, the associated power loss would be about 3.0 W. When the current sense transformer is used, power losses are about 50 mW. The disadvantage of this solution lies in the current error brought by the magnetization current of current sense transformer. This error is additive so it should accounted for and reduced.

A toroidal core with 38 turns of the secondary winding was used in NCP1216A demo board. The primary winding is created by one turn of isolated wire. The peak current I_{2pk} of the current sense resistor can be obtained from equation 8:

$$I_{2pk} = I_{1pk} \cdot \frac{1}{N_s} - I_{magpk} \quad \text{(eq. 8)}$$

where:

I_{1pk} is the peak current of the power switch
N_s is the count of secondary turns
I_{magpk} is the peak value of the magnetization current

Figure 2 shows the current sense transformer circuit. The peak value of the magnetization current is given by equation 9:

$$I_{magpk} = \frac{V_{csth\ max} \cdot \delta_{max}}{L_s \cdot f_{op}} \quad \text{(eq. 9)}$$

where:

$V_{csth\ max}$ is the maximum threshold voltage of the current sense input
L_s is the inductance of the secondary winding

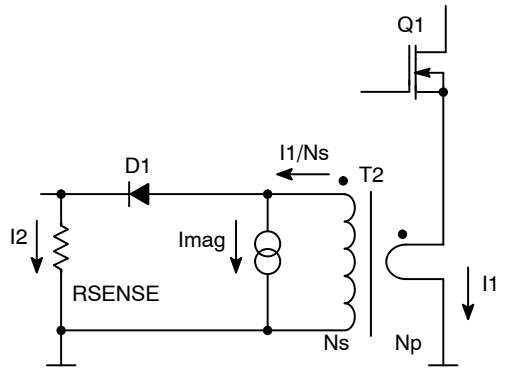

Figure 2. Implementation of the Current Sense Transformer

The value of the current sense resistor R_{sense} can be calculated by using equation 10:

$$R_{sense} = \frac{V_{csth\ max}}{I_{2pk}} \quad \text{(eq. 10)}$$

The NCP1216A Leading Edge Blanking circuit (LEB) allows the designer to avoid using a RC network to suppress voltage spikes during the switch turn-on event.

Primary RCD Clamp and Inductor Snubber Network Design

Because of manufacturing constraints, the leakage inductance between primary and secondary windings is never equal to zero. The energy stored in this leakage inductance during *ton* will cause large voltage spikes when the switch is turning off. To protect the power switch from a catastrophic voltage spike, a RCD clamping network must be used. The values of these components depend not only on the leakage inductance value but also on the reflected voltage, the parasitic influence of the layout, and the RCD capacitor. The power dissipation of the RCD clamp can be obtained from equation 11:

$$P_{clamp} = \frac{1}{2} \cdot I_{1pk}^{2} \cdot L_{leak} \cdot f_{op} \cdot \frac{V_{clamp}}{V_{clamp} - V_{refl}} \qquad \text{(eq. 11)}$$

where:

L_{leak} is value of the leakage inductance
V_{clamp} is value of the clamp voltage
V_{refl} is value of the reflected voltage ($V_{refl} = V_{in\ max}$ for forward converters with max. DC = 50%)

The optimal values of the clamping devices are given by equations 12 and 13:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot \left(V_{clamp} - V_{refl}\right)}{L_{leak} \cdot I_{1pk}^{2} \cdot f_{op}} \qquad \text{(eq. 12)}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot f_{op} \cdot R_{clamp}} \qquad \text{(eq. 13)}$$

where:

V_{ripple} is the ripple voltage level on the clamping capacitor; this ripple should be minimized.

An RC snubber network is connected across the inductor L2 to dampen the parasitic oscillations caused when the freewheel and forward diodes are switched.

Both the clamp and snubber networks dissipate heat and affect the converter efficiency.

Regulation Loop Design

A standard loop topology with a TLV431 shunt regulator is used. The optocoupler provides good isolation between input and output sides of the converter. The output voltage is set up by the R9 and R10 divider ratio according to equation 14:

$$V_{out} = 1,25 \cdot \left(1 + \frac{R_9}{R_{10}}\right) \qquad \text{(eq. 14)}$$

The maximum current flowing through the optocoupler LED is determined by resistor R7. The internal consumption of the TLV431 is low, thus avoiding another biasing element, bypassing the LED. Resistor R8 and C12 constitute the feedback loop compensation circuit. The optimal values for these components are based on the feedback response measurements.

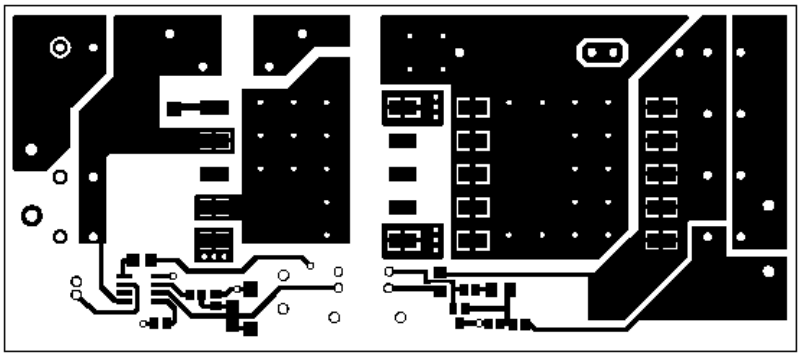

Figure 3. PCB Layout (Top Side)

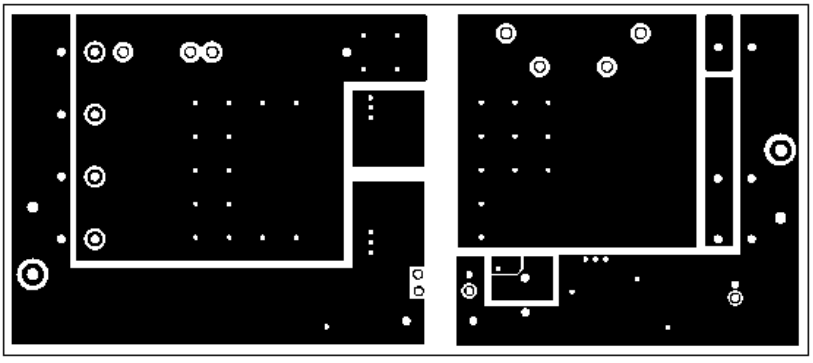

Figure 4. PCB Layout (Bottom Side)

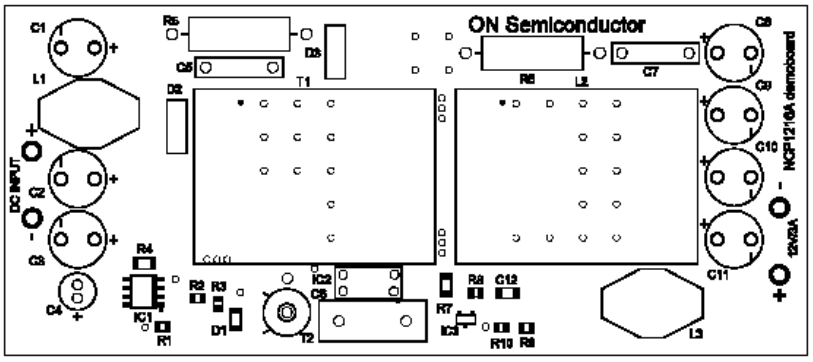

Figure 5. Component Arrangement (Top Side)

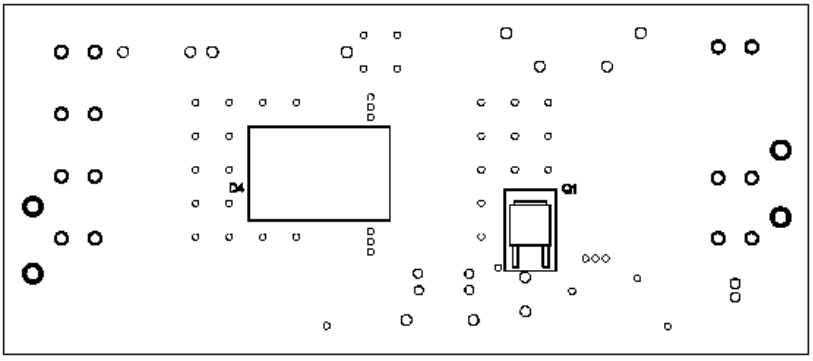

Figure 6. Component Arrangement (Bottom Side)

PCB Layout Design

A double-sided PCB is used to minimize the size of the converter. The board is designed with respect to the power dissipation created by the power devices, thus large cooling areas are used. Sound grounding techniques and appropriate isolation distances were incorporated into the layout. The PCB layout and component arrangement can be seen on Figures 3, 4, 5 and 6.

Table 1. BILL OF MATERIALS

L1	10 μH DS3316P−103−Coilcraft
L2	100 μH B0754−A−Coilcraft
L3	1.0 μH DS3316P−102−Coilcraft
T1	C0972−A−Coilcraft
T2	Toroid ϕ6.0 mm, Material T30−Epcos N_s = 38 Turns
C1, C2, C3	22 μ/100 V Nippon Chemi−Con−KMF
C4	22 μ/25 V Nippon Chemi−Con−KMF
C5	1,5 nF/500 V Through Hole Ceramic Capacitor
C6	4n7 Y2 Type Capacitor
C7	2,2 nF/500 V Through Hole Ceramic Capacitor
C8, C9, C10, C11	220 μ/25 V Nippon Chemi−Con−LXZ
C12	33 nF SMD 1206
R1	12 kΩ SMD 0805
R2	1,8 kΩ SMD 0805
R3	10 Ω SMD 0805
R4	0R SMD1206
R5	8,2 kΩ/1.0 W Through Hole
R6	100 Ω/1.0 W Through Hole
R7	560 Ω SMD1206
R8	18 kΩ SMD 0805
R9	39 kΩ SMD 0805
R10	4,3 kΩ SMD 0805
D1	MMSD914T1−ON Semiconductor
D2, D3	MURA2403T3−ON Semiconductor
D4	MURB1620CT−ON Semiconductor
Q1	FQD18N20V2TF−Fairchild
IC1	NCP1216A−ON Semiconductor
IC2	PC817−SHARP
IC3	TLV431BSN1T1−ON Semiconductor

Performance of the Converter

The power conversion efficiency of the DC/DC converter is shown in Figures 7 and 8.

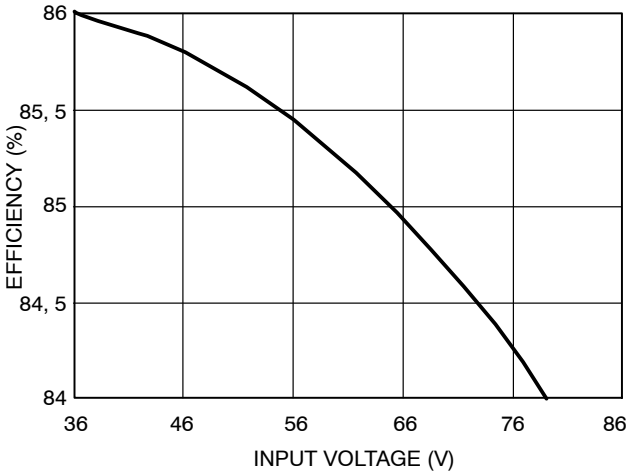

Figure 7. DC/DC Converter Efficiency vs. Input Voltage

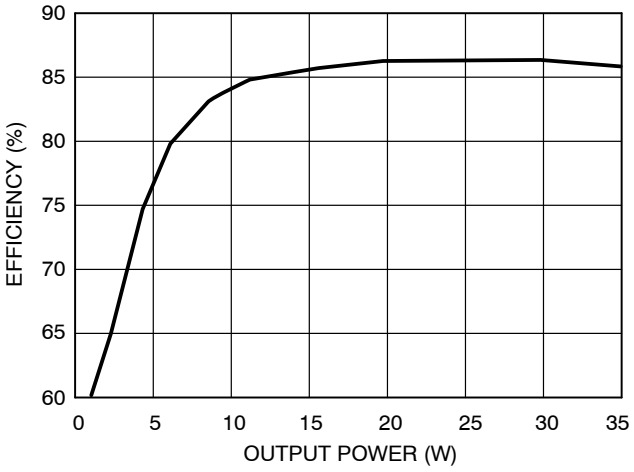

Figure 8. DC/DC Converter Efficiency vs. Output Power (V_{in} = 48 V)

The no-load consumption as a function of input voltage is shown in Figure 9.

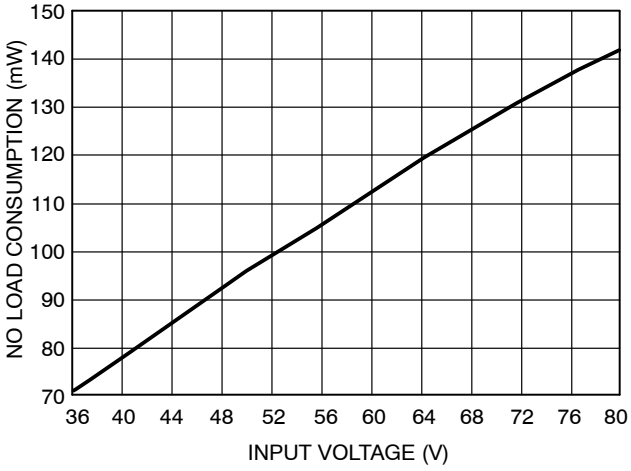

Figure 9. No Load Consumption vs. Input Voltage

The gate (trace 1) and drain (trace 2) waveforms of the power MOSFET Q1 are shown in Figures 10, 11, 12 and 13 for several converter conditions.

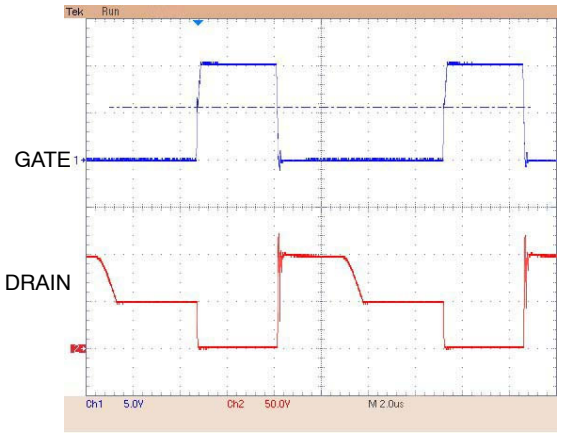

Figure 10. V_{input} = 48 V, I_{out} = 3.0 A

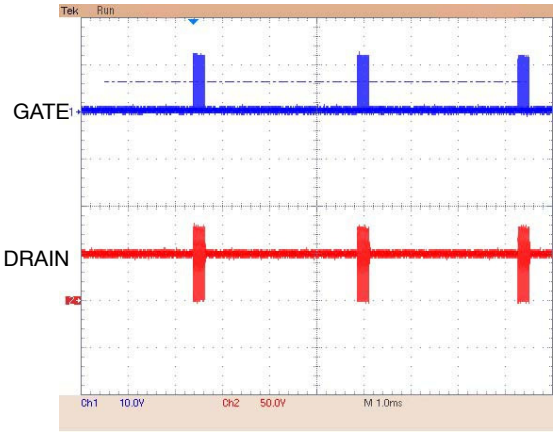

Figure 11. No Load Operation

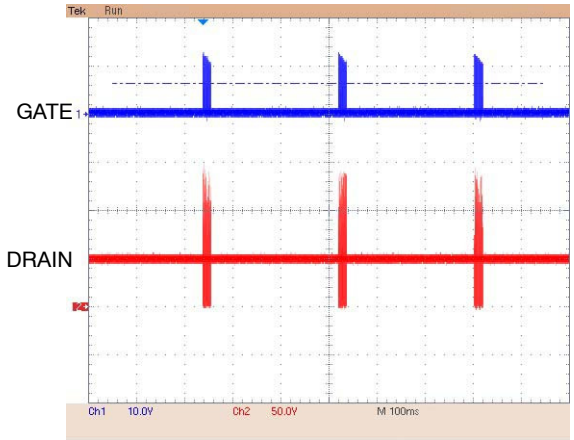

Figure 12. Overload Operation

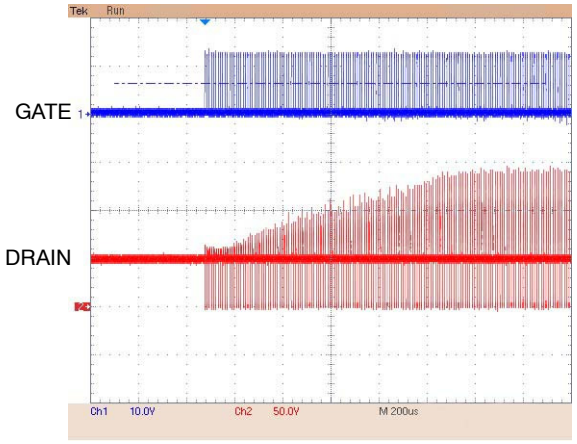

Figure 13. Detailed Burst During Overload

The load regulation for an output current step from 10% to 100% can be seen in Figure 14.

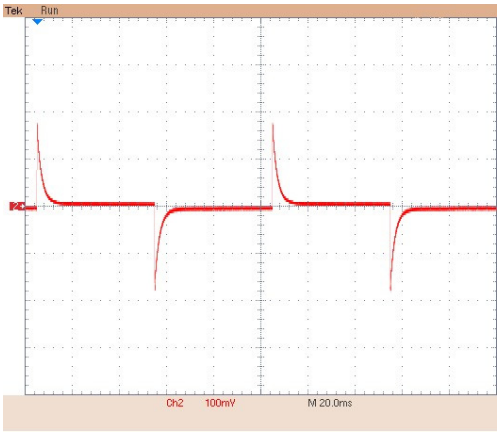

Figure 14. Load Regulation (I_{out} changing from 10% to 100%−0.3 A to 3.0 A)

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