Evaluation Board for Dual, Interleaved, Step-Down DC-to-DC Controller with Tracking

EVAL-ADP1823

INTRODUCTION

This document describes the design, operation, and test results of the ADP1823 evaluation board. The input range in this evaluation board is 5.5 V to 20 V. The output voltages are configured for V_{OUT1} = 1.8 V with a maximum current limit at 15 A and V_{OUT2} = 1.2 V with a maximum current limit at 15 A. All of the results tested from the evaluation board were running at a switching frequency f_{SW} = 300 kHz with V_{IN} = 12 V, V_{OUT1} = 1.2 V at up to 15 A and V_{OUT2} = 1.8 V at up to 15 A.

GENERAL DESCRIPTION

The ADP1823 is a versatile, dual output, interleaved, synchronous PWM buck controller that generates two independent outputs from an input voltage of 2.9 V to 20 V. It is ideal for a wide range of high power applications, such as DSP and processor core, general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. Each channel can be configured to provide output voltage from 0.6 V to 85% of the input voltage. The two channels operate 180° out of phase, which reduces the current stress on the input capacitor and allows the use of a smaller and lower cost input capacitor.

The ADP1823 operates at a pin-selectable fixed switching frequency of either 300 kHz or 600 kHz. For some noise sensitive applications, it can also be synchronized to an external clock to achieve switching frequency between 300 kHz and 1 MHz. The ADP1823 includes an adjustable soft start to limit input inrush current, voltage tracking for sequencing or DDR termination, independent power-good output, and a power enable pin. It also provides current-limit and short-circuit protection by sensing the voltage on the synchronous MOSFET.

The ADP1823 evaluation board schematic is shown in Figure 16. The switching frequency chosen is 300 kHz to get good efficiency over a wide range of input and output conditions. Table 2 shows the bill of materials of the evaluation board.

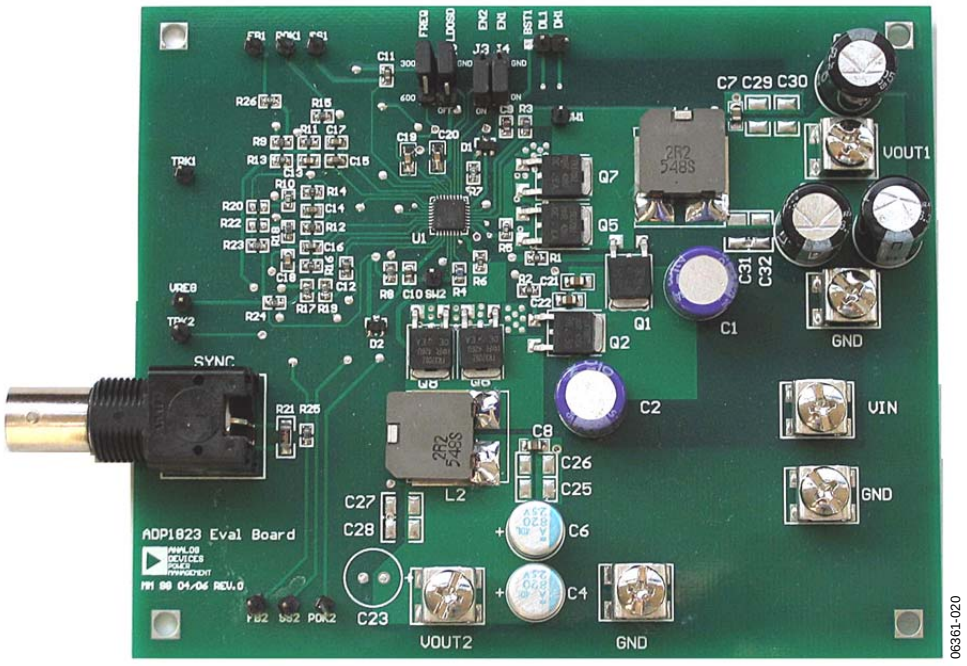

Figure 1. ADP1823 Evaluation Board

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

COMPONENT DESIGN

INPUT CAPACITOR

The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. Select the input bulk capacitor based on its ripple current rating. The two channels in ADP1823 operate 180° out of phase, thus reducing the current rating on the input capacitor.

If the maximum output load currents of Channel 1 and Channel 2 are about the same, the input ripple current is less than half of the higher of the output load currents. The input capacitor current is approximated as

$$Iin_{Ripple} \approx \frac{I_L}{2} \quad (1)$$

where I_L is the current though the inductor.

If the load currents of the two channels are significantly different (the smaller is less than 50% of the larger), in this case, if the duty cycle D is between 20% and 80%, the input capacitor ripple current is approximately $I_L\sqrt{D(1 - D)}$.

If duty cycle D is less than 20% or greater than 80%, the ripple current is approximately $0.4I_L$.

INDUCTOR SELECTION

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output voltage ripple and conduction losses in the MOSFETs, but allows using smaller inductors and less output capacitance for a specified peak-to-peak voltage overshoot at load transient. Generally, choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output current. Use the following equation to calculate the inductor value:

$$L = \frac{V_O(1 - D)}{\Delta I_L f_{SW}} \quad (2)$$

where:

L is the inductor value.
f_{SW} is the switching frequency.
V_O is the output voltage.
D is the duty cycle.
ΔI_L is the inductor ripple current, typically 1/3 of the dc load.

OUTPUT CAPACITOR SELECTION

Choose the output capacitor to set the desired output voltage ripple. The output voltage ripple is a function of the inductor ripple current and the capacitor impedance at the switching frequency. The output voltage ripple can be approximated as

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 f_{SW} C_{OUT}} \right) \quad (3)$$

For high ESR capacitors, the ripple is dominated by the ESR, while for low ESR capacitors, the output ripple is dominated by the capacitor. ESL of the capacitor also affects the output ripple, especially the though-hole electrolytic capacitors. In practical designs, multiple types of capacitors are used. For instance, a MLCC (multilayer ceramic capacitor) can be paralleled with an electrolytic capacitor to reduce the ESL and ESR.

Another factor that should be considered is the load-step transient response on the output, where the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. A minimum capacitance at the output is needed in order to have a fast load-step response and reasonable overshoot voltage. The minimum capacitance can be calculated as

$$C_{OUT,min1} = \frac{\Delta {I_O}^2 L}{2 V_O \Delta V_{up}} \quad (4)$$

$$C_{OUT,min2} = \frac{\Delta {I_O}^2 L}{2(V_{IN} - V_O) \Delta V_{down}} \quad (5)$$

where:

ΔI_O is the step load.
ΔV_{up} is the output voltage overshoot when the load is stepped down.
ΔV_{down} is the output voltage overshoot when the load is stepped up.
V_{IN} is the input voltage.
$C_{OUT,min1}$ is the minimum capacitance according to the overshoot voltage ΔV_{up}.
$C_{OUT,min2}$ is the minimum capacitance according to the overshoot voltage ΔV_{down}.

Select an output capacitance that is greater than both $C_{OUT, min1}$ and $C_{OUT, min2}$.

Make sure that the ripple current rating of the output capacitors is greater than the following current:

$$I_{COUT} = \sqrt{\frac{{\Delta I_L}^2}{12}} \quad (6)$$

MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance (R_{DSON}) to reduce the conduction loss, and low gate charge to reduce switching loss.

For the low-side (synchronous) MOSFET, the dominant loss is the conduction loss. It can be calculated as

$$P_{C,low} = (1 - D)\left(I_O{}^2 + \frac{\Delta I_L{}^2}{12}\right)R_{DSON} \quad (7)$$

The gate charge loss is dissipated by the ADP1823 regulator and gate drivers. The gate charge loss is approximated by the following equation:

$$P_G = V_G Q_G f_{SW} \quad (8)$$

where:

V_G is the driver voltage.
Q_G is the MOSFET total gate charge.

The high-side (main) MOSFET has to be able to handle two main power dissipations: conduction loss and switching loss. The switching loss is related to rise and fall times of the MOFSET, the switching frequency, the inductor current, and the input voltage. The high-side MOSFET switching loss is approximated by the equation

$$P_T = \frac{V_{IN} I_L (t_R + t_F) f_{SW}}{2} \quad (9)$$

where t_R and t_F are the rise and fall times of the MOSFET.

They can be calculated by

$$t_R = \frac{\frac{Q_{GS}}{2} + Q_{GD}}{\frac{V_G - V_{SP}}{R_G}}$$

and

$$t_F = \frac{\frac{Q_{GS}}{2} + Q_{GD}}{\frac{V_{SP}}{R_G}}$$

where:

Q_{GS} and Q_{GD} are the parameters of MOSFET, provided from the MOSFET data sheet.
R_G is the resistor on the driver.
V_{SP} is approximated using

$$V_{SP} \approx V_{TH} + \frac{I_O}{g_m}$$

where g_m is the MOSFET transconductance.

The high-side MOSFET conduction loss can be calculated as

$$P_{C,high} = D\left(I_O{}^2 + \frac{\Delta I_L{}^2}{12}\right)R_{DSON} \quad (10)$$

It is important to choose a high-side MOSFET that balances the conduction loss and the switching loss.

Make sure that the selection MOSFET can meet the total power dissipation when combining the switching and conduction loss (generally, about 1.5 W for a single D-PAK, 0.8 W for SO-8, and 1.2 W for PowerPak-SO8).

SOFT START

The ADP1823 uses an adjustable soft start to limit the output voltage ramp-up period, thus limiting the input inrush current. The soft start is set by selecting the capacitor, C_{SS}, from SS1 and SS2 to GND. The ADP1823 charges C_{SS} to 0.8 V through an internal 90 kΩ resistor. The voltage on the soft start capacitor while it is charging is

$$V_{CSS} = 0.8\left(1 - e^{-\frac{t_{SS}}{RC_{SS}}}\right)$$

The soft start period ends when the voltage on the soft start pin reaches 0.6 V.

$$C_{SS} = \frac{t_{SS}}{-R\ln\left(1 - \frac{0.6}{0.8}\right)}$$

where R = 90 kΩ and t_{ss} is the soft start time.

Therefore,

$$C_{SS} = 8.015 t_{SS} \times 10^{-6}\ \text{F} \quad (11)$$

CURRENT LIMIT

The ADP1823 employs a unique, programmable cycle-by-cycle lossless current-limit circuit. In every switching cycle, the voltage drop across the synchronous MOSFET R_{DSON} is measured to determine if the current is too high.

This measurement is done by an internal comparator and an external resistor. The CSL1 and CSL2 pins are the inverting inputs of the current-limit comparators and the noninverting inputs are referenced to PGND1 and PGND2, respectively. A resistor is tied between the CSL pin and the switch node, which is the drain of the synchronous MOSFET. A 50 µA current is forced though the resistor to set an offset voltage drop across it. When the synchronous MOSFET is on and the voltage drop on it exceeds the offset voltage on the external resistor, an overcurrent fault is flagged.

When the ADP1823 senses an overcurrent condition, the next switching cycle is suppressed, and the soft start capacitor is discharged. The ADP1823 remains in this mode as long as the overcurrent condition persists. When the overcurrent condition is removed, operation resumes in soft start mode.

The external current-limit resistor can be calculated by the following equation:

$$R_{CLS} = \frac{\left(I_{limit} + \frac{\Delta I_L}{2}\right) R_{DSON}}{50\,\mu A} \quad (12)$$

where I_{limit} is the limit current.

VOLTAGE TRACKING

The ADP1823 features tracking inputs, TRK1 and TRK2, which make the output voltage track another voltage. This is especially useful in core and I/O voltage sequencing applications.

The ADP1823 tracking input is an additional positive input to the error amplifier. The feedback voltage is regulated to the lower of the 0.6 V reference or the voltage at TRK, so a lower voltage on TRK limits the output voltage. This feature allows implementation of two different types of tracking: coincident tracking, where the output voltage is the same as the master voltage until the master voltage reaches regulation, and ratiometric tracking, where the output voltage is limited to a fraction of the master voltage. In all tracking configurations, the master voltage should be higher than the slave voltage.

Note that the soft start time of the master voltage should be set to be longer than the soft start of the slave voltage. That forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start of the slave voltage is longer, the slave will come up more slowly and the tracking relationship will not be seen at the output. The slave channel should still have a soft start capacitor to give a small but reasonable soft start time to protect in case of restart after a current-limit event. For more information about the voltage tracking, see the ADP1823 data sheet.

COMPENSATION DESIGN

Figure 2 shows the voltage mode control loop for a synchronous buck converter. Usually, design the compensator to get adequate phase margin and high cross frequency for stable operation and good transient response. There are two types of compensation circuits for the ADP1823, Type II and Type III. For more details, see the *Compensating the Voltage Mode Buck Regulator* section in the ADP1823 data sheet.

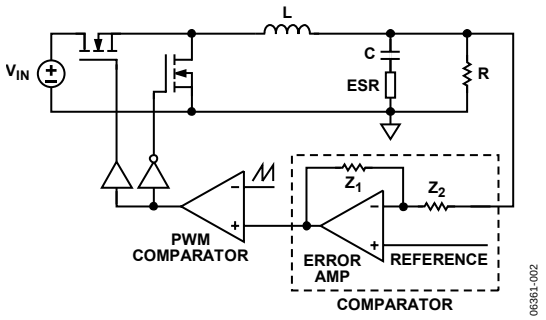

Figure 2. Voltage Mode Buck Converter

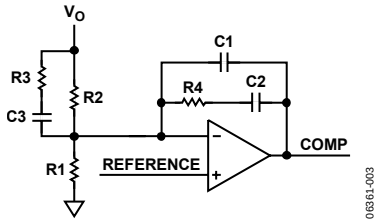

Figure 3. Type III Compensation Circuit

The buck converter control to output transfer function can be described by the following equation:

$$G_{VD}(s) = \frac{V_O(s)}{d(s)} = \frac{V_{IN}}{1 + \frac{1}{R}} \cdot \frac{1 + \frac{s}{2\pi f_Z}}{1 + \frac{s}{Q2\pi f_O} + \frac{s^2}{(2\pi f_O)^2}} \quad (13)$$

where:

$$f_Z = \frac{1}{2\pi R_C C}$$

$$f_O = \frac{\sqrt{\frac{R}{R + R_C}}}{2\pi\sqrt{LC}}$$

$$Q = \frac{1 + R}{L + R\,R_C C} \cdot \frac{1}{2\,\pi f_O}$$

R_C is the ESR of the output capacitor.

The compensation network consists of the error amplifier and the impedance networks Z1 and Z2. Figure 3 shows a Type III compensation circuit. It provides two poles and two zeros. The transfer function of this compensator is

$$G_{EA}(s) = \frac{-A_{EA}}{s} \cdot \frac{\left(1 + \frac{s}{2\pi f_{Z1}}\right) \cdot \left(1 + \frac{2}{2\pi f_{Z2}}\right)}{\left(1 + \frac{s}{2\pi f_{P1}}\right) \cdot \left(1 + \frac{s}{2\pi f_{P2}}\right)} \quad (14)$$

where:

$$A_{EA} = \frac{1}{(C_1 + C_2) \cdot R_2}$$

$$f_{Z1} = \frac{1}{2\pi R_4 C_2}$$

$$f_{Z2} = \frac{1}{2\pi (R_2 + R_3) \cdot C_3}$$

$$f_{P1} = \frac{1}{2\pi R_3 C_3}$$

$$f_{P2} = \frac{1}{2\pi R_4 \cdot \frac{C_1 C_2}{C_1 + C_2}}$$

The loop gain can be written as

$$T(s) = \frac{G_{VD}(s) \cdot G_{EA}(s)}{V_{Ramp}} \quad (15)$$

where V_{Ramp} is the PWM ramp peak voltage; in ADP1823, V_{Ramp} = 1.3 V.

Use the following guidelines to select the compensation components:

1. Set the loop gain cross frequency f_C. A good choice is to place the cross frequency f_C at $f_S/10$ for fast response.
2. Cancel ESR zero f_Z by compensator pole f_{P1}.
3. Place the high frequency pole f_{P2} to achieve maximum attenuation of switching ripple and high frequency noise. A good choice is f_{P2} = (5 ~ 10) f_C.
4. Place two compensator zeros nearby at the power stage resonant frequency f_O. Usually, place f_{Z1} below f_O and place f_{Z2} between f_O and f_C.
5. Check the phase margin to get the good regulation performance.

TEST RESULTS

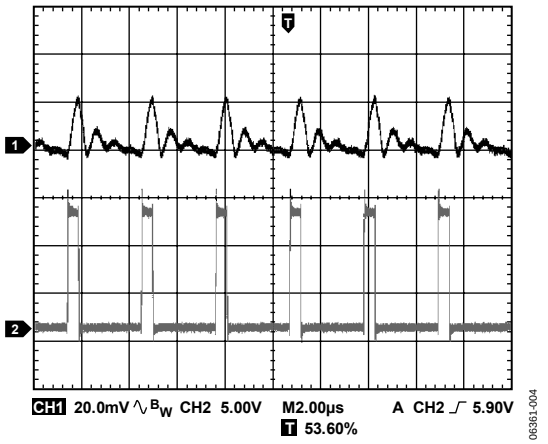

Figure 4. Output Ripple of Channel 1, V_{OUT} = 1.8 V, f_{SW} = 300 kHz, Channel 1: V_{OUT1}, Channel 2: SW1

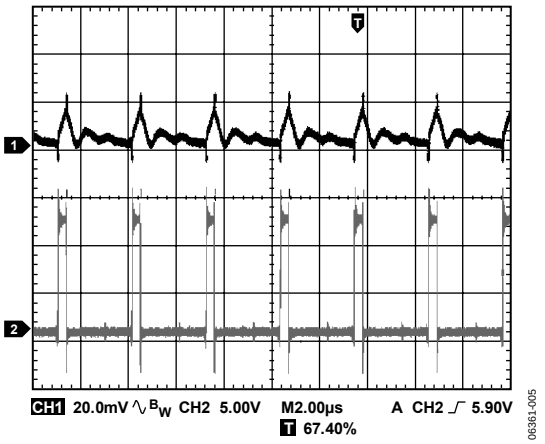

Figure 7. Output Ripple of Channel 2, V_{OUT} = 1.2 V, f_{SW} = 300 kHz, Channel 1: V_{OUT2}, Channel 2: SW2

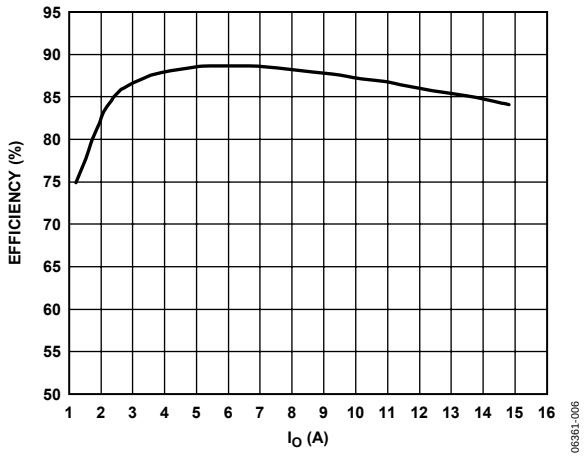

Figure 5. Efficiency vs. Load Current, V_{OUT} = 1.8 V, f_{SW} = 300 kHz

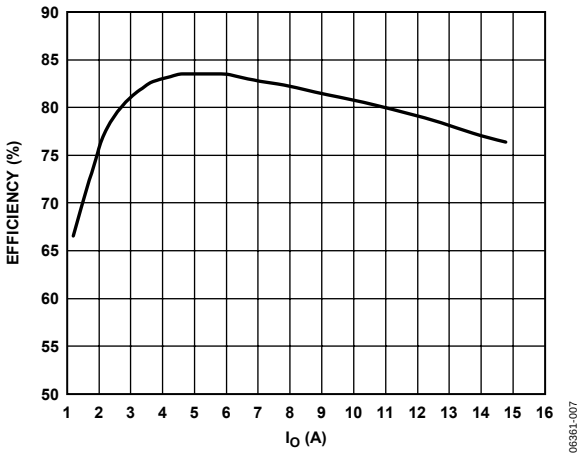

Figure 8. Efficiency vs. Load Current, V_{OUT} = 1.2 V, f_{SW} = 300 kHz

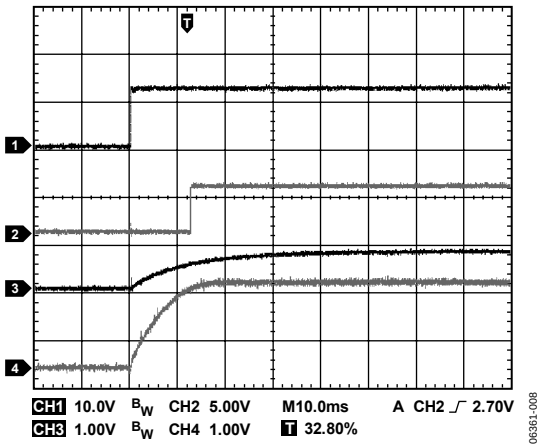

Figure 6. Soft Start of Channel 1, Channel 1: EN1, Channel 2: PG1, Channel 3: SS1, Channel 4: V_{OUT1}

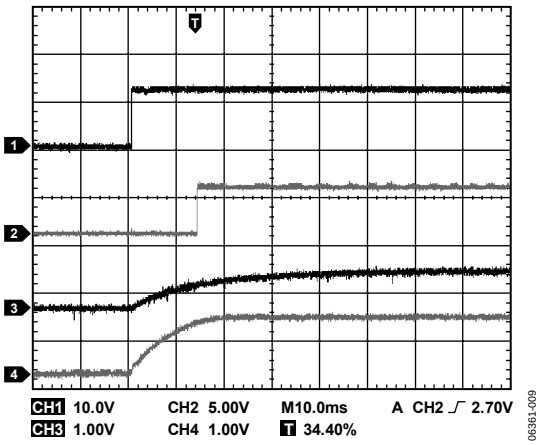

Figure 9. Soft Start of Channel 2, Channel 1: EN2, Channel 2: PG2, Channel 3: SS2, Channel 4: V_{OUT2}

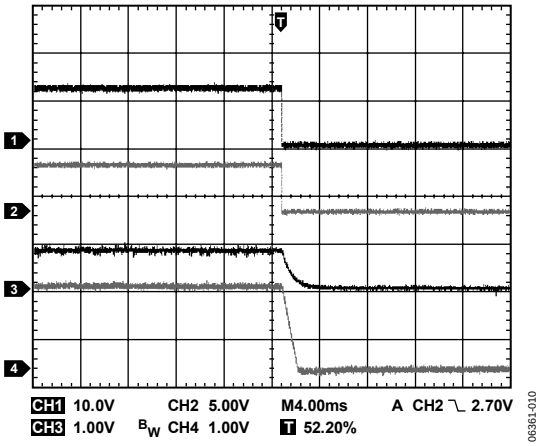

Figure 10. Disable Channel 1,
Channel 1: EN1, Channel 2: PG1, Channel 3: SS1, Channel 4: V_{OUT1}

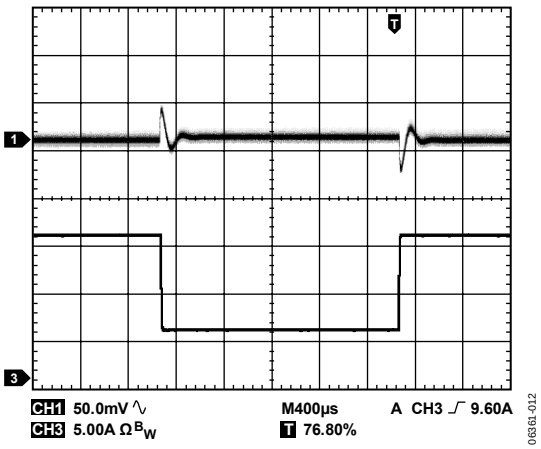

Figure 11. Load Transient Response of Channel 1,
5 A to 15 A , V_{IN} = 12 V, V_O = 1.8 V

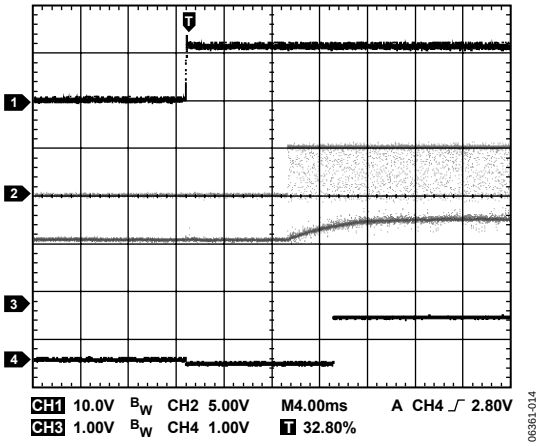

Figure 12. Precharge Start of Channel 1,
Channel 1: V_{IN}, Channel 2: Low-Side Gate, Channel 3: V_{OUT}, Channel 4: POK

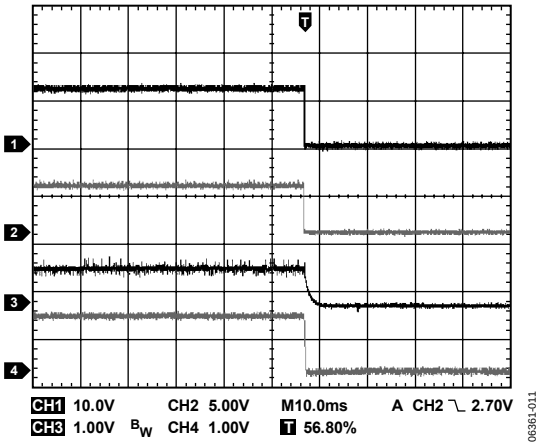

Figure 13. Disable Channel 2,
Channel 1: EN2, Channel 2: PG2, Channel 3: SS2, Channel 4: V_{OUT2}

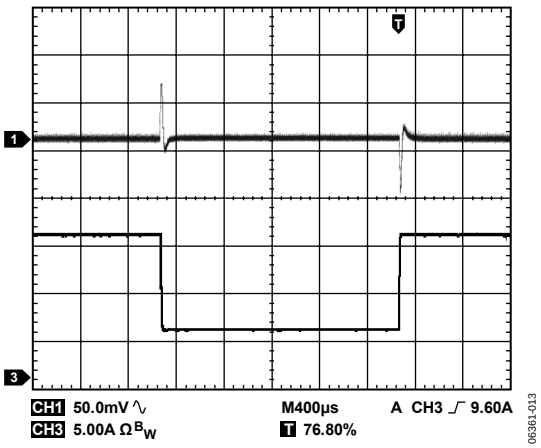

Figure 14. Load Transient Response of Channel 2,
5 A to 15 A, V_{IN} = 12 V, V_O = 1.2 V

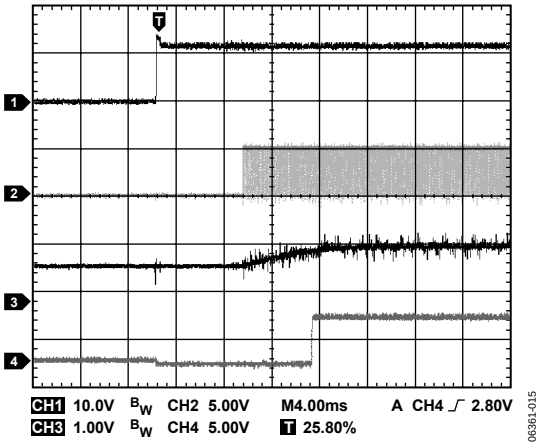

Figure 15. Precharge Start of Channel 2
Channel 1: V_{IN}, Channel 2: Low-Side Gate, Channel 3: V_{OUT}, Channel 4: POK

PCB LAYOUT GUIDELINES

In any switching converter, some circuit paths carry high dI/dt, which can create spikes and noise. Other circuit paths are sensitive to noise. Still others carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and copper area accordingly.

The following is a list of recommended layout practices for ADP1823, arranged in approximately decreasing order of importance:

1. Keep the high current loops small. While the inductor is considered to have continuous high current, this current is switched alternately through the top and bottom FETs. The current waveform in each FET is a pulse with very high dI/dt, so the path to, through, and from each individual FET should be as short as possible and the two paths should be commoned as much as possible. In designs that use a pair of D-Pak or SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair and the high-side drain can be bypassed to the low-side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs in order to minimize inductance around this loop through the FETs and capacitor.

   In designs that place the two FETs on opposite sides of the board, it may work well to place one FET directly opposite to (above and below) the other so as to form a minimal current loop area. Again, make sure that the high-side drain is bypassed to the low-side source with a suitable ceramic bypass capacitor, connected as closely as possible to the FETs to minimize the loop area.

   Recommended ceramic capacitor values range from 4.7 µF to 22 µF depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor.

2. GND, IN bypass, V_{REG} bypass, soft start capacitors, and the bottom ends of the output feedback divider resistors should be tied to an (almost isolated) small ground plane under the IC. No high current or high dI/dt signals should be connected to this ground plane. One via should connect GND to the die paddle heat sink area. The AGND and PGND planes should be separated before joining together. Other low current signal grounds can also be connected here if a ground connection is needed; these may include SYNC, FREQ, or LDOSD. This ground area should be connected through one wide trace to the negative terminal of the output filter capacitors. Because the ADP1823 is a dual output controller, it is desirable to place the output filters of the two output voltages adjacent to each other. This provides the best accuracy for the two outputs.

3. PGND pins handle high dI/dt gate drive current returning from the source of the low-side MOSFET. The voltage at this pin also establishes the 0 V reference for the OCP function and the CSL pins. A small PGND plane should connect the PGND pins and the PV bypass capacitors through a wide and direct path to the source of the appropriate low-side MOSFET.

4. Gate drive traces (DH and DL) handle high dI/dt so tend to produce noise and ringing. They should be as short and direct as possible. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. For this reason, it is occasionally helpful to place small value resistors (such as 10 Ω) in series with the gate traces. These can be populated with 0 Ω if resistance is not needed.

5. The switch node is the interconnection of the source of the high-side FET with the drain of the low-side FET and the inductor. This is the noisiest place in the switcher circuit with large ac and dc voltage and current. This node should be wide to keep resistive voltage drop down. However, to minimize the generation of capacitively coupled noise, the total area should be small. The best layout will generally place the FETs and inductor all close together on a small copper plane in order to minimize series resistance and keep the copper area small.

   Connect a direct and moderately sized trace from the switch node back to the SW pin and the CSL resistor. This trace will handle the high dI/dt gate current for the high-side FET. The voltage on this trace is also sensed through the CSL resistors and pins to sense an overcurrent condition. The high dI/dt and sensing overcurrent do not occur at the same time.

   Keep the compensation and feedback components away from the switch nodes and their associated components.

6. The negative terminal of the output filter capacitors should be tied closely to the source of the low-side FET. Doing this helps minimize voltage differences between GND and PGND at the ADP1823. The current in these capacitors is not very high in a buck converter, but the output trace will handle the full output current of the converter. High dc current flows through this trace to the input filter capacitors, so it is generally helpful to place a bulk input filter capacitor close to the output filter capacitors on this output ground plane. The GND connection of the ADP1823 should be connected to this output ground at the output filter capacitors.
7. Generally, be sure that all traces are sized according to the current that will be handled as well as their sensitivity in the circuit. Standard PCB layout guidelines mainly address heating effects of current in a copper conductor. While these are completely valid, they do not fully cover other concerns such as stray inductance or dc voltage drop. Any dc voltage differential in connections between ADP1823 GND and the converter power output ground can cause a significant output voltage error, as it affects converter output voltage according to the ratio with the 600 mV feedback reference. For example, a 6 mV offset between ground on the ADP1823 and the converter power output will cause a 1% error in the converter output voltage.
8. The CSP package has an exposed die paddle on the bottom that efficiently conducts heat to the PCB. Adding thermal vias to the PCB provides a thermal path to the inner or bottom layers. Note that the thermal pad is attached to the die substrate, so the planes that the thermal pad is connected to must be electrically isolated or connected to GND.

EVALUATION BOARD SCHEMATIC AND LAYOUT

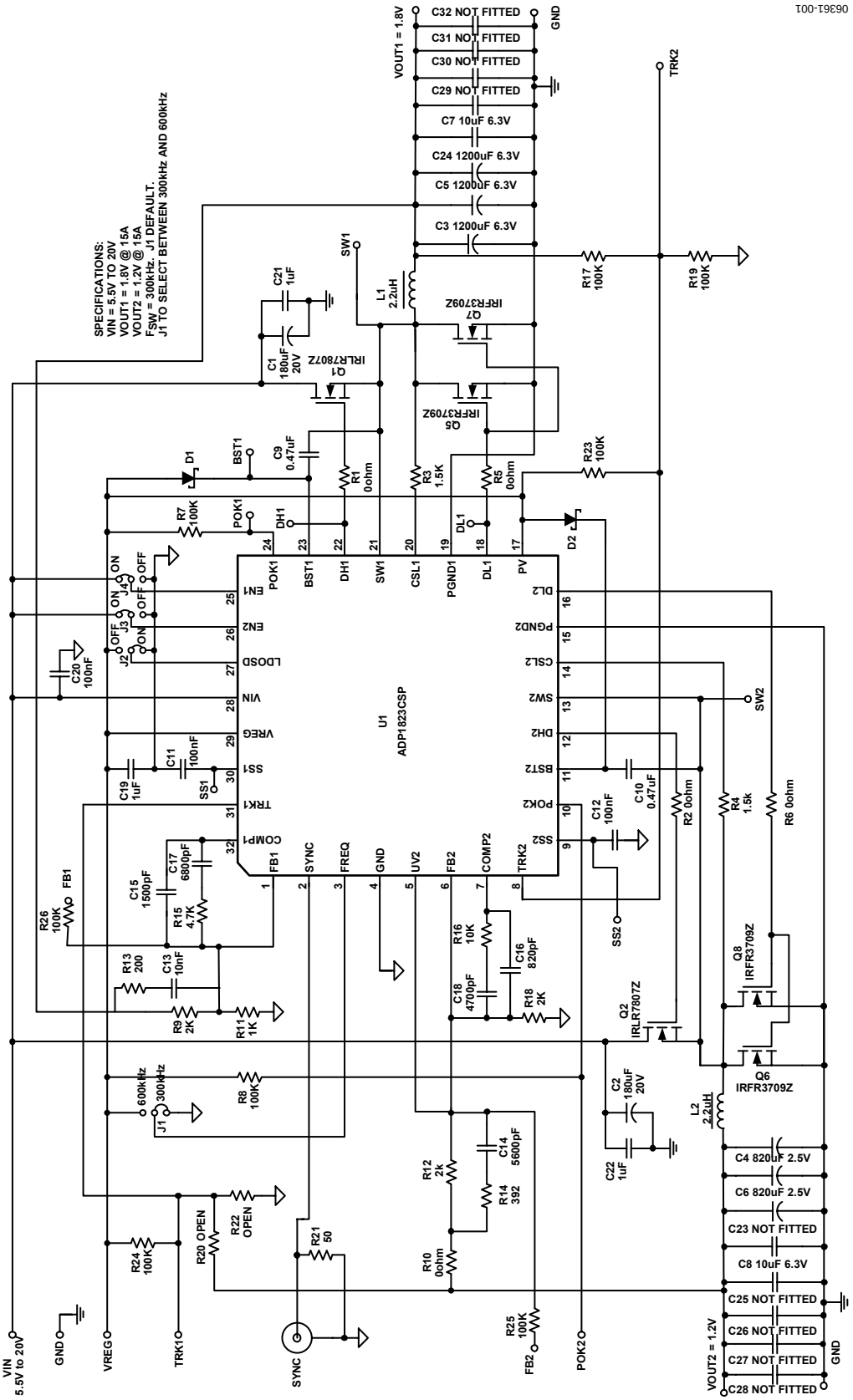

Figure 16. ADP1823 Evaluation Board Schematic, f_{SW} = 300 kHz

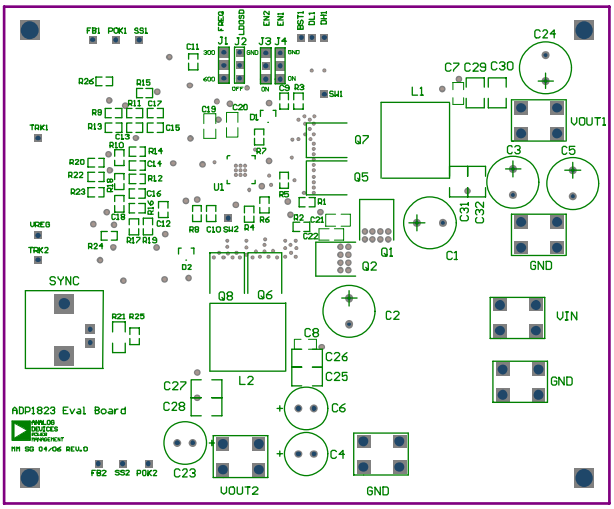

Figure 17. Silk Screen Layer

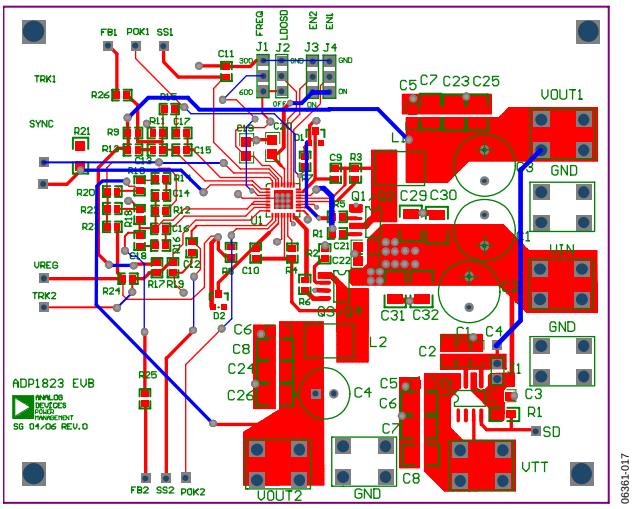

Figure 19. Top and Bottom Layers

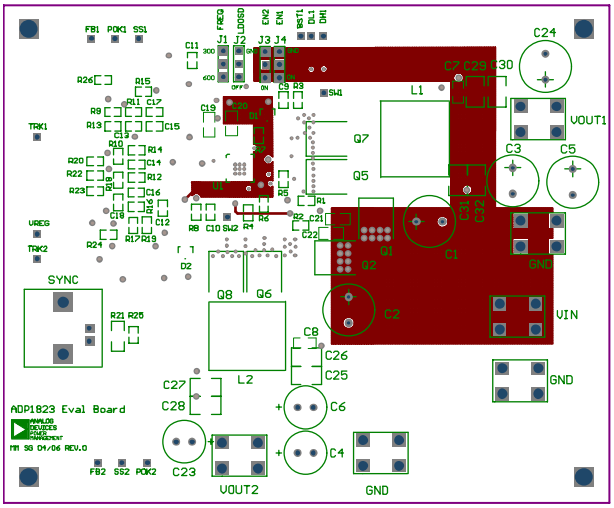

Figure 18. Inner Layer 1

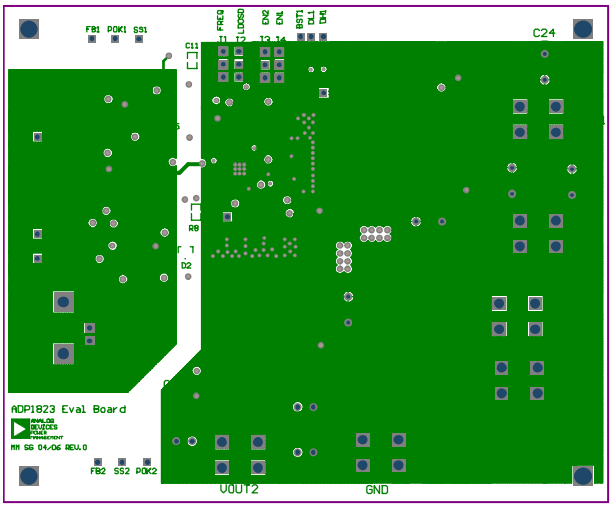

Figure 20. Inner Layer 2

Table 1. Jumper Description

Jumper	Description	Function
J1	Frequency Selection	VREG: f_{SW} = 600 kHz GND: f_{SW} = 300 kHz
J2	LDO Shunt Down or Enable	VREG: LDO shunt down GND: LDO enable
J3	Channel 1 Enable or Disable	VIN: Channel 1 enable GND: Channel 1 disable
J4	Channel 2 Enable or Disable	VIN: Channel 2 enable GND: Channel 2 disable

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Item	Description	Manufacturer	Part No.	Designator	Qty.
1	Capacitor, OS-CON, 180 µF, 20 V	Sanyo	20SP180M	C1, C2	2
2	Capacitor, Polymer Aluminum, 820 µF, 2.5 V	United Chemi-con	APSA2R5ELL821MHB5S Mouser: 661-PSA2.5VB820M	C4, C6	2
3	Capacitor, Aluminum Electrolytic, 1200 µF, 6.3 V	Rubycon	6.3 ZLG1200M 10×16	C3, C5, C24	3
4	Capacitor, Ceramic, 10 µF, 6.3 V, X5R, 0805	Murata	GRM21BR60J106K	C7, C8	2
5	Capacitor, Ceramic, 0.47 µF, 10 V, X5R, 0603	Taiyo Yuden Murata	LMK107BJ474MA-T GRM188R61A474KA61	C9, C10	2
6	Capacitor, Ceramic, 0.1 µF, 10V, X7R, 0603	Vishay	VJ0603Y104MXQ	C11, C12	2
7	Capacitor, Ceramic, 10 nF, 50 V, NPO, 0603	Vishay	VJ0603Y123KXXA	C13	1
8	Capacitor, Ceramic, 5600 pF, 50 V, NPO, 0603	Vishay	VJ0603Y562 KXXA	C14	1
9	Capacitor, Ceramic, 1500 pF, 50 V, NPO, 0603	Vishay	VJ0603Y152 KXXA	C15	1
10	Capacitor, Ceramic, 820 pF, 50 V, NPO, 0603	Vishay	VJ0603Y821 KXXA	C16	1
11	Capacitor, Ceramic, 6800 pF, 10 V, NPO, 0603	Vishay	VJ0603Y822 KXXA	C17	1
12	Capacitor, Ceramic, 4700 pF, 10 V, NPO, 0603	Vishay	VJ0603Y472 KXXA	C18	1
13	Capacitor, Ceramic, 1.0 µF, 10 V, X5R, 0603	Taiyo Yuden Murata	LMK107BJ105MK-T GRM185R61A105KE36	C19	1
14	Capacitor, Ceramic, 0.1 µF, 50 V, Y5V, 0603	Taiyo Yuden	UMK107F104ZA-T	C20	1
15	Capacitor, Ceramic, 1.0 µF, 25 V, X5R, 0805	Taiyo Yuden Murata	TMK212BJ105KG-T GRM21BR61E105KA99	C21, C22	2
16	Capacitor, Ceramic		Not used	C25, C26, C27, C28, C29, C30, C31, C32	8
17	Resistor, 0 Ω, 1/10 W, 1%, 0603	Vishay	CRCW06030R00F	R1, R2, R5, R6, R10	5
18	Resistor, 1.5 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031501F	R3, R4	2
19	Resistor, 100 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031003F	R7, R8, R17, R19, R23, R24, R25, R26	8
20	Resistor, 2.0 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06032001F	R9, R12, R18	3
21	Resistor, 1.0 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031001F	R11	1
22	Resistor, 100 kΩ, 1/10 W, 1%, 0603		Not used	R20, R22	2
23	Resistor, 4.75 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06034751F	R15	1
24	Resistor, 10 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031002F	R16	1
25	Resistor, 200 Ω, 1/10 W, 1%, 0603	Vishay	CRCW06032000F	R13	1
26	Resistor, 392 Ω, 1/10 W, 1%, 0603	Vishay	CRCW06032920F	R14	1
27	Resistor, 49.9 Ω, 1/4 W, 1%, 1206	Vishay	CRCW120649R9F	R21	1
28	Inductor, 2.2 µH, 15 A, 4.5 mΩ DCR	Toko	FDA1254-2R2M=P3	L1, L2	2
29	Diode, Switching, 250 mA, 75 V, SOT-23	Central Semi	CMPD4448	D1, D2	2
30	Transistor, N MOSFET, 30 A, D-Pak, 18 mΩ	IR	IRLR7807Z	Q1, Q2	2
31	Transistor, N MOSFET, 60 A, D-Pak, 8 mΩ	IR	IRFR3709Z	Q5, Q6, Q7, Q8	4
32	IC, Dual Interleaved Step-Down Controller with Tracking	Analog Devices	ADP1823	U1	1
33	Jumper, 0.1″ Spacing	Any		J1, J2, J3, J4	4
34	Test Points	Any		VREG, TRK1, TRK2, POK1, POK2, FB1, FB2, SS1, SS2, BST1, SW1, SW2, DH1, DL1	14
35	Terminal			VIN, GND, VOUT1, GND, VOUT2, GND	6
36	BNC			SYNC	1

ORDERING GUIDE

Model	Package Description
ADP1823-EVAL	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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