Embedded ACPI Compliant DDR Power Generation Using the ISL6532A

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Introduction

The ISL6532A provides a complete ACPI compliant power solution for dual channel DDRI and DDRII Memory systems. Included are both a synchronous buck controller and integrated LDO to supply VDDQ with high current during S0/S1 (Run) states and standby current during S3 (Suspend-To-RAM = STR) state. During Run mode, a fully integrated sink-source regulator generates an accurate (VDDQ/2) high current VTT voltage. A buffered version of the VDDQ/2 reference is provided as V_{REF}. The ISL6532A also features VDDQ overcurrent protection and an internal LDO controller for production of 1.5V Video and Core Voltages.

The ISL6532A contains high performance error amplifiers, a high accuracy reference, an internal 50% tracking reference, a fixed 250kHz internal oscillator, overcurrent protection for the VDDQ regulator utilizing the control MOSFET $r_{DS(ON)}$ and Power Good indication. All these features are packaged in a 28-Lead 6x6mm QFN. A more complete description of the IC can be found in the datasheet[1].

Reference Design

The ISL6532AEVAL1 is an evaluation board that highlights the operation of the ISL6532A in an embedded DDR DRAM Memory Power application. The V_{DDQ} supply has been designed to supply 2.5V at a maximum load of 20A. The V_{TT} termination supply will track the V_{DDQ} supply at 50% while sourcing or sinking current. The LDO is designed to supply 1.5V AGP core voltage. The schematic, Bill of Materials, and Board Layout for the ISL6532AEVAL1 can be found in the Appendix.

Quick Start Evaluation

The ISL6532AEVAL1 board is shipped ‘ready to use’ right from the box. The ISL6532AEVAL1 supports testing with standard laboratory equipment or with an ATX power supply. All three outputs can be exercised through external loads. Both the V_{DDQ} and V_{TT} regulators have the ability to source or sink current while the AGP Linear regulator may only source current.

There are auxiliary posts available on the board for introducing power to the board if an ATX supply is not available. If an ATX supply is used, these posts may be used to monitor the voltages supplied by the ATX supply. There are also posts available on each regulated output rail for drawing a load and/or monitoring the voltages. Ten individually labeled probe points are also available for use. These probe points provide Kelvin connections to signals which may be of interest to the designer.

Three switches have been placed on the board to accommodate ACPI signal simulation. The ATX switch will enable or disable the ATX power supply, while the other two switches will send S5 or S3 signals to the ISL6532A.

Recommended Test Equipment

To test the full functionality of the ISL6532A, the following equipment is recommended:

- An ATX power supply (minimum 160W configuration)
- Three electronic loads
- Four channel oscilloscope with probes
- Precision digital multimeters

If individual power supplies are to be utilized in place of the ATX power supply, then the 5V power supply should be capable of producing 15A of continuous current. The supply for the 5VSBY rail should be capable of producing up to 1A. A single 5V supply may be used for both VCC5 and 5VSBY. The 12V supply should be capable of producing at least 1A of continuous current.

Power and Load Connections

Input Voltages

Simply plug the 20 pin connector from the ATX power supply into the 20 pin receptacle, J1, on the evaluation board. If laboratory supplies are to be used, then connect the 5V supplies to the VCC5 and 5VSBY posts. Connect the 12V supply to the 12V post. Connect the ground leads of all supplies to the corresponding GND post directly to the left of each supply post.

Loading V_{DDQ}

Connect the positive terminal of the first electronic load to the VDDQ post. Connect the return terminal of the same load to the corresponding GND post.

Loading V_{TT} - Sourcing Current

To test V_{TT} while the regulator sources current, connect the positive terminal of the second electronic load to the VTT post. Connect the return terminal of the same load to the corresponding GND post.

Loading V_{TT} - Sinking Current

To test V_{TT} while the regulator sinks current, connect the positive terminal of the second electronic load to the VDDQ post. Connect the return terminal of the same load to the VTT post.

CAUTION: The return terminal of the load must float for this to work properly.

Loading V_{AGP}

Connect the positive terminal of the third electronic load to the 1.5VAGP post. Connect the return terminal of the corresponding GND post.

Standby 3.3V Generation

The ISL6532AEVAL1 has been designed to generate a 3.3VSBY rail from the 5VSBY input. The 3.3VSBY rail is used as the input to the standby LDO when the system is in the Sleep State.

Power Up and State Transitions

There are several distinct state transitions that the ISL6532A supports. These include a Cold/Mechanical Start (S5 to S0 state transition), Active to Sleep (S0 to S3 transition), Sleep to Active (S3 to S0 transition) and finally Active to Shutdown (S0 to S5 transition). Table 1 shows the switch positions and the corresponding ACPI states.

TABLE 1. ISL6532AEVAL1 STATES

ATX	S3	S5	STATE
ON	Active	Active	Active (S0)
ON	S3	Active	Sleep (S3)
ON	Active	S5	Shutdown (S5)

If the ATX switch toggled to OFF while the system is in either Active of Sleep state, the ISL6532A will revert to an S3 (Sleep) state. When either the S3 or S5 switch is toggled from ACTIVE to the corresponding sleep state, there is circuitry on the evaluation board that will force the ATX supply OFF

Initial Power Up - Cold Start

There are two ways to initiate a Cold Start on the ISL6532AEVAL1. Prior to applying power to the ATX supply, the S5 and S3 switch toggles should be pointing to “ACTIVE” while the ATX switch toggle is pointing to “OFF”. After applying power to the ATX supply, the ISL6532A can be Cold Started be engaging the ATX switch to “ON”. The second method requires the system to be in Shutdown state, with the ATX switch “ON”, the S3 switch “ACTIVE” and the S5 switch in “S5”. After engaging the S5 switch to “ACTIVE”, the system will Cold Start. Figure 1 shows a Cold Start.

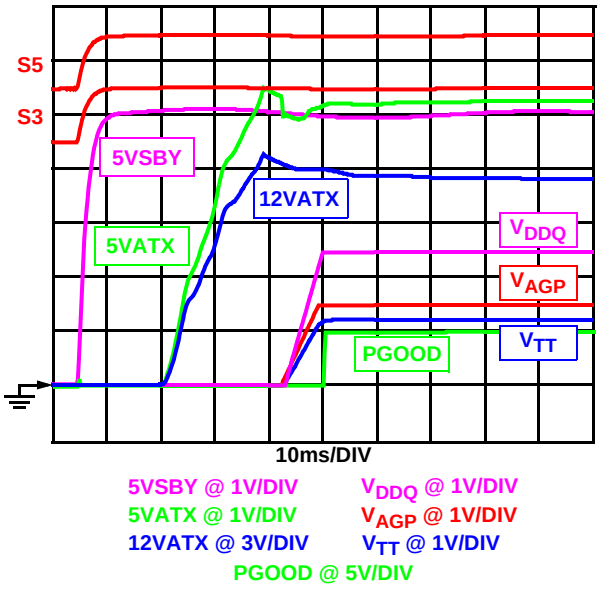


FIGURE 1. COLD/MECHANICAL START

Active to Sleep State Transition

Figure 2 shows the transition from Active to Sleep. Refer to Table 1 for proper switch positions to achieve this state transition. When transitioning from Active State to Sleep State, it is important that the load on the V_{DDQ} rail be reduced to levels that the standby LDO is capable of supporting. If the load on V_{DDQ} is excessive, V_{DDQ} voltage will collapse.

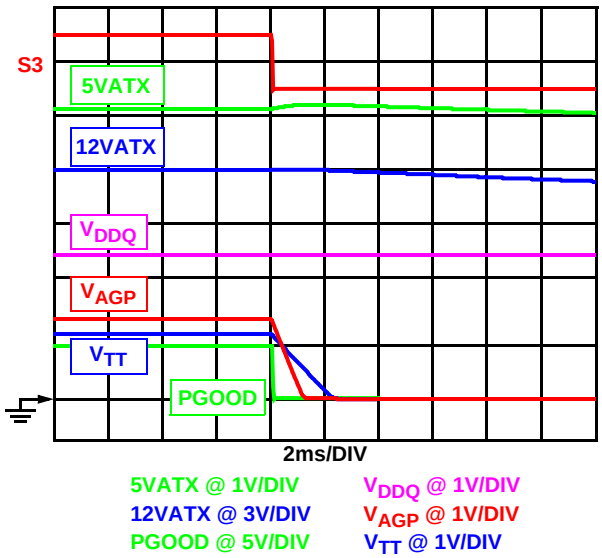


FIGURE 2. ACTIVE TO SLEEP TRANSITION

Sleep to Active State Transition

Figure 3 shows the transition from Sleep to Active State. Refer to Table 1 for proper switch positions to achieve this state transition. Once the PGOOD signal has been asserted, the V_{DDQ} rail can then be loaded beyond the S3 load limitations of the standby LDO.

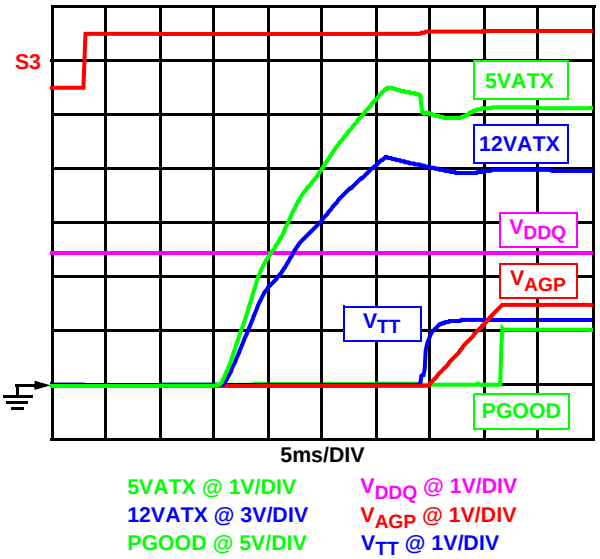


FIGURE 3. SLEEP TO ACTIVE TRANSITION

Shutdown to Active State Transition

Figure 4 shows the transition from Shutdown to Active. Refer to Table 1 for proper switch positions to achieve this state transition.

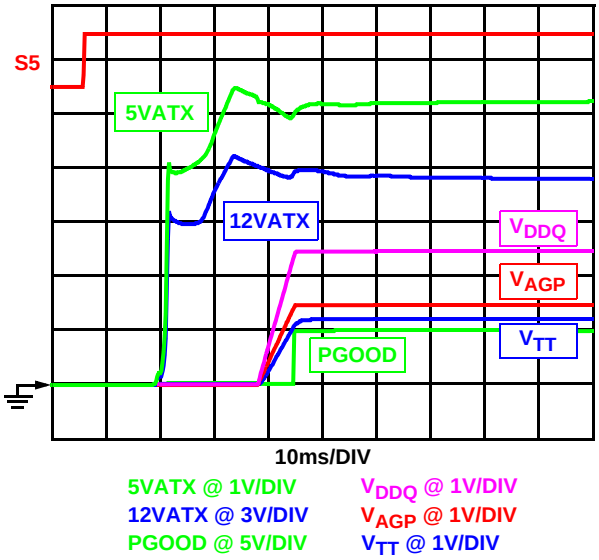


FIGURE 4. SHUTDOWN TO ACTIVE TRANSITION

V_{DDQ} Ripple Voltage

Figure 5 shows the ripple voltage on the V_{DDQ} output.

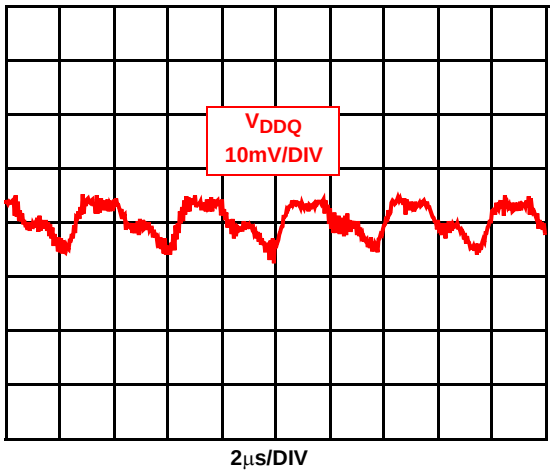


FIGURE 5. V_{DDQ} RIPPLE VOLTAGE

Transient Performance

Figures 6 through 10 show the response of the outputs when subjected to a variety of transient loads while in the Active (S0) State. Figure 6 shows V_{DDQ} under transient loading. Figure 7 shows V_{TT} under a transient loading that causes V_{TT} to source current. Figure 8 shows V_{TT} under a transient that causes V_{TT} to sink current. Figure 9 shows both V_{DDQ} and V_{TT} under simultaneous transient loading. Finally, Figure 10 shows the 1.5V AGP rail under transient loading.

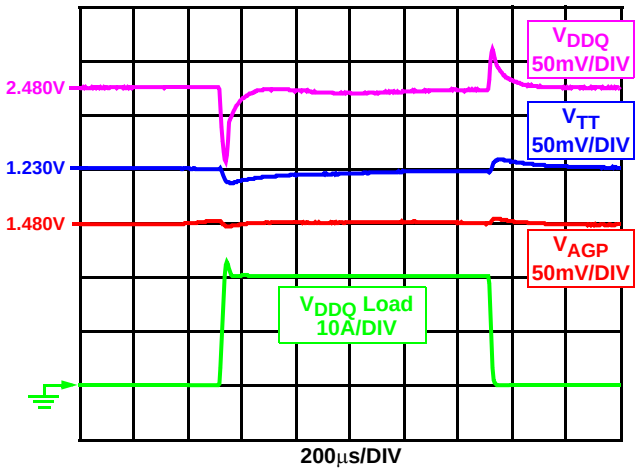


FIGURE 6. TRANSIENT ON V_{DDQ}

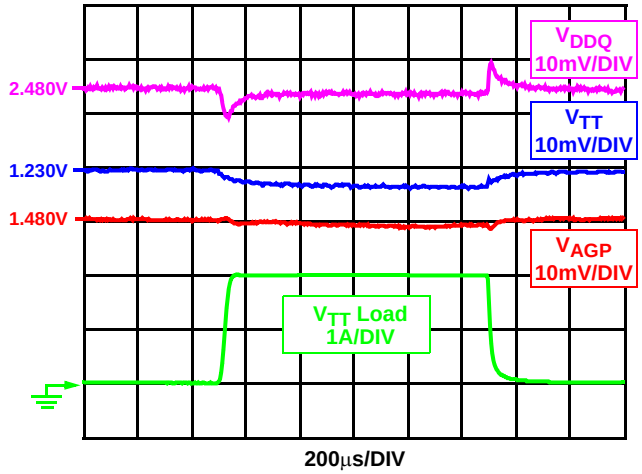


FIGURE 7. SOURCING TRANSIENT ON V_{TT}

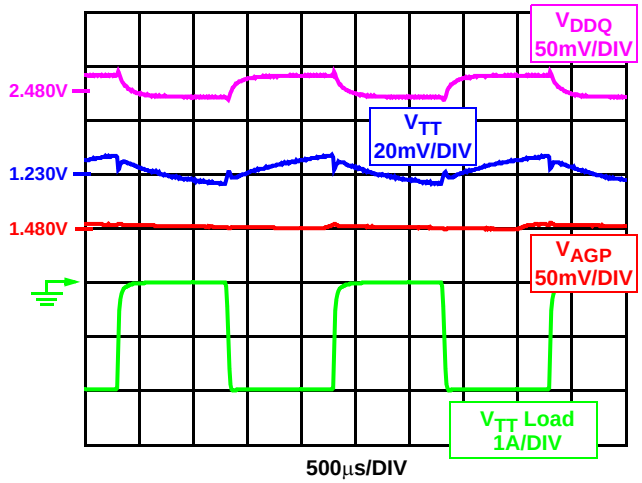


FIGURE 8. SINKING TRANSIENT ON V_{TT}

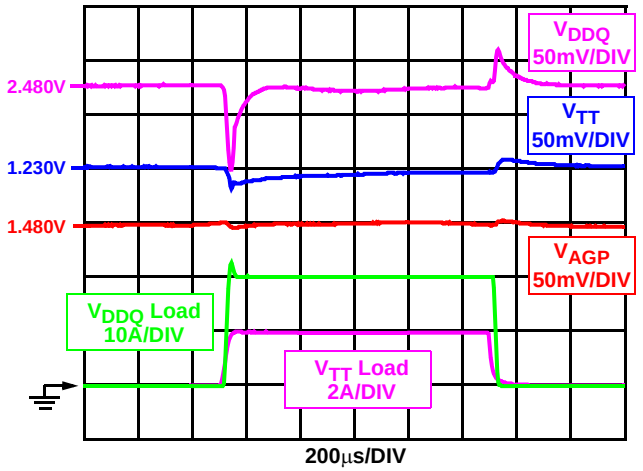


FIGURE 9. SOURCING TRANSIENTS ON V_{DDQ} AND V_{TT}

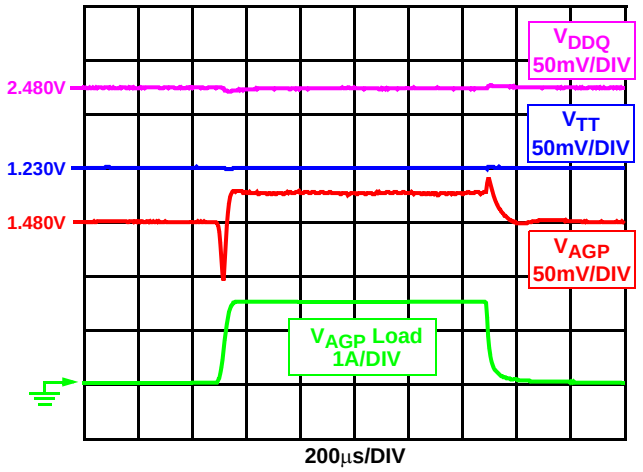


FIGURE 10. TRANSIENTS ON 1.5V AGP RAIL

Efficiency

Figure 11 shows the efficiency of the VDDQ regulator while in Active (S0) State. As the other regulated outputs are all derived through linear regulation, their efficiencies are not shown.

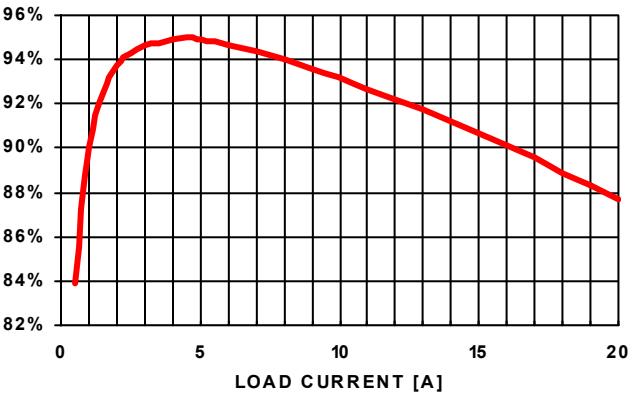


FIGURE 11. V_{DDQ} EFFICIENCY

ISL6532AEVAL1 Customization

There are numerous ways in which a designer might modify the ISL6532AEVAL1 evaluation board for differing requirements. Some of the changes which are possible include:

- The input and output inductors, L1 and L2
- The input and output capacitance for any of the three regulators.
- The overcurrent trip point, programmed through the OCSET resistor, R7
- By changing the value of C19, the soft start profile of the V_{TT} rail, when transitioning from Sleep to Active State
- All MOSFET footprints on the evaluation board allow for either SO8 or PowerPak packaged MOSFETs to be utilized
- The 3.3VSBY LDO, Ux1, may be circumvented by shorting pins 2 and 3 together. This will provide the V_{DDQ} standby LDO with 5V while in Sleep state, which allows the load to be increased by 100mA.

Conclusion

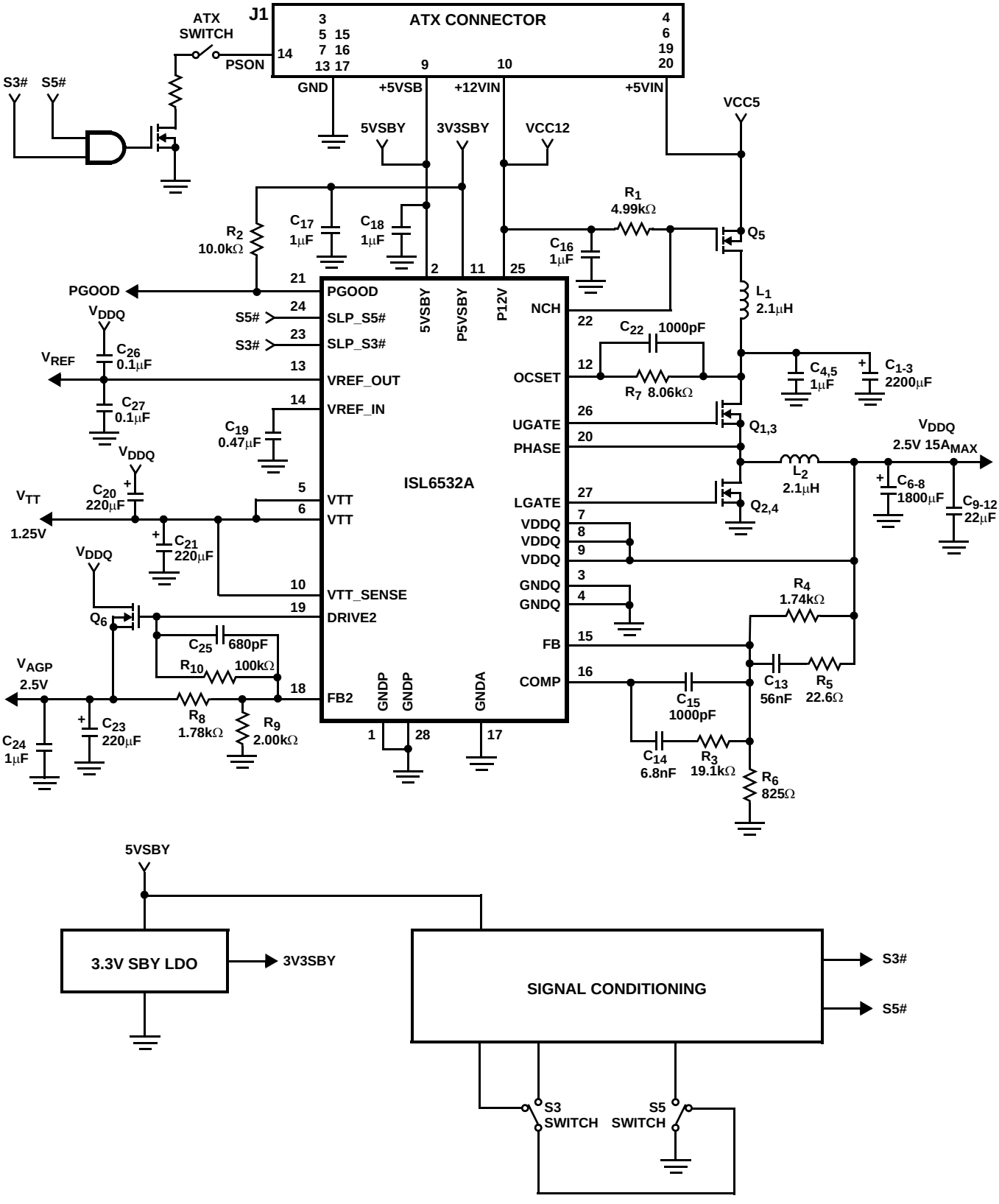
The ISL6532AEVAL1 is a versatile platform that allows designers to gain a full understanding of the functionality of the ISL6532A in a DDR Memory System. The board is also flexible enough to allow the designer to modify the board for differing requirements.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6532A Data Sheet,* Intersil Corporation, File No. FN9099.

ISL6532EVAL1 Schematic



ISL6532AEVAL1 Bill of Material

REF DES	DESCRIPTION	PKG	VENDOR	VENDOR P/N	QTY
C4, 5, 16-18	1µF, X5R Capacitor	0603	Various	-	6
C1, 2, 3	2200µF 6.3V MBZ Capacitor	10x20	Rubycon	6.3MBZ2200M10X20	3
C6, 7, 8	1800µF 16V MBZ Capacitor	10x23	Rubycon	16MBZ1800M10X23	3
C20, 21, 23	220µF, 25V	8x11.5	Panasonic	EEU-FCIE221	3
C9-12	22µF Capacitor	1206	Various	-	4
C13	56nF Capacitor	0603	Vishay	VJ0603Y563KXXA	1
C14	6.8nF Capacitor	0603	Vishay	VJ0603Y682KXBA	1
C15, 22	1000pF Capacitor	0603	Vishay	VJ0603Y102KXB	2
C19	0.047µF, 10V, X5R MLC Capacitor	0603	TDK	C1608X5R1A474K	1
C25	680pF Capacitor	0603	Vishay	VJ0603Y681KXB	1
C26, 27	0.1µF Capacitor	0603	Vishay	VJ0603Y104KXXA	2
L1, 2	2.1µH, 7T 14AWG on T50-52B Core	-	CoEv	C9616	2
Q1-4, Q6	30V N-Channel MOSFET	PowerPak	Vishay	Si7840DP	5
Q5	30V N-Channel MOSFET	DPAK	Vishay	SUD50N03-07	1
R1, 4	1.74kΩ, 1% Resistor	0603	Vishay	CRCW06031741F	2
R2	10.0kΩ, 1% Resistor	0603	Vishay	CRCW06031002F	1
R3	19.1kΩ, 1% Resistor	0603	Vishay	CRCW06031912F	1
R5	22.6Ω, 1% Resistor	0603	Vishay	CRCW060322R6F	1
R6	825Ω, 1% Resistor	0603	Vishay	CRCW0603825RF	1
R7	8.06kΩ, 1% Resistor	0603	Vishay	CRCW06038061F	1
R8	1.78kΩ, 1% Resistor	0603	Vishay	CRCW06031781F	1
R9	2.00kΩ, 1% Resistor	0603	Vishay	CRCW06032001F	1
R10	100kΩ, 1% Resistor	0603	Vishay	CRCW06031003F	1
U1	ACPI Compliant DDR Power Regulator	28ld 6x6mm QFN	Intersil	ISL6532ACR	1

SL6532AEVAL1 Layout

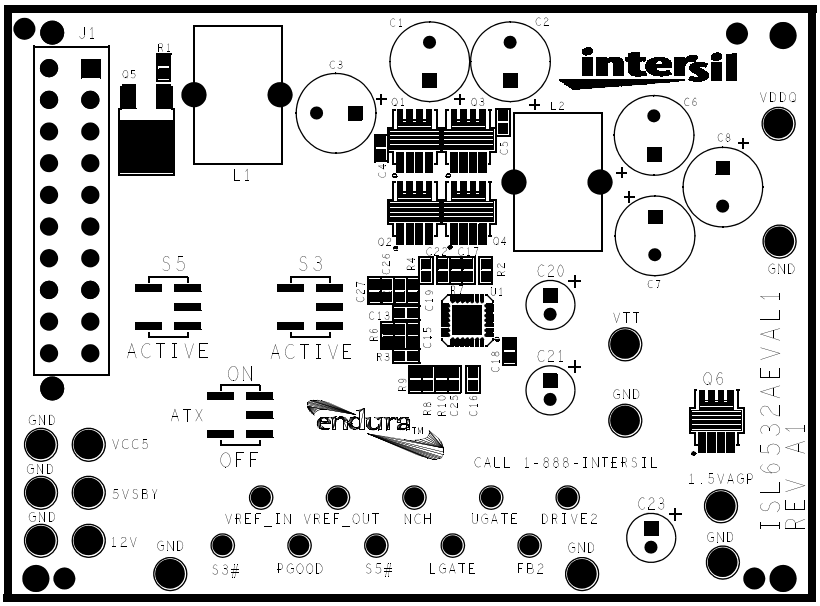


FIGURE 12. TOP SILK SCREEN

SL6532AEVAL1 Layout (Continued)

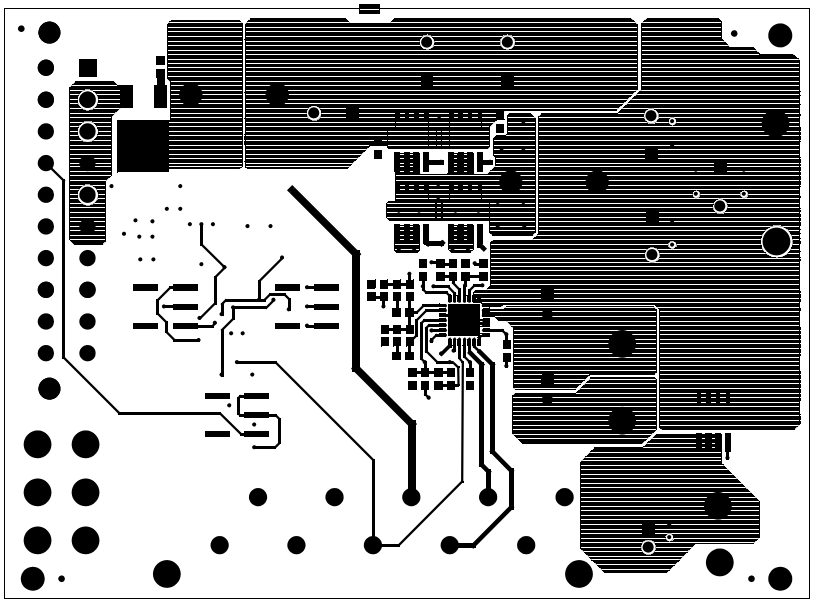


FIGURE 13. TOP

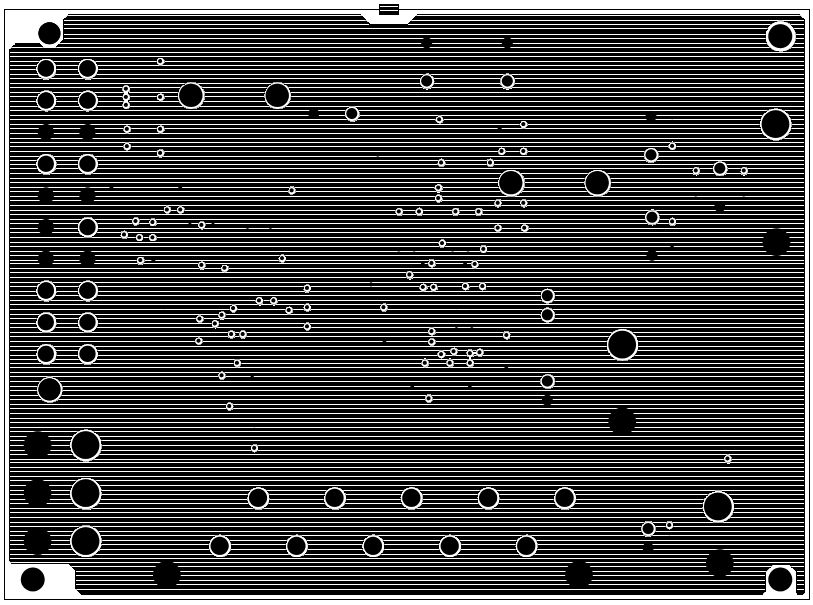


FIGURE 14. INTERNAL 1 GROUND

SL6532AEVAL1 Layout (Continued)

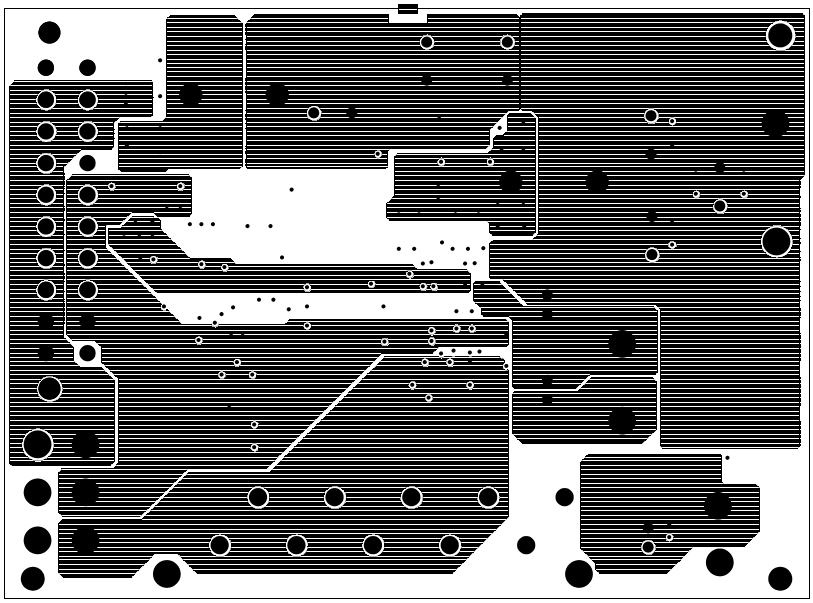


FIGURE 15. INTERNAL 2 POWER

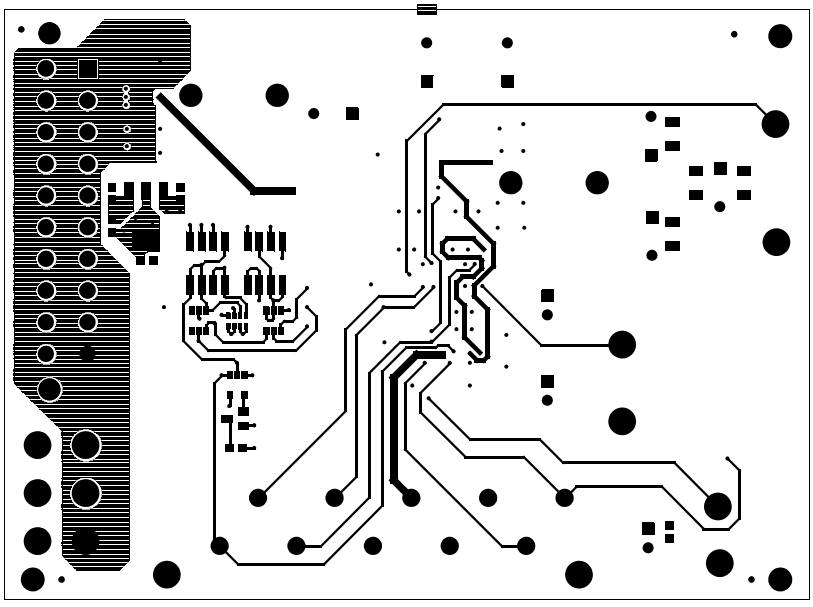


FIGURE 16. BOTTOM

SL6532AEVAL1 Layout (Continued)

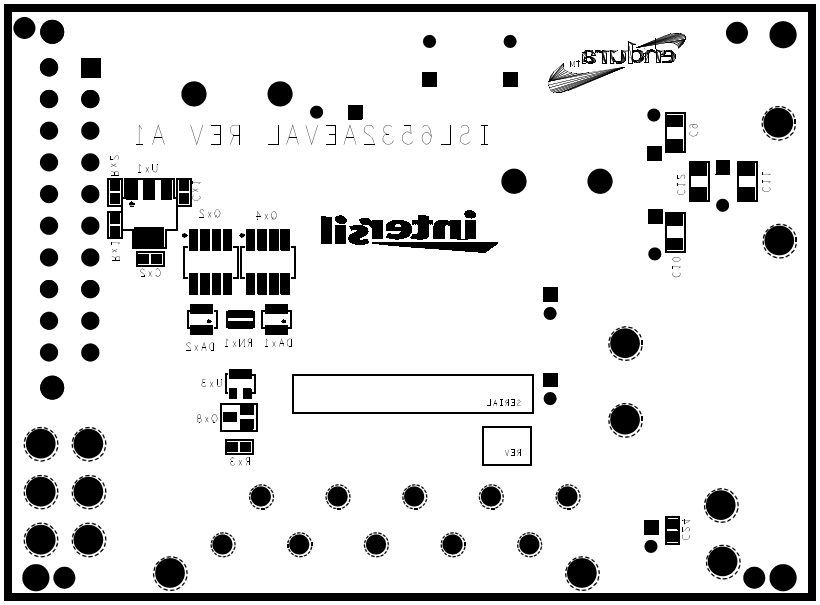


FIGURE 17. BOTTOM SILK SCREEN