Evaluation Board for ADP2116

EVAL-ADP2116

FEATURES

Full featured demo board for the ADP2116
Standalone capability
Configurable, dual synchronous step-down, dc-to-dc switching regulator
Dual 3 A/3 A or 3 A/2 A output or single combined 6 A output
Input voltage V_{IN}: 2.75 V to 5.5 V
Selectable fixed output: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V or adjustable output voltage to 0.6 V minimum
Selectable switching frequency: 300 kHz, 600 kHz, 1.2 MHz or synchronized from 200 kHz to 2 MHz
Configurable SYNC input or CLKOUT output
Two independent enable inputs
Two power good outputs
Externally programmable soft start
Size: 3-9/16 inch × 2-5/8 inch

APPLICATIONS

Demonstrate features and configurability of ADP2116
Emulate functionality of ADP2116 in a user's circuit
Evaluate ADP2116 performance

GENERAL DESCRIPTION

The ADP2116 evaluation (demo) board is a complete, dual, step-down, dc-to-dc converter design based on the ADP2116, a configurable, dual 3 A/single 6 A, synchronous step-down, dc-to-dc regulator.

The ADP2116 is a versatile step-down switching regulator that satisfies a wide range of user point-of-load requirements. The two PWM channels are 180° phase shifted and provide ±1.5% accurate regulated output voltages. For more details, see the ADP2116 data sheet.

The ADP2116 evaluation board comes configured with 2.5 V at 3 A and 1.2 V at 3 A outputs, the switching frequency is set to 600 kHz, and pulse skip is enabled. If needed, the ADP2116 evaluation board output voltages and configuration can be modified by changing the values of the appropriate passive components and changing the links. The ambient temperature operating range is from −40°C to +85°C.

ADP2116 EVALUATION BOARD

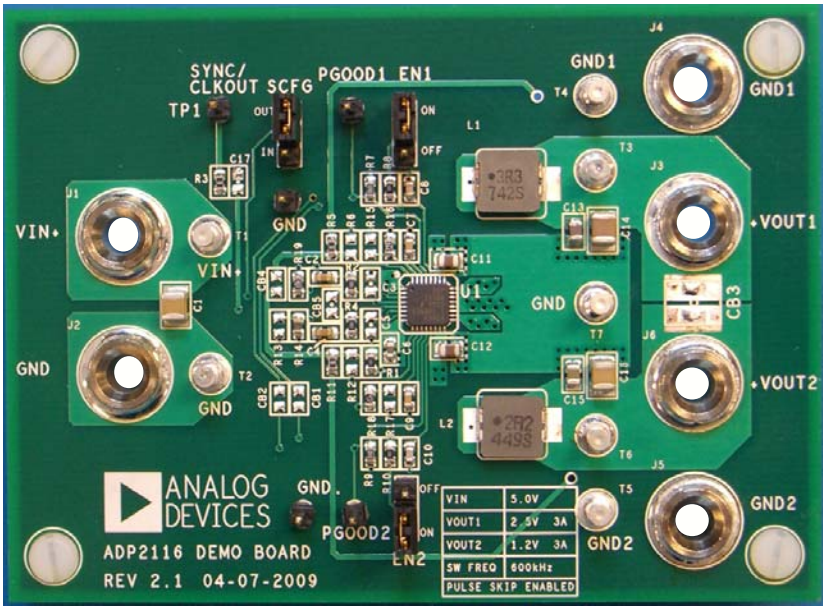

Figure 1. ADP2116-EVALZ—V_{OUT1}: 2.5 V @ 3 A; V_{OUT2}: 1.2 V @ 3 A; f_{SW} = 600 kHz; Pulse Skip Enabled

Rev. 0

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REVISION HISTORY

11/09—Revision 0: Initial Version

USING THE EVALUATION (DEMO) BOARD

POWERING UP

The ADP2116 evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Input Power Source

The power source voltage must not exceed 5.5 V, which is the maximum operating input voltage of the ADP2116.

Connect the negative terminal of the power source to the J2 (GND) jack of the evaluation board and the positive terminal of the power source to the J1 (VIN+) jack of the evaluation board.

Output Load

Before connecting a load to the output of the demo board, make sure that the output voltage does not exceed the maximum operating voltage range of the load. To connect a load to the output of Channel 1, connect the negative terminal of the load to Jack J4 (GND1) on the evaluation board and connect the positive terminal of the load to Jack J3 (+VOUT1). To connect a load to the output of Channel 2, connect the negative terminal of the load to Jack J5 (GND2) of the evaluation board and connect the positive terminal to Jack J6 (+VOUT2).

For the single interleaved output configuration, the outputs of Channel 1 and Channel 2 are shorted together by soldering Link CB3. To apply a load to the single interleaved dual-phase output, connect the negative terminal of the load to either Jack J4 (GND1) or Jack J5 (GND2) of the evaluation board and connect the positive terminal of the load to either Jack J3 (+VOUT1) or Jack J6 (+VOUT2).

Enabling and Disabling the DC-to-DC Converter

HEADER3 EN1 is used to control Channel 1. Use one of the following methods to enable or disable Channel 1:

- To enable Channel 1, short the middle pin of HEADER3 EN1 to VIN+ by placing a shunt in the on position, or apply a dc voltage from 2.0 V to 5.5 V to the middle pin.
- To disable Channel 1, short the middle pin of HEADER3 EN1 to GND by placing a shunt in the off position or apply a positive dc voltage below 0.8 V to the middle pin.

HEADER3 EN2 is used to control Channel 2. Use one of the following methods to enable or disable Channel 2:

- To enable Channel 2, short the middle pin of HEADER3 EN2 to VIN+ by placing a shunt in the on position, or apply a dc voltage from 2.0 V to 5.5 V to the middle pin.
- To disable Channel 2, short the middle pin of HEADER3 EN2 to GND by placing a shunt in the off position, or apply a positive dc voltage below 0.8 V to the middle pin.

For the single interleaved output configuration, the EN1 and EN2 signals are connected together at the Circuit Breaker CB1, which is a solder link. Use either HEADER3 EN1 or EN2 to enable and disable Channel 1 and Channel 2 simultaneously.

Input and Output Voltages

To measure the input voltage, V_{IN}, connect the negative probe of the voltmeter to Terminal T2 (GND) on the evaluation board and connect the positive probe to Terminal T1 (VIN+).

To measure the output voltage of Channel 1, V_{OUT1}, connect the negative probe of the voltmeter to Terminal T4 (GND1) and connect the positive probe to Terminal T3. To measure the output voltage of Channel 2, V_{OUT2}, connect the negative probe to Terminal T5 (GND2) and connect the positive probe to Terminal T6.

To measure the output voltage, V_{OUT}, for the single interleaved output configuration, connect the negative probe of the voltmeter to Terminal T7 (GND) and connect the positive probe to either Terminal T3 or Terminal T6.

External Synchronization

To synchronize the dc-to-dc converter to an external clock:

1. Short the middle pin of HEADER3 SCFG to GND by placing a shunt in the in position. This configures the (SYNC/CLKOUT) pin of the ADP2116 as an input.
2. Apply an external clock signal to Test Point TP1 SYNC/CLKOUT. The clock signal must have a logic high level from 2.0 V up to the voltage of the input power, V_{IN}, and a logic low level below 0.8 V. Set the external clock pulse width to more than 100 ns and the frequency, f_{SYNC}, equal to double the target PWM switching frequency, f_{SW}:

$$f_{SYNC} = 2 \times f_{SW} \quad (1)$$

For reliable synchronization, the external clock frequency, f_{SYNC}, must be in the range from 800 kHz to 2 MHz because the switching frequency is set to 600 kHz.

Internal Clock Out

Shorting the middle pin of HEADER3 SCFG to VIN+ by placing the shunt in the out position makes the ADP2116 internal clock available at Test Point TP1 (SYNC/CLKOUT). The frequency of the internal clock, f_{CLKOUT}, is twice that of the switching frequency, f_{SW}, of the converter and 90° phase-shifted.

PGOOD1 and PGOOD2 Signals

When Channel 1 is enabled and the output voltage, V_{OUT1}, is in regulation range, the logic signal at the Test Point PGOOD1 is high. When Channel 2 is enabled and the output voltage, V_{OUT2}, is in regulation range, the logic signal at Test Point PGOOD2 is also high. For the single dual-phase interleaved output configuration, the PGOOD1 and PGOOD2 signals are tied together at the Circuit Breaker CB2, which is a solder link. Use either Test Point PGOOD1 or Test Point PGOOD2 to monitor whether the converter output voltage, V_{OUT}, is within regulation.

EVALUATING PERFORMANCE OF THE DC-TO-DC CONVERTER

Switching Waveforms

To observe the switching waveform with an oscilloscope, place the probe tip at the end of Inductor L1 (or L2 for Channel 2) that is connected to the SWx pin of the ADP2116. The probe ground is connected to GND.

Output Voltage Ripple

To observe the output voltage ripple, place the oscilloscope probe tip at Terminal T3 (or T6 for Channel 2), the converter output, and connect the probe ground lead to Terminal T7 (GND). The oscilloscope input should be set to ac-coupled.

Measuring Efficiency

The efficiency, η, is calculated by comparing the measured input power with the measured output power of the converter:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad (2)$$

Measuring Line Regulation

Vary the input voltage and measure the change of the output voltage.

Measuring Load Regulation

Measure the load regulation by increasing the load current at the output and measuring the change in output voltage.

Line Transient Response

Generate a step input voltage (V_{IN}) change and observe the behavior of the output voltage, V_{OUT1} (V_{OUT2} for Channel 2), with an oscilloscope.

Load Transient Response

Generate a load current transient at the output, V_{OUT1} (V_{OUT2} for Channel 2), and observe the output voltage response with an oscilloscope. Use a current probe attached to the wire between the output and the load to visualize the current transient.

MODIFYING THE BOARD

To modify the converter configuration, unsolder and/or replace/remove the appropriate passive components or links on the board.

Changing the Operation Mode Settings

The operating mode of the ADP2116 dc-to-dc converter can be changed by replacing the configuration resistors, R13 and R14, with a different value, as shown in Table 1. This configuration sets the current limit for Channel 2 and enables or disables the transition to pulse skip mode at light loads.

Table 1. Setting the Operating Mode

		Maximum DC Load Current (A)		Peak Current Limit (A)		
R13 (Ω) ± 5%	**R14 (Ω) ± 5%**	**V_{OUT1}**	**V_{OUT2}**	**V_{OUT1}**	**V_{OUT2}**	**Pulse Skip**
0	Open	3	3	4.5	4.5	Forced PWM
Open	82 k	3	3	4.5	4.5	Enabled
Open	47 k	3	2	4.5	3.3	Forced PWM
Open	27 k	3	2	4.5	3.3	Enabled

Changing the Output Voltages

The output voltages set points of the converter can be changed by replacing Resistor R15, Resistor R16, Resistor R17, and Resistor R18 with the resistor values shown in Table 3.

In addition, when the adjustable output voltage version is used for the ADP2116, the output voltage, V_{OUT1}, is set by the resistive voltage divider R5/R6 and the output voltage, V_{OUT2}, is set by the resistive voltage divider R11/R12.

To calculate the desired resistor values, first determine the value of the bottom divider string resistor, R6 (R12 for Channel 2), by ensuring that the divider string current, I_{STRING}, is greater than 20 µA.

For Channel 1,

$$R6 = 0.6\text{ V}/I_{STRING} \quad (3)$$

For Channel 2,

$$R12 = 0.6\text{ V}/I_{STRING} \quad (4)$$

Then calculate the value of the top resistor, R5 (R11 for Channel 2).

For Channel 1,

$$R5 = R6 \times \left[\frac{V_{OUT1} - 0.6\text{ V}}{0.6\text{ V}}\right] \quad (5)$$

For Channel 2,

$$R11 = R12 \times \left[\frac{V_{OUT2} - 0.6\text{ V}}{0.6\text{ V}}\right] \quad (6)$$

Note that when the output voltage of Channel 1, V_{OUT1}, is changed, to ensure stable operation, the values of Inductor L1, the C13 and C14 output capacitors, and the R2 and C2 compensation components must be recalculated and changed (see the ADP2116 data sheet for details on external component selection). If the output voltage of Channel 2, V_{OUT2}, is changed, the values of the Inductor L2, the C15 and C16 output capacitors, and the R4 and C4 compensation components must be recalculated and changed.

Changing the Switching Frequency

The switching frequency (f_{SW}) set point can be changed by replacing Resistor R19 with a different value, as shown in Table 2.

Table 2. Setting the Switching Frequency, f_{SW}

R19 (Ω) ± 5%	Switching Frequency, f_{SW} (kHz)
0	300
8.2 k	600
27 k	1200

Note that when the switching frequency (f_{SW}) is changed, to ensure stable operation, the values of the Inductor L1 and Inductor L2, the C13, C14, C15, and C16 output capacitors, and the R2, C2, R4, and C4 compensation components must be recalculated and changed (see the ADP2116 data sheet for details on external component selection).

Changing the Soft Start Time

The soft start time of the ADP2116 on the evaluation board is programmed to 1 ms.

To change the soft start time, t_{SS}, replace Capacitor C7 (C9 for Channel 2) with a different capacitor value using the following:

For Channel 1,

$$C7\text{ [nF]} = 10 \times t_{SS}\text{ [ms]} \quad (7)$$

For Channel 2,

$$C9\text{ [nF]} = 10 \times t_{SS}\text{ [ms]} \quad (8)$$

Combining the Two Channels into a Single Output

For a single, interleaved dual-phase output, make the following modifications:

- Short the outputs, +VOUT1 and +VOUT2, by soldering the bridge on CB3.
- Tie the EN1 and EN2 signals by shorting CB1.
- Tie the PGOOD1 and PGOOD2 signals by shorting CB2.
- Tie the FB1 and FB2 signals by shorting CB4.
- Tie the COMP1 and COMP2 signals by shorting CB5.
- Set the same output voltages of both channels by choosing R15 = R17 and R16 = R18.
- Choose and set the operating mode to 3 A/3 A, forced PWM configuration, by setting R13 to 0 Ω and leaving R14 open.

Table 3. Programming the Output Voltages

R15 (Ω) ± 5%	R16 (Ω) ± 5%	V_{OUT1} (V)	R17 (Ω) ± 5%	R18 (Ω) ± 5%	V_{OUT2} (V)
Open	0	0.8	Open	0	0.8
Open	4.7 k	1.2	Open	4.7 k	1.2
Open	8.2 k	1.5	Open	8.2 k	1.5
Open	15 k	1.8	Open	15 k	1.8
Open	27 k	2.5	Open	27 k	2.5
Open	47 k	3.3	Open	47 k	3.3
Open	82 k	Adjustable 0.6 to <1.6	Open	82 k	Adjustable 0.6 to <1.6
0	Open	Adjustable 1.6 to 3.3	0	Open	Adjustable 1.6 to 3.3

TYPICAL PERFORMANCE CHARACTERISTICS

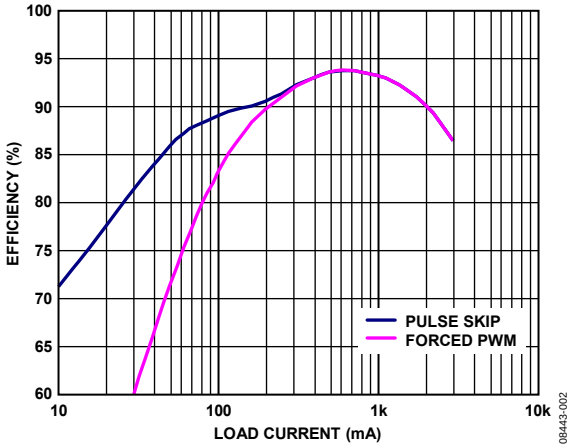

Figure 2. Efficiency vs. Load, V_{IN} = 5 V, Channel 1, V_{OUT1} = 2.5 V

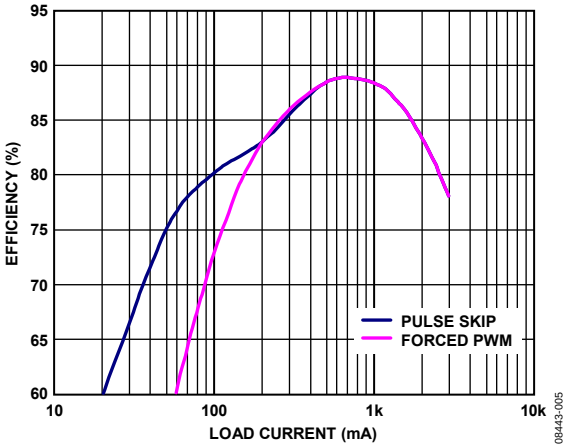

Figure 5. Efficiency vs. Load, Channel 2, V_{IN} = 5 V, V_{OUT2} = 1.2 V

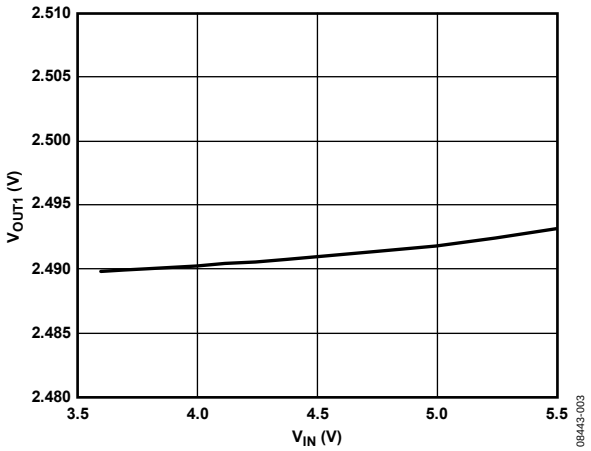

Figure 3. Line Regulation, Channel 1, V_{OUT1} = 2.5 V, 3 A Load

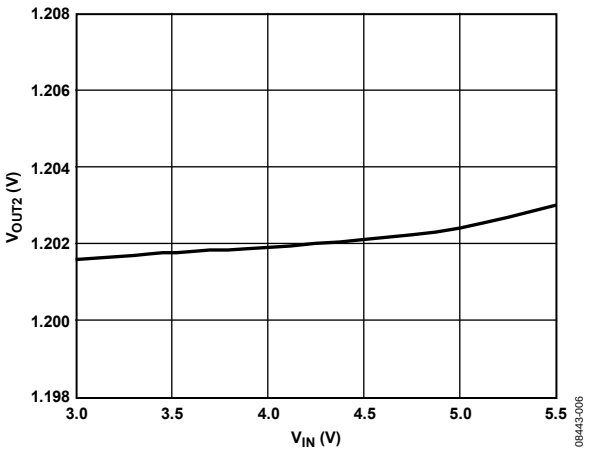

Figure 6. Line Regulation, Channel 2, V_{OUT2} = 1.2 V, 3 A Load

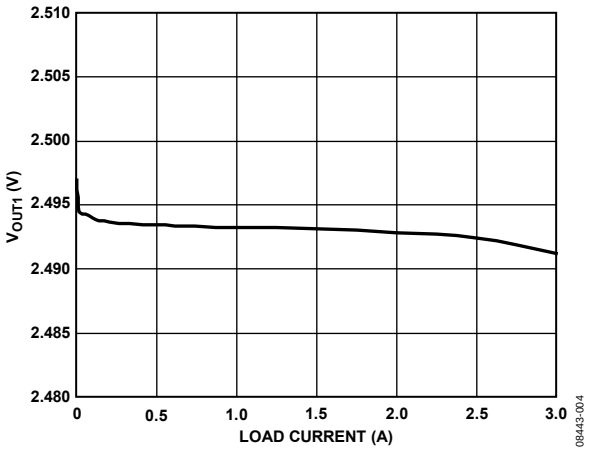

Figure 4. Load Regulation, Channel 1, V_{IN} = 5 V, V_{OUT1} = 2.5 V, Pulse Skip Enabled

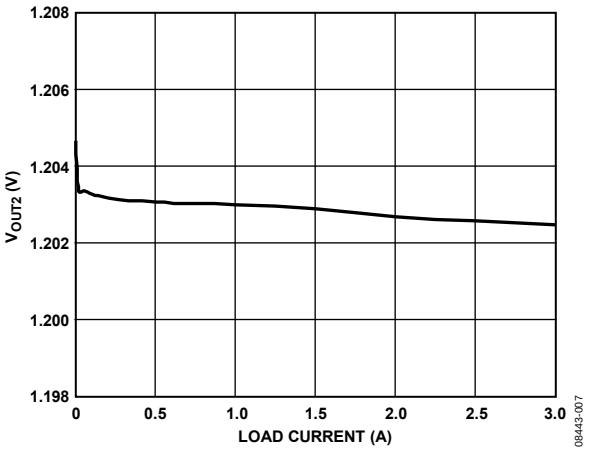

Figure 7. Load Regulation, Channel 2, V_{IN} = 5 V, V_{OUT2} = 1.2 V, Pulse Skip Enabled

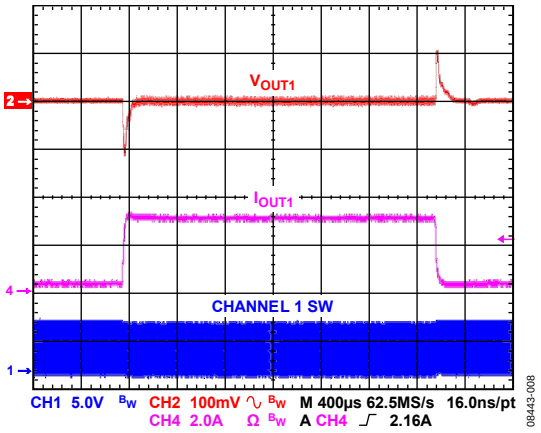

Figure 8. Load Transient Response, 0.3 A to 3 A, V_{OUT1} = 2.5 V

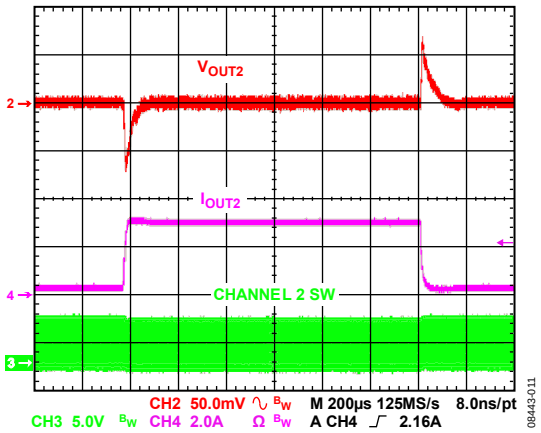

Figure 11. Load Transient Response, 0.3 A to 3A, V_{OUT2} = 1.2 V

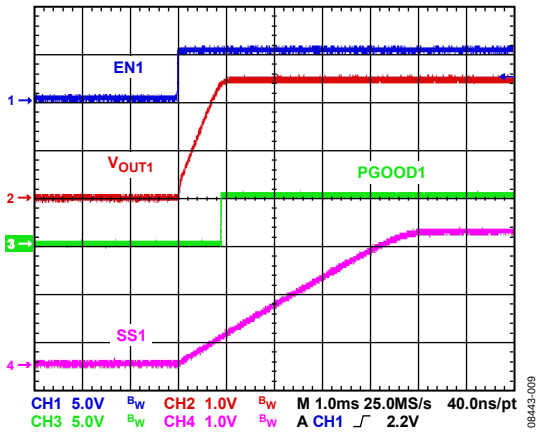

Figure 9. Soft Start, Channel 1, V_{OUT1} = 2.5 V

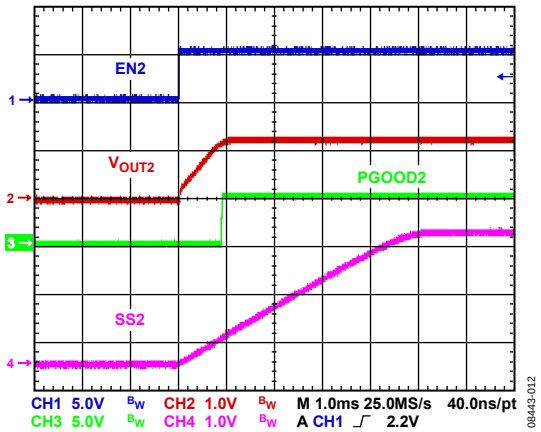

Figure 12. Soft Start, Channel 2, V_{OUT2} = 1.2 V

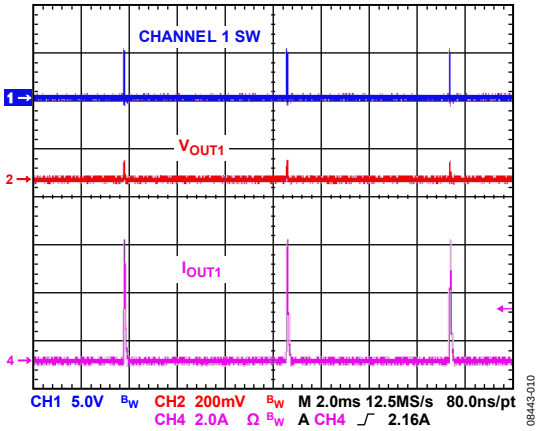

Figure 10. Current Limit Operation, Channel 1

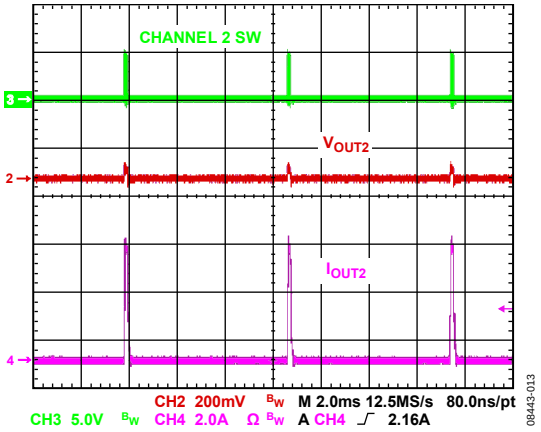

Figure 13. Current Limit Operation, Channel 2

BODE PLOTS

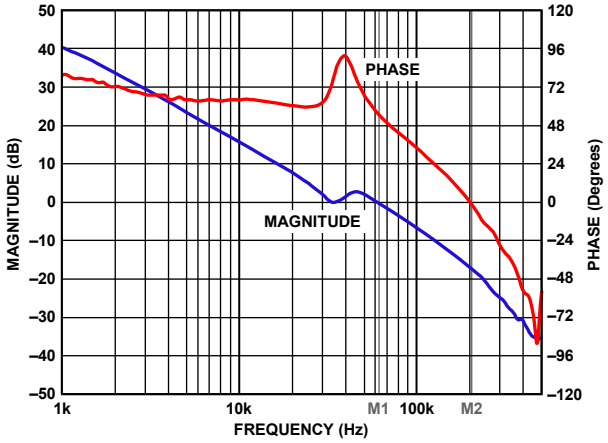

Figure 14. Channel 1: V_{IN} = 5 V, V_{OUT1} = 2.5 V, Load = 3 A, f_{SW} = 600 kHz, Crossover Frequency (f_{CO}) = 62 kHz; Phase Margin 55°

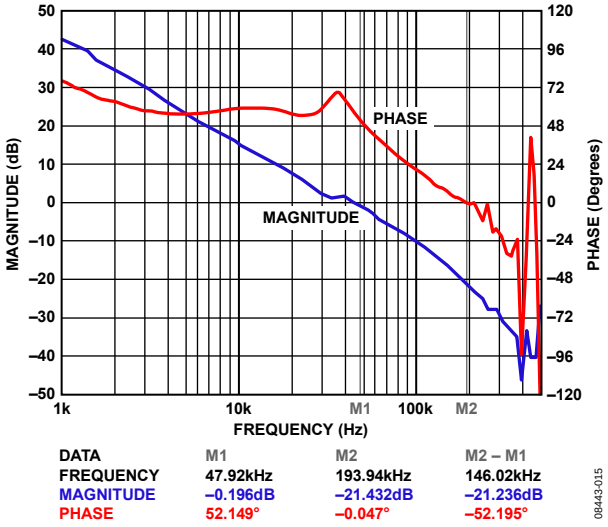

Figure 15. Channel 2: V_{IN} = 5 V, V_{OUT2} = 1.2 V, Load = 3 A, f_{SW} = 600 kHz, Crossover Frequency (f_{CO}) = 48 kHz; Phase Margin 52°

EVALUATION BOARD SCHEMATICS AND ARTWORK

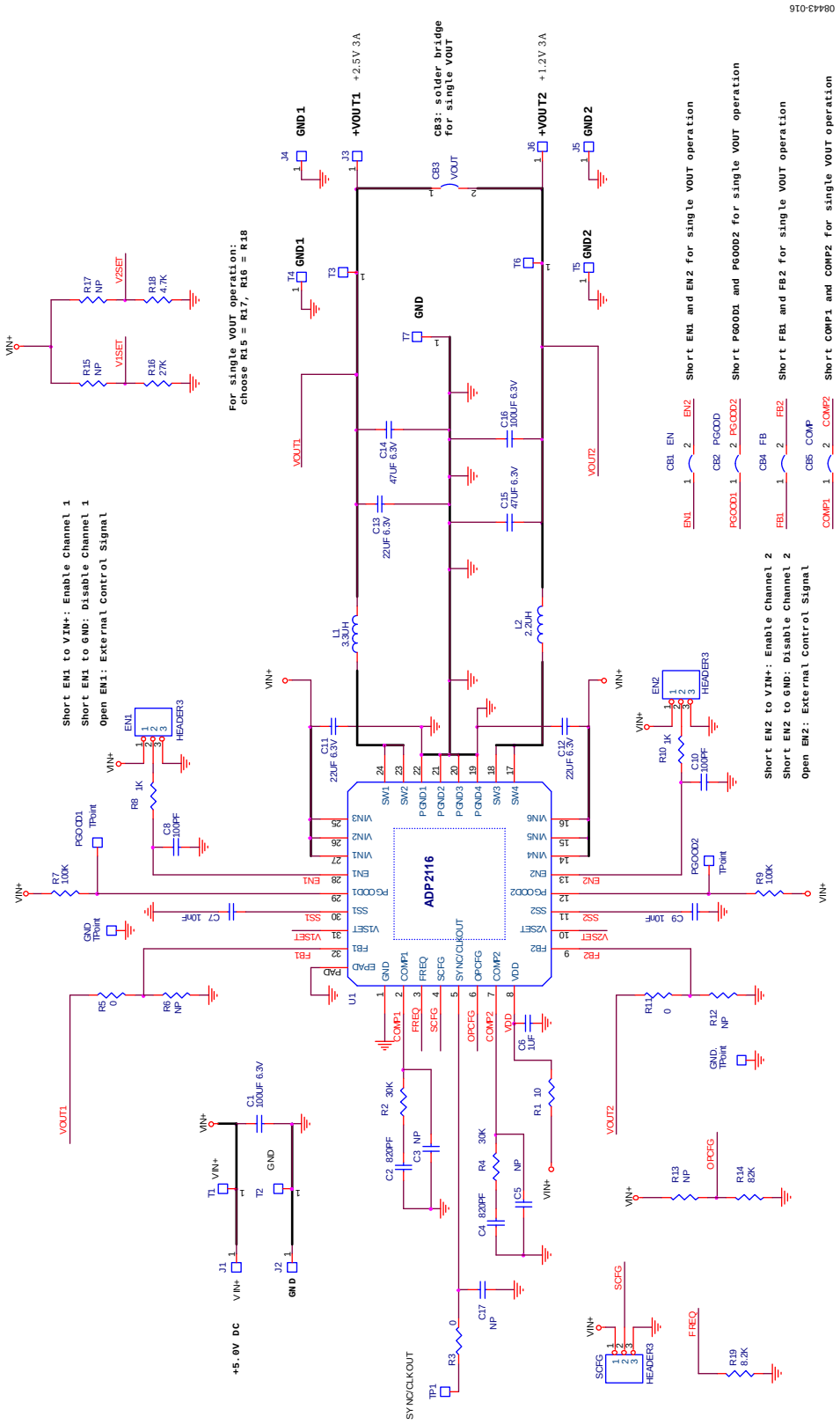

Figure 16. ADP2116-EVALZ Schematic: Dual 2.5 V at 3 A and 1.2 V at 3A Output, Switching Frequency 600 kHz, Pulse Skip Enabled

PCB LAYOUT

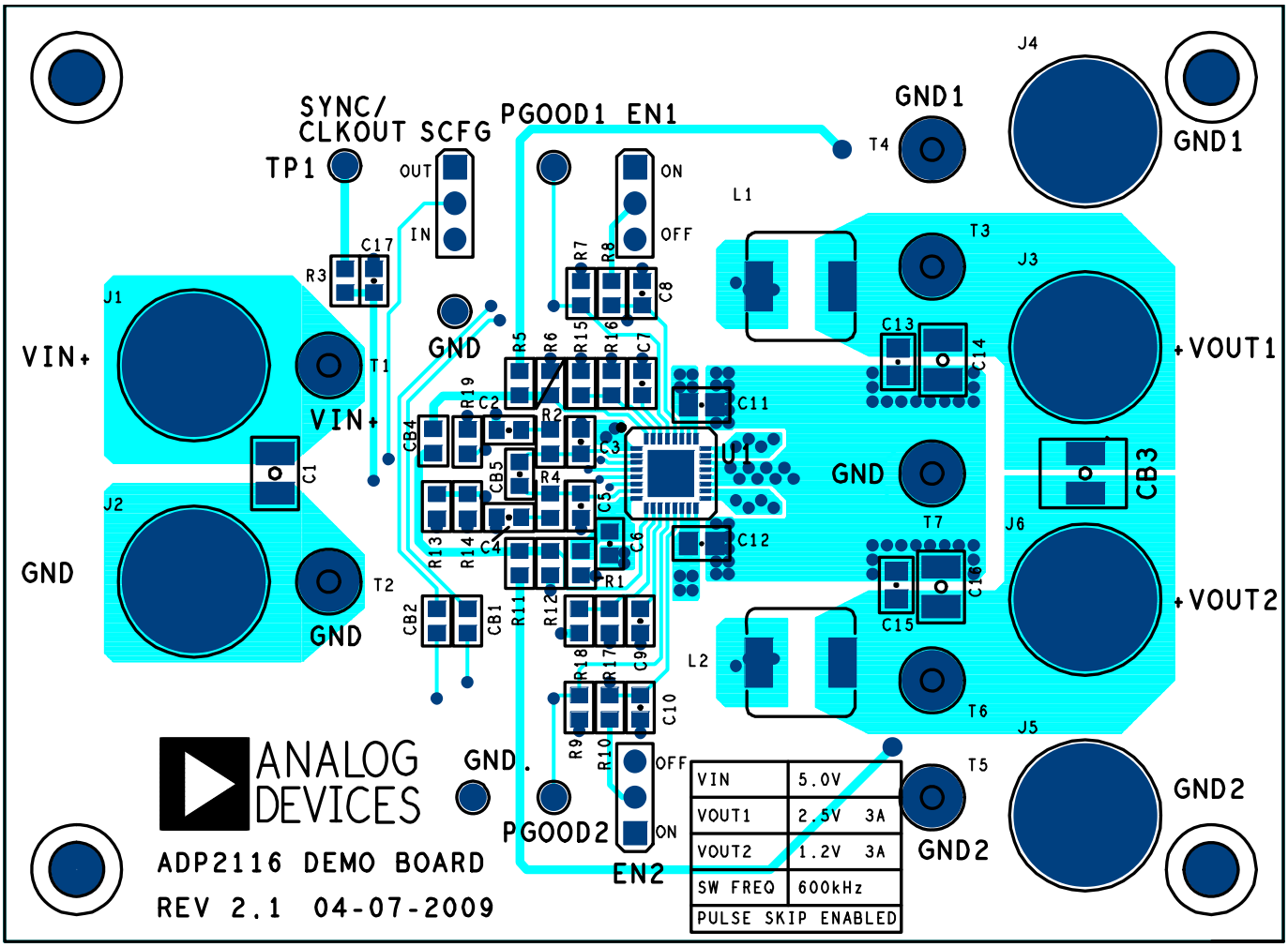

Figure 17. Layer 1—Component Side

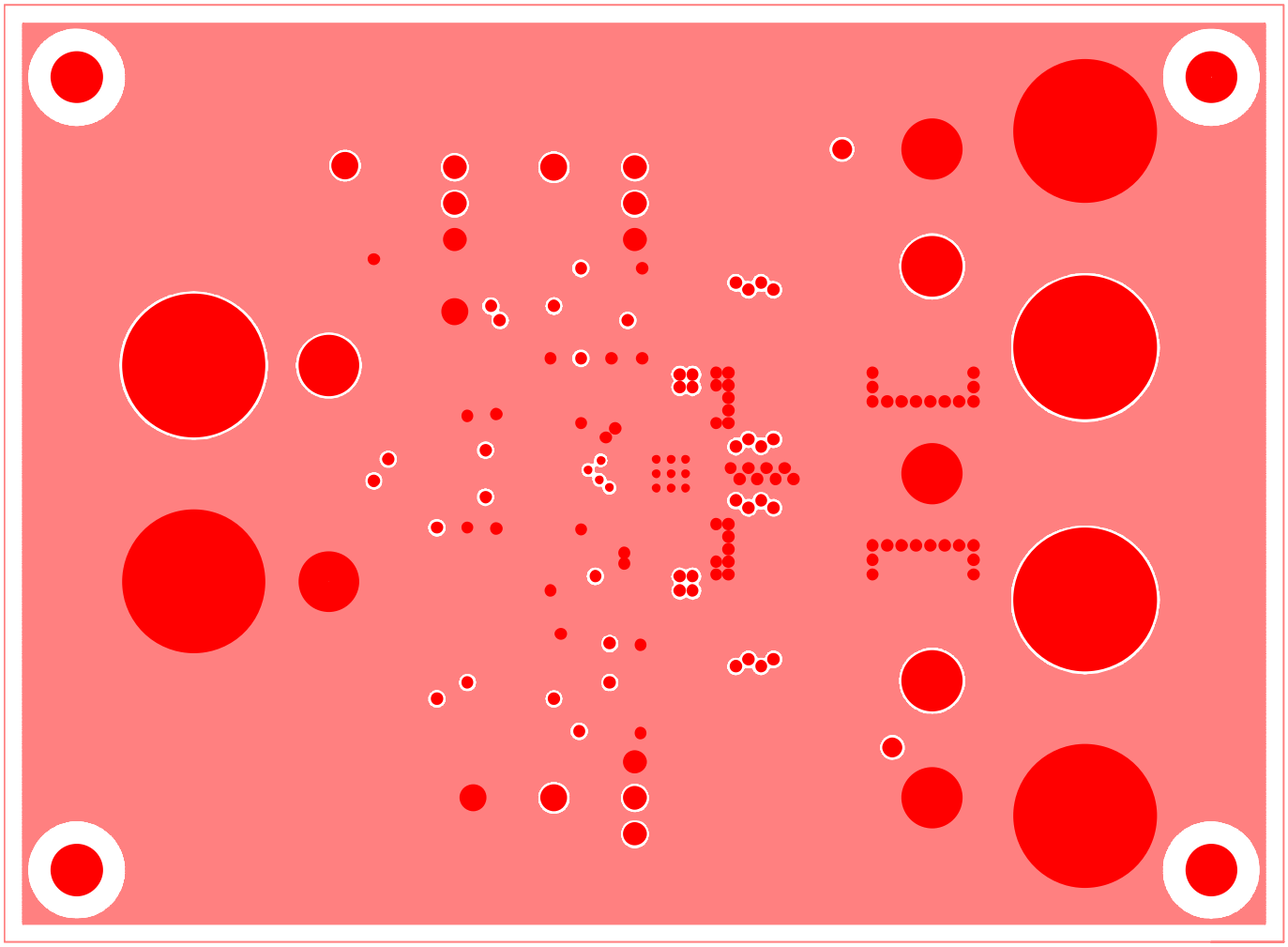

Figure 18. Layer 2—Ground Plane

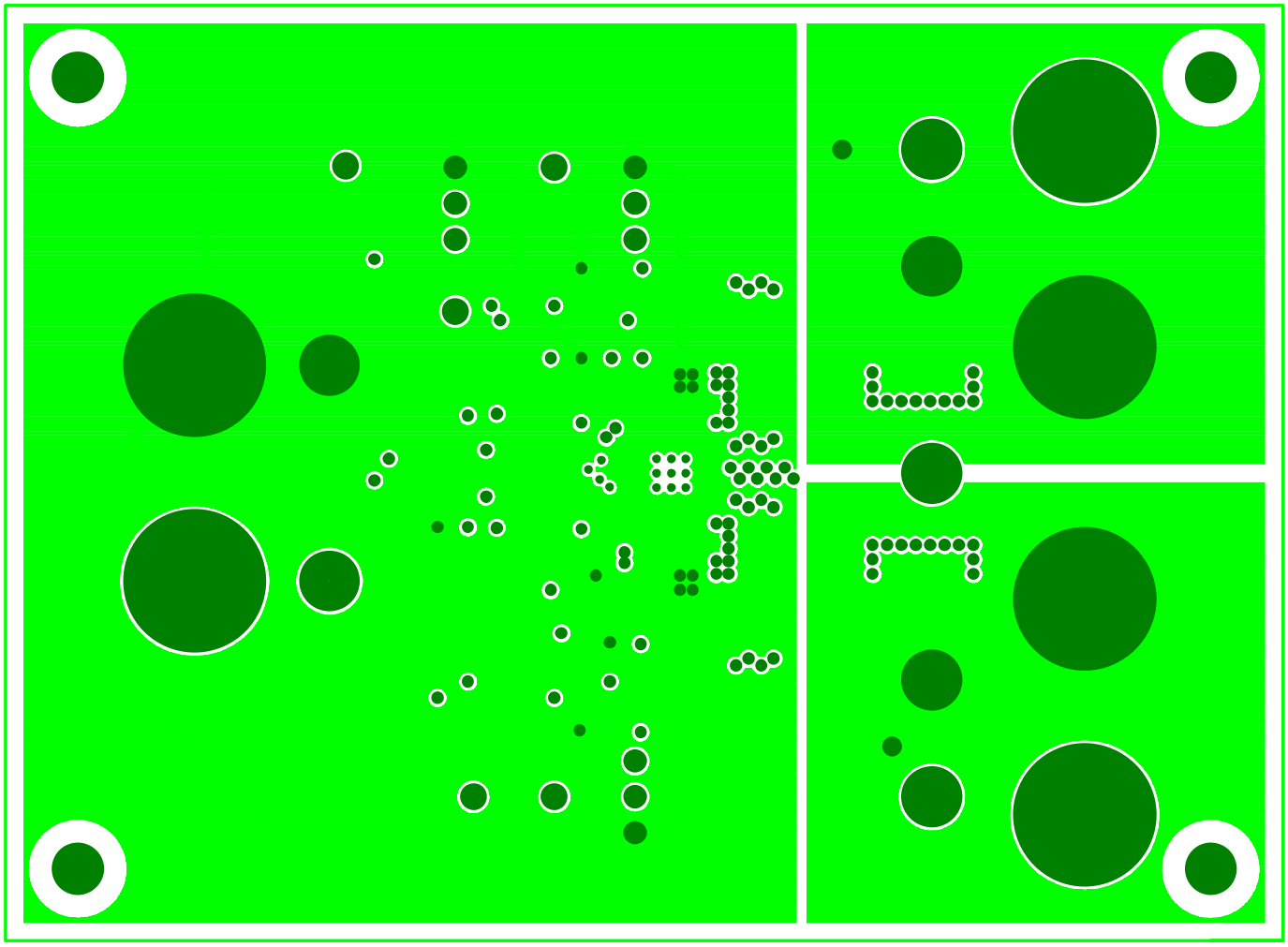

Figure 19. Layer 3—Power Plane

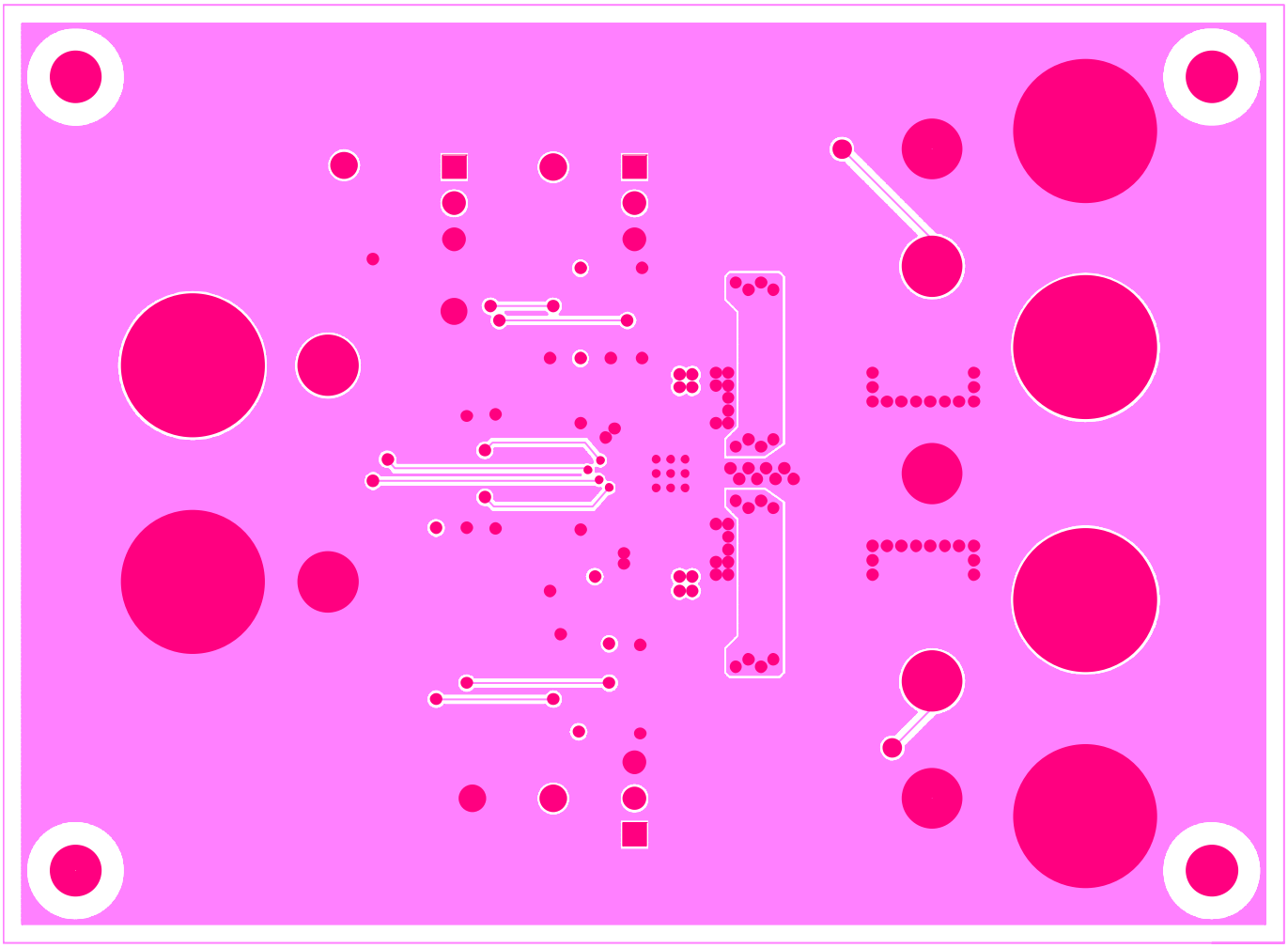

Figure 20. Layer 4—Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. ADP2116-EVALZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
4	CB1, CB2, CB4, CB5	Circuit breaker, 0603, open		
1	CB3	Circuit breaker, open		
2	C1, C16	Capacitor, MLCC, 100 µF, 6.3 V, X5R, 1210	Murata	GRM32ER60J107ME20L
2	C2, C4	Capacitor, MLCC, 820 pF, 50 V, NP0, 0603	Panasonic	ECJ-1VC1H821J
3	C3, C5, C17	Not populated		
1	C6	Capacitor, MLCC, 1.0 µF, 10 V, X7R, 0603	TDK	C1608X7R1C105K
2	C7, C9	Capacitor, MLCC, 10000 pF, 50 V, X7R, 0603	Panasonic	ECJ-1VB1H103K
2	C8, C10	Capacitor, MLCC, 100 pF, 50 V, C0G, 0603	TDK	C1608C0G1H101J
3	C11, C12, C13	Capacitor, MLCC, 22 µF, 6.3 V, X5R, 0805	TDK	C2012X5R0J226M
1	C14	Capacitor, MLCC, 47 µF, 6.3 V, X5R, 1210	Panasonic	ECJ-4YB0J476M
1	C15	Capacitor, MLCC, 47 µF, 6.3 V, X5R, 0805	Taiyo Yuden	JMK212BJ476MG-T
3	EN1, EN2, SCFG	HEADER3 0.100 inch	Sullins	PBC03SAAN
5	TP1, PGOOD1, PGOOD2, GND., GND	Test point	Sullins	PBC01SAAN
6	J1, J2, J3, J4, J5, J6	Jack, noninsulated, staking 0.218 inch	Keystone Electronics	575-4
1	L1	Inductor, fixed, 3.3 µH, SMD	TOKO	FDV0620-3R3M
1	L2	Inductor, fixed, 2.2 µH, SMD	TOKO	FDV0620-2R2M
1	R1	Resistor, 10 Ω, 1/10 W, 5%, SMD, 0603		
2	R2, R4	Resistor, 30 kΩ, 1/10 W, 5%, SMD, 0603		
3	R3, R5, R11	Resistor, 0 Ω, 1/10 W, 5%, SMD, 0603		
5	R6, R12, R13, R15, R17	Not populated		
2	R7, R9	Resistor, 100 kΩ, 1/10 W, 5%, SMD, 0603		
2	R8, R10	Resistor, 1 kΩ, 1/10 W, 5%, SMD, 0603		
1	R14	Resistor, 82 kΩ, 1/10 W, 5%, SMD, 0603		
1	R16	Resistor, 27 kΩ, 1/10 W, 5%, SMD, 0603		
1	R18	Resistor, 4.7 kΩ, 1/10 W, 5%, SMD, 0603		
1	R19	Resistor, 8.2 kΩ, 1/10 W, 5%, SMD, 0603		
7	T1, T2, T3, T4, T5, T6, T7	Terminal, double turret, brass, 0.078″	Keystone Electronics	1502-1
1	U1	Configurable, dual 3 A/single 6 A, synchronous step-down, dc-to-dc regulator	Analog Devices	ADP2116ACPZ-R7
3		Connector, shunt dual beam 30AU PCB	Tyco Electronics	390088-1
4		Standoff, 0.500 inch, #4-40, nylon 6/6, hex	Keystone Electronics	1902C
4		Screw, nylon, slot pan head, 4-40 thread, 1/4 inch length	Richco Plastic Co.	NSS-4-4-01

ORDERING GUIDE

Model	Description
ADP2116-EVALZ[1]	Dual Output, 2.5 V at 3 A and 1.2 V at 3 A, 600 kHz Switching Frequency, Pulse Skip Enabled Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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EB08443-0-11/09(0)