ISL6752EVAL1Z Evaluation Board with Synchronous Rectifiers

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Introduction

The ISL6752EVAL1Z board utilizes Intersil's zero voltage switching (ZVS) topology. In addition to the ZVS function, this board also incorporates N-Channel FETs as secondary side rectifiers, also known as synchronous rectifiers (SR). Power dissipation of the secondary side rectifiers is reduced because the conduction losses of SRs can be significantly less than the conduction losses of PN or Schottky diodes.

Scope

This application note will cover the implementation of synchronous rectifiers (SRs) and their associated drive circuits as used on the ISL6752EVAL1Z board. The various implications of using SRs are covered. The implementation of the primary side ZVS controller, based on the ISL6752, is covered extensively in Intersil application note AN1262, "Designing with the ISL6752, ISL6753 Full-Bridge Controllers".

Also covered is the performance of this evaluation board. Measured waveforms are compared to the theoretical waveforms. Efficiency and regulation is also measured.

At the end of this application note, the schematic, the bill of materials and the printed circuit board layout are included for reference.

TABLE 1. SPECIFICATIONS

Max Input Voltage	450VDC
Operating Input Voltage	325V to 425VDC
Max Input Current	2.5ADC
Rated Output Current	50ADC
Current Limit	60A±5%
Output Voltage	12V±5%

Circuit Elements

The evaluaition board is composed of several distinct circuit elements. Please reference the schematic at the end of this application note.

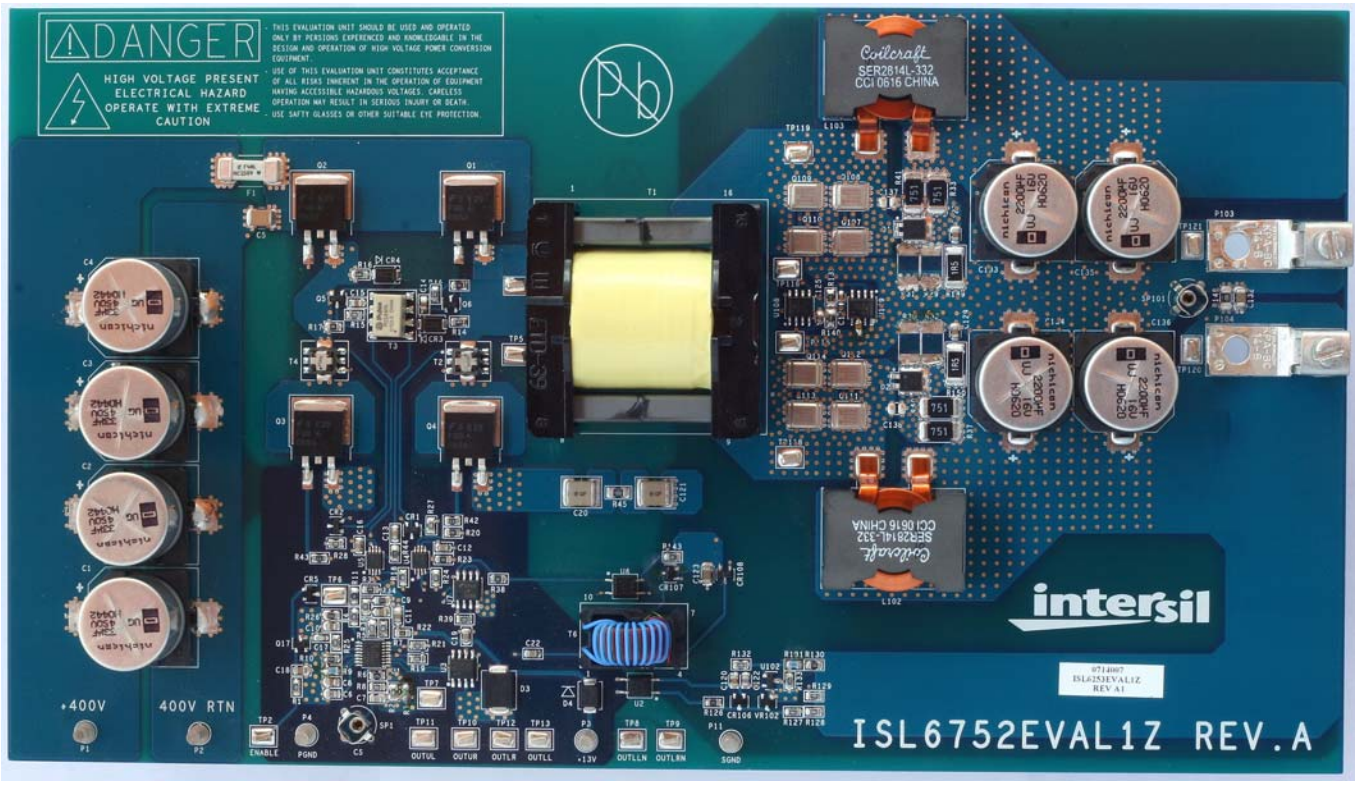


FIGURE 1. ISL6752EVAL1Z EVALUATION BOARD

Primary Side Control

The ISL6752 ZVS controller, U1, is located on the primary side, eliminating the need for two AC line isolating gate drive transformers to drive the primary side bridge FETs. Instead, the low side FETs are driven direcly by MOSFET drivers and the high side FETs are driven by a gate drive transformer that only requires operational insulation. Primary side control also simplifies the design of the current sensing transformers because they also do not have to be AC line isolating.

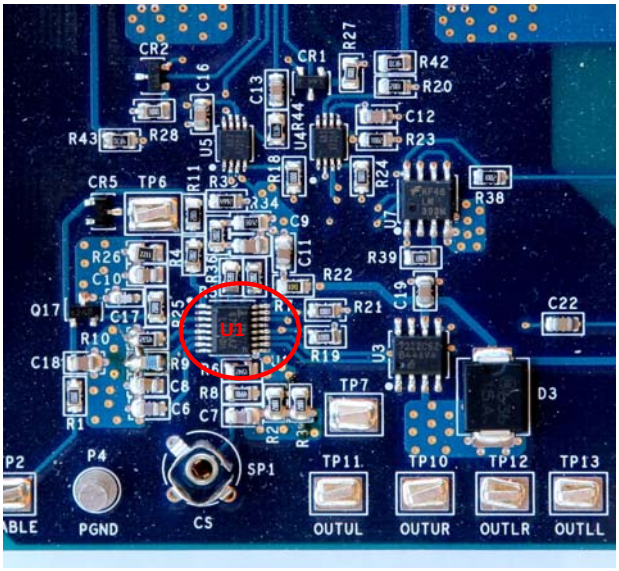


FIGURE 2. PRIMARY SIDE CONTROL CIRCUIT

ZVS Full Bridge

The low side FETs, Q_3 and Q_4, are driven directly by MOSFET drivers, U4. The two high side FETs, Q_1 and Q_2, are also driven by a MOSFET driver, U5, but are coupled with one gate drive transformer, T_3, that has complementary outputs. The design of the gate drive transformer is simplified because it only needs 400V operational insulation and it is always driven with a symmetrical square wave.

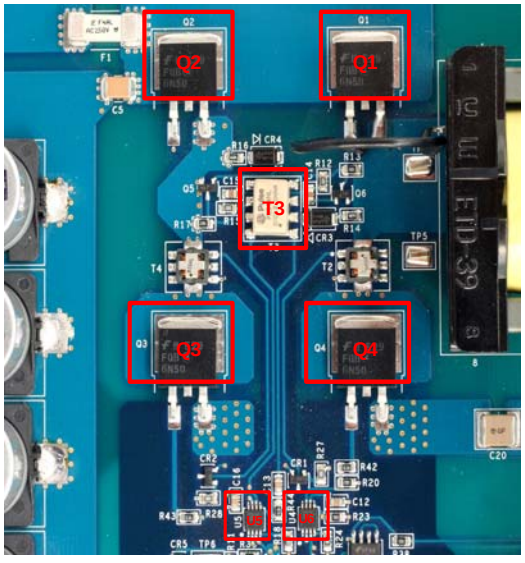


FIGURE 3. ZVS FULL BRIDGE CIRCUIT

High Voltage Protection

Because a failure of the bridge can cause catastrophic damage to the primary side control elements, a voltage crowbar, F1 and D_3, and a voltage blocking diode, D_4, are incorporated. D_3 clamps the bias voltage to a safe level. If 400V is applied to the V_{DD} bias node, F1 opens shortly after D_3 conducts current. D_4 provides additional protection by blocking high voltage from being applied to the 13V lab supply. Note that a fully debugged power supply does not need these additional components. These parts are left on the eval board to minimize damage should the user accidently introduce a fault while evaluating the circuits. The designer may want to keep F1 in the final design to prevent a loud bang should the bridge fail.

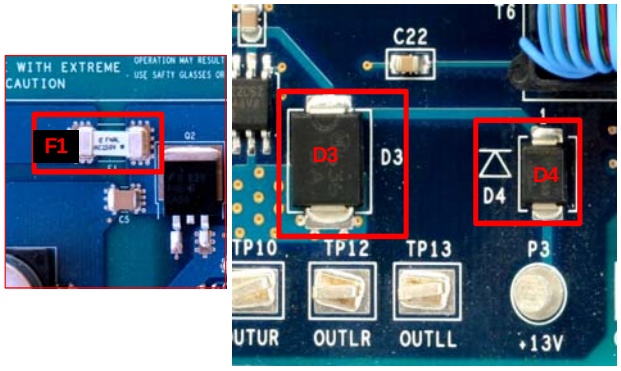


FIGURE 4. HIGH VOLTAGE PROTECTION CIRCUIT

Primary Side Current Sensing

The primary side bridge has 2 current sensing transformers (CT), one on each leg. Using two transformers allows each CT to reset during alternate half cycles. Alternative methods of current sensing using only one CT will also be covered.

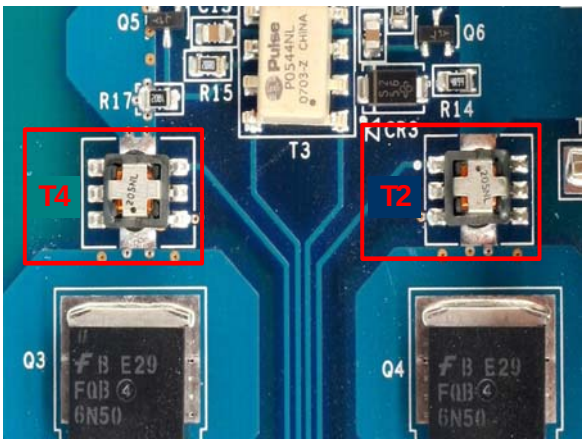


FIGURE 5. PRIMARY SIDE CURRENT SENSING CIRCUIT

Synchronous Rectifier Drive Circuit

Two banks of SRs, Q_{107} through Q_{110} and Q_{111} through Q_{114}, are driven by MOSFET drivers, U108 and U109. An RCD network on the inputs to the drivers delay the turn-on of the SRs relative to the turn-off of the primary side bridge

FETs. Pulse transformer, T_6, crosses the isolation boundary to couple the control signals from the ISL6752 to the MOSFET drivers. Note that this transformer also provides the secondary side bias voltage to the MOSFET drivers.

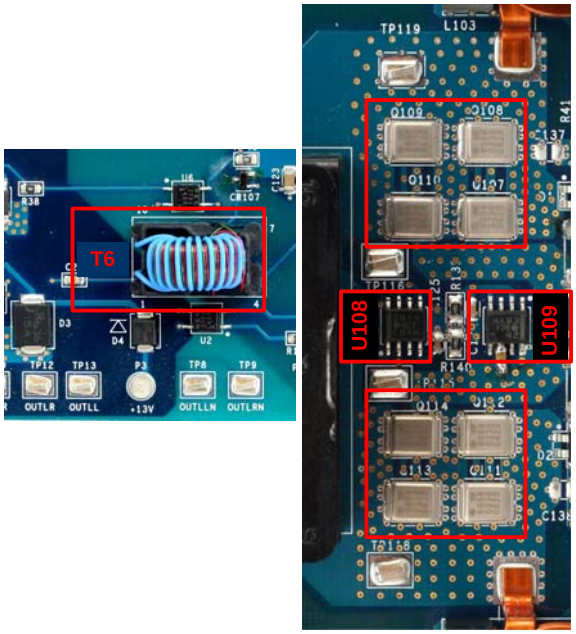


FIGURE 6. SYNCHRONOUS RECTIFIER DRIVE CIRCUIT

Current Doubler Output

The current doubler output is composed of two banks of SRs, Q_{107} through Q_{110} and Q_{111} through Q_{114}, inductors L_{102} and L_{103}, and output filter capacitors, C_{132} through C_{136}. The advantage of this topology is that the output current is shared by the two inductors reducing conduction losses. Another advantage is that the secondary winding of the power transformer does not require a center tap simplifying the construction of the transformer.

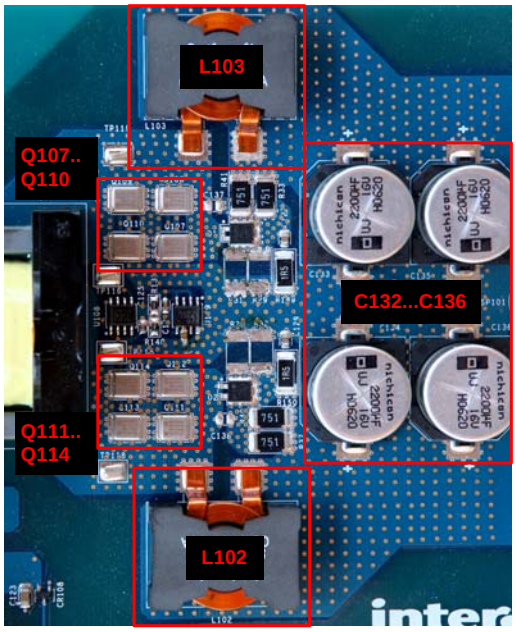


FIGURE 7. CURRENT DOUBLER OUTPUT CIRCUIT

Output Voltage Error Amplifier

A line isolation rated opto-coupler, U2, passes the analog error signal generated by the error amplifier, U102 from the secondary to the primary.

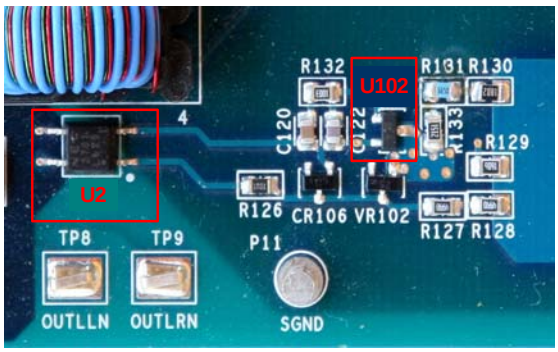


FIGURE 8. OUTPUT VOLTAGE ERROR AMPLIFIER CIRCUIT

Basic SR Principles

Replacing diodes with MOSFETs has two major advantages:

- dramatically reduces conduction losses
- the applied duty cycle remains virtually constant from no load to full load.

and two significant disadvantages:

- additional complexity and cost
- when paralleling units for redundancy, provisions must be made to prevent current circulation among the units.

SR Drive Timing Requirements

To emulate a diode, an SR must be driven on when a diode would be normally conducting. But unlike a diode, if the SR is on, the current through the SR can reverse if the voltage on the SR “cathode” becomes positive. The consequence of this is that if the SR is driven on when the primary side is sourcing voltage to the secondary, the secondary side will be shorted by the SR.

Figure 9 illustrates the timing required to drive the SRs. Note the delays to prevent the overlapping of the drive signals. When an SR is turned off when current is flowing from source to drain, the current will divert from the FET channel to the internal body diode. It is desirable to minimize the period that the current flows through the body diode to minimize dissipation.

SR Drive and Bias

OUTLLN and OUTLRN in Figure 10 are control signals from the ISL6752 that are used to drive the SRs. Because the ISL6752 is located on the primary side, a pulse transformer, T_6 is used to cross the isolation boundary. The simplified schematic of Figure 10 illustrates the use of T_6 to not only couple OUTLLN and OUTLRN to the secondary, but also to generate the bias for the drivers on the secondary.

When OUTLLN or OUTLRN transition to a logic high, it is necessary to turn off the SRs quickly. For example, when OUTLLN is high, V1 is positive relative to ground charging C_{125} quickly through CR108. U108 inverts the input and turns off SR1. In a similar manner, when OUTLLRN is high, U109 drives SR2 off.

When OUTLLN and OUTLRN transition to a logic low, it is necessary to turn on the SRs after a time delay to prevent the SRs from shorting the primary side bridge when it is sourcing current. For example, when OUTLLN transitions to low, V1 is grounded and CR108 prevents C_{125} from being discharged by V1. CR125 discharges instead through R_{140} delaying the transition of V2 from high to low on the input of U108. When V2 is low, the output of U108 drives SR1 on. In a similar manner, the transition of OUTLLRN from high to low is delayed to drive SR2 on.

Note that the cathodes of CR108 and CR107 are connected together to alternately peak charge C_{123}. Because C_{123} is large in value, after the initial charging, the voltage does not change significantly from cycle to cycle. An important aspect of generating the bias for U108 and U109 in this manner is that the thresholds for the logic transitions on the inputs of U108 and U109 are proportional to V_{BIAS} and the voltage to charge C_{125} and C_{124} is also V_{BIAS}. Consequently, the delays generated by the RC networks are independent of the absolute value of V_{BIAS}.

Current Doubler

Figure 11 illustrates the current flow in the two inductors of the current doubler topology. Color coding is used to correlate the current flow in the circuit with the waveforms. The green waveform represents the sum of the red and blue currents through R_{LOAD}. For circuit clarity, the paralleled SRs and output capacitors of the ISL6752EVAL1Z board are not shown.

When using diodes (instead of SRs), if the average load current is less than 1/2 of the ramp current in the output inductors, the current in the inductors becomes discontinuous and the duty cycle of the PWM is shortened to maintain the desired output voltage.

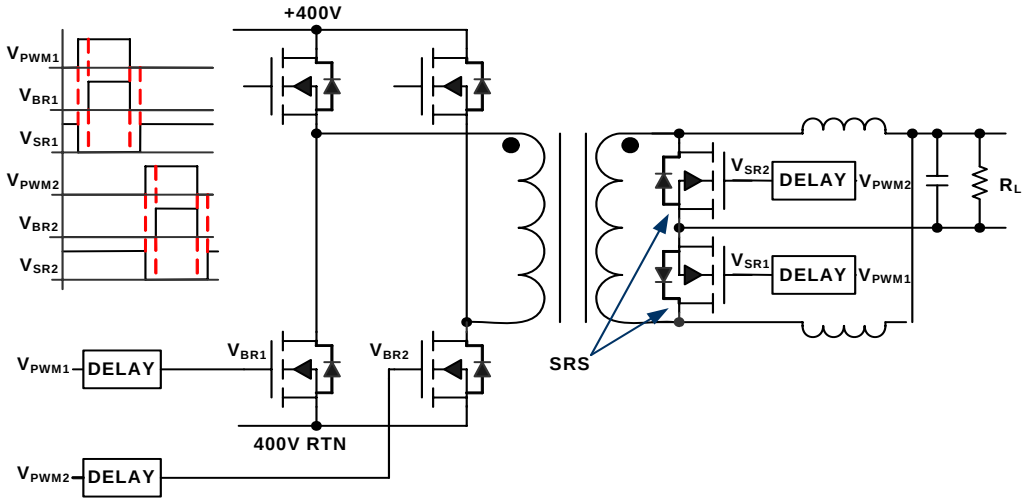


FIGURE 9. TIMING REQUIRED TO DRIVE SRs

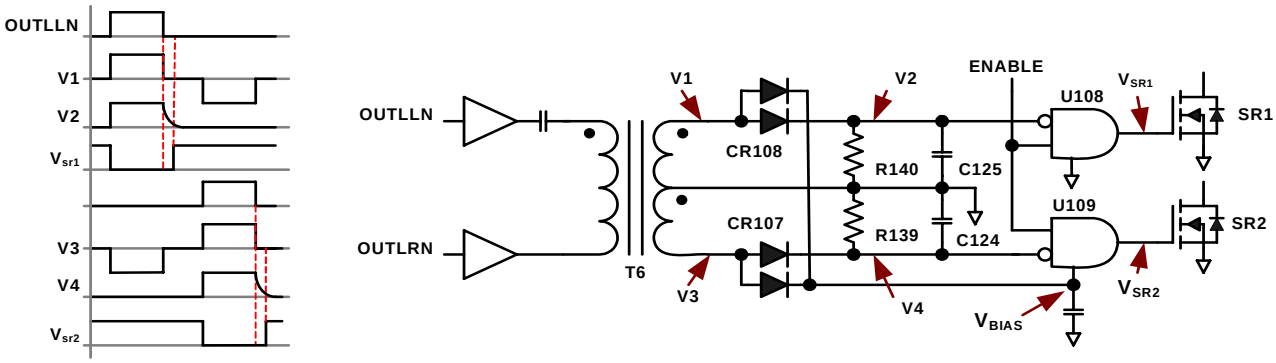


FIGURE 10. SIMPLIFIED SCHEMATIC

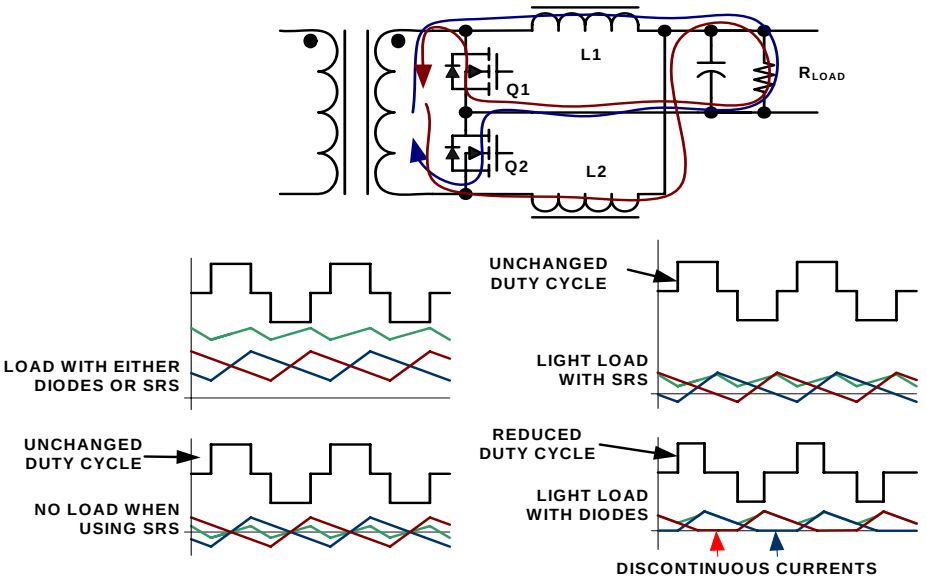


FIGURE 11. INDUCTOR FLOW IN TWO INDUCTORS OF CURRENT DOUBLER TOPOLOGY

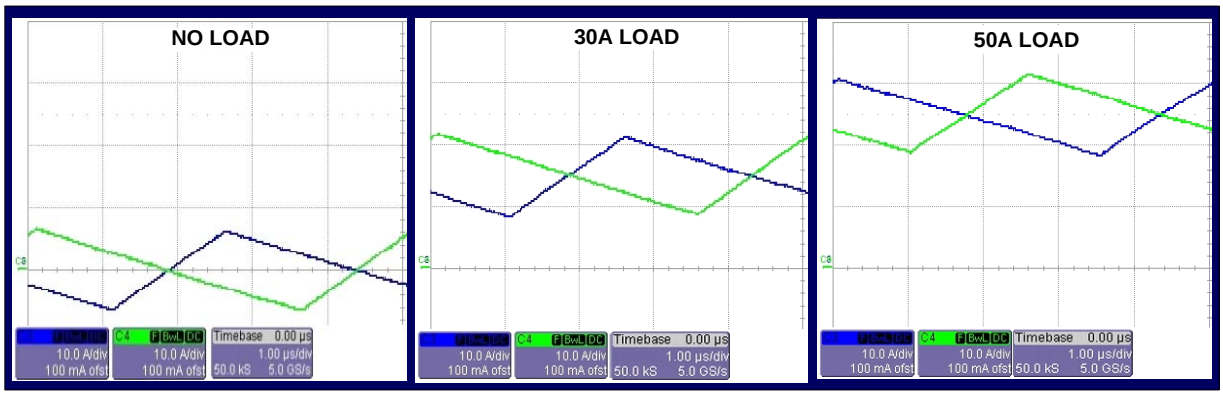


FIGURE 12. INDUCTOR CURRENT WAVEFORMS

When using SRs, the inductor currents in L_1 and L_2 can become negative because current can flow in SRs bidirectionally. Consequently, the duty cycle remains virtually unchanged. The benefit of this is that the load transient performance is the same for any load from zero up to current limit. Another advantage is that for very light loads, the duty cycle is not reduced to very small duty cycles, pulse skipping does not occur, and the associated voltage jitter does not happen.

An important design consideration for the current doubler topology is that the DC resistance of both halves must be equal. The pcb layout must be as symmetrical as possible and the DCRs of the inductors should also be reasonably equal. If not, the current between the two sides will not split equally. Because perfect physical pcb symmetry is not always possible, it is necessary to confirm the current sharing between the inductors.

In Figure 12, the inductor current waveforms are taken from the ISL6752EVAL1Z board. The balance of currents between the two inductors was achieved after two board revisions. Observe how the inductor currents maintain the same waveform shape even at no load.

Another design consideration when using SRs is the problem of connecting the outputs of multiple power supplies in parallel for redundancy or for increased power capacity. A consequence of negative current flowing in an SR (when a diode would otherwise be reversed biased and off) is that power can be transferred from the secondary to the primary if one of the paralleled outputs has a higher voltage. The voltage loop of the units with lower set point voltages will attempt to pull down the voltage by sinking current from the higher set point units. The primary side bridge capacitor is charged by the secondary side eventually resulting with excessive voltage damage. This damage can be avoided by using or-ing diodes (or FETs) on the paralleled outputs. Another solution is to turn off the SRs (diode emulation

mode) when the current reverses in the SRs but this eliminates some of the advantages of using SRs. Paralleling features are not implemented on the ISL6752EVAL1Z board.

Current Sensing

Current flowing from the secondary to the primary can result with an unanticipated malfunction of the current sensing transformer circuit if reverse SR currents are not considered. Figure 13 is a commonly used primary side current sensing circuit utilizing one current sensing transformer (CT).

This circuit works well for peak current mode control if power is always flowing from primary to secondary, as is the case when diodes are used instead of SRs. Figure 14 illustrates the performance of the current sensing output when power always flows from primary to secondary.

The voltage across R_S is as expected. The vertical dashed lines show when the power cycle is terminated at the required peak of the current.

Figure 15 illustrates what happens at no load to the sense voltage across R_S.

Notice that the negative components of the primary transformer current are rectified resulting with two peaks of current across R_S for each half cycle. Under steady state conditions, the rectified negative component may cause erratic performance because the cycle can terminate on the first peak (the inverted peak as indicated by the vertical red line) instead of the required second peak. This condition can easily be corrected by having a small load across the output to insure that the negative peak is always less than the positive.

However, a minimum load does not correct a more serious problem that occurs when there is a large load step from a heavy load to no load. When the load current is interrupted, the output capacitor charges higher than the regulated voltage. As the regulation loop is starting to respond by slewing to a minimum duty cycle, the excessive voltage on the output capactior starts to discharge back to the primary. This results with a large negative current at the beginning of the duty cycle, which causes the duty cycle to be terminated very early. The imbalance of the applied volt-seconds to the power transformer may saturate the power transformer and damage the power bridge.

Another scenario is that the current sensing transformer itself may saturate, which will also damage the bridge. The control loop cannot maintain balanced alternate half cycles applied to the power transformer without valid current sense information.

There are two solutions to this problem. Figure 16 illustrates the placements of two current sensing transformers, one on each drain leg of the bottom FETs.

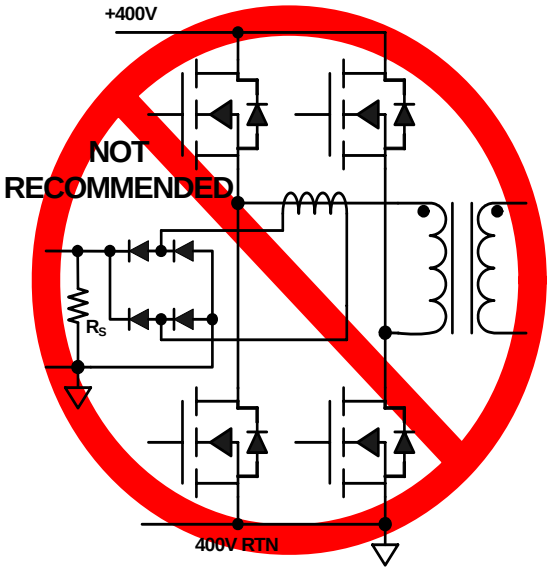


FIGURE 13. PRIMARY SIDE CURRENT SENSING CIRCUIT UTILIZING ONE CT

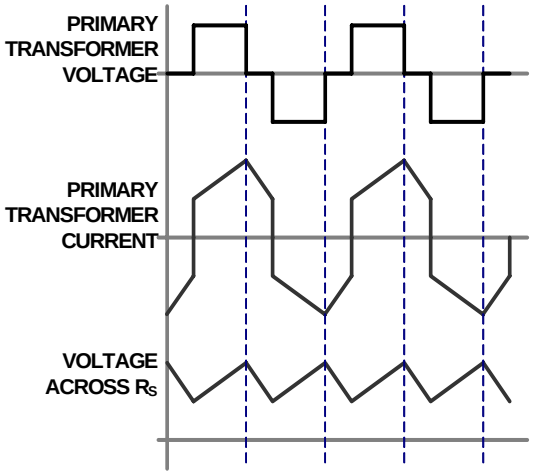


FIGURE 14. PERFORMANCE OF CURRENT SENSING OUTPUT

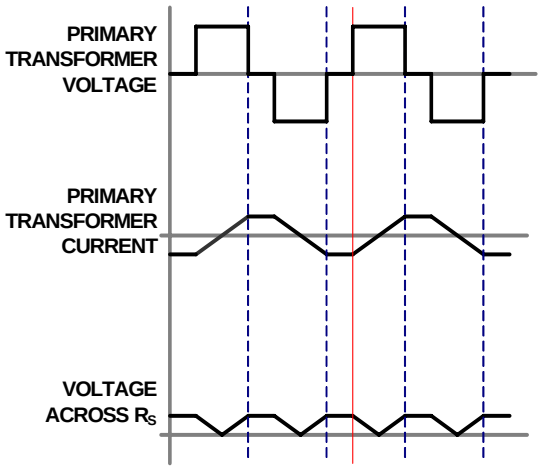


FIGURE 15. NO LOAD TO SENSE VOLTAGE ACROSS R_S

In this configuration, only positive current flowing into the drains of the bottom FETs are sensed across R_S solving the problem of rectified negative currents being impressed across R_S. An advantage of using two CTs is that there is a full half cycle available to reset the cores of the CTs. This is the solution used in the ISL6752EVAL1Z board.

Figure 17 is the current sense waveform as seen on SP1 of the ISL6752EVAL1Z board with an output load of 60A.

Figure 18 shows a different current sensing implementation that also solves the problem of Figure 13.

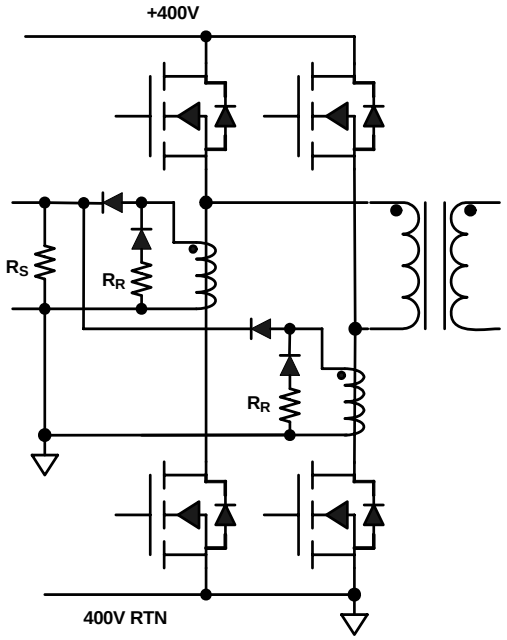


FIGURE 16. PLACEMENT OF TWO CURRENT SENSING TRANSFORMERS

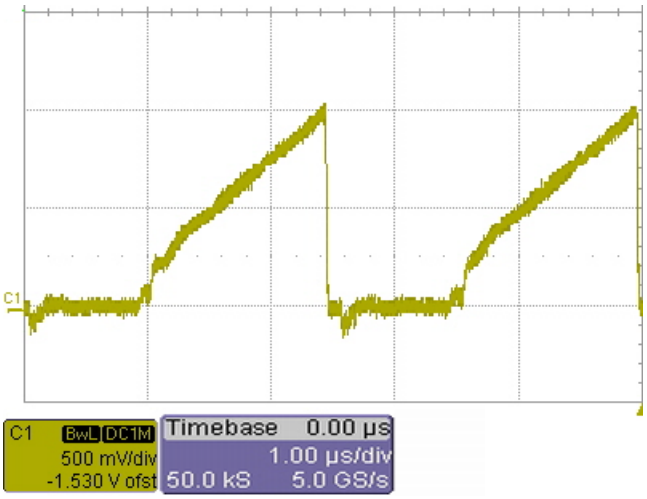


FIGURE 17. CURRENT SENSE WAVEFORM AT SP1 OF ISL6752EVAL1Z BOARD

In this example, both drain currents of the bottom FETs are sensed by only one CT. But there are some limitations that must be considered. To reset the core, the minimum time available is the duration of the selected dead time between the two FETs on the same side of the bridge. This dead time can be made longer to accommodate the resetting of the CT but the consequences of reducing the maximum duty cycle available for output voltage regulation must be considered.

If the dead time is kept short, then the peak voltage required for resetting the core will be relatively large. For example, assume that the dead time is selected to be 2% of the duty cycle. The worst case reset voltage is then approximately shown in Equation 1:

$$(0.98/0.02) \bullet V_{SMAX} = 49V \quad \text{(EQ. 1)}$$

where V_{SMAX} is 1V (the current limit voltage of the ISL6752).

Notice in Figure 18 that the 400V RTN is slightly more negative than the signal ground. This is recommended for applications that directly drive the bottom FETs with MOSFET drivers. If the 400V RTN and the MOSFET drivers are grounded, regenerative feedback will be present on the output of the MOSFET drivers because of the presence of the CT windings in the gate drive loop.

A variation of the current sense circuit of Figure 18 is to place the current sensing transformer in the common drain lead of the two high side FETs, as shown in Figure 19.

The circuits of Figures 18 and 19 give exactly the same performance, but the problem associated with the gate drives (as explained in Figure 18) is avoided. The disadvantage of placing the CT at this location is that the CT must be designed with 400VDC operational insulation.

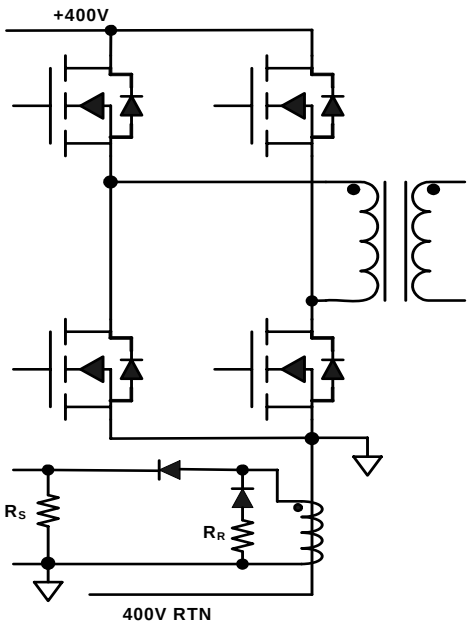


FIGURE 18. CURRENT SENSING TRANSFORMERS

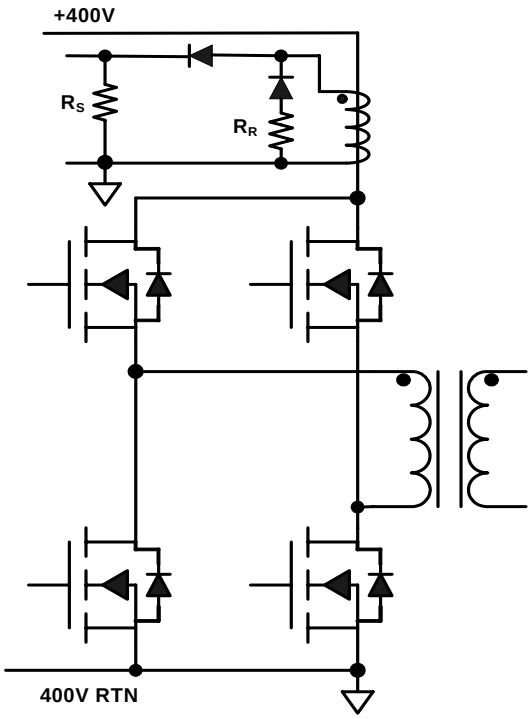


FIGURE 19. CURRENT SENSING TRANSFORMERS IN THE COMMON DRAIN LEAD

Conclusion

This application note investigates the use of MOSFETs as synchronous rectifiers to replace conventional diodes. The advantanges of improved power efficiency and load transient are reviewed along with implemention problems that must be solved.

References

[1] Fred Greenfeld, Intersil Application Note AN1246, “Techniques to Improve ZVS Full-bridge Performance”

[2]Fred Greenfeld, Intersil Application Note AN1262, “Designing with the ISL6752, ISL6753 ZVS Full-bridge Controllers”

Appendix

The following sections cover the set-up of the ISL6752EVAL1Z board. Also included are the bill of materials, schematic, measured waveforms, parameters and pcb layout.

Setting Up

Danger

-This evaluation unit should be used and operated only by persons experienced and knowledgeable in the design and operation of high voltage power conversion equipment.

-Use of this evaluation unit constitutes acceptance of all risk inherent in the operation of equipment having accessible hazardous voltage. Careless operation may result in serious injury or death.

-Use safety glasses or other suitable eye protection.

Lab equipment required:

- DC lab power supply, 13VDC @ 200mA minimum
- 400VDC regulated lab power supply, 2.5ADC min with current limit
- Fan to cool heatsinks
- Oscilloscope, digital preferred with 4 channels, 20MHz minimum bandwidth
- DC load, 80A min, >750W
- DC Mulitmeter

Connect the DC load to the output of the evaluation board. Terminal P102 is negative and terminal P104 is positive. Adjust the load to zero. With both supplies turned off, connect the 13VDC supply to +13V (P3) and PGND (P4). Connect the 400V supply to +400V (P1) and 400V RTN (P2). Turn on the 13V supply and adjust the current limit to 200mA. Adjust the voltage to +13.0VDC. The lab supply current should be approximately 125mA.

Caution

A voltage clamp, D3, is used to protect the primary side control circuit from catastrophic damage should the high voltage bridge fail. In order to prevent this clamp from conducting, do not adjust the 13VDC lab supply over 13.5VDC.

Turn on the 400V supply and adjust the current limit to 2.5A. Adjust the voltage to 400VDC. Do not exceed 450VDC! The current should be approximately 45mA. Turn on the fan and direct the air flow through the heatsinks mounted on the bottom of the board. Using TP120 and TP121, the output voltage should be 12 ±0.5VDC.

The output load and input voltage can now be safely adjusted. Because there is no thermal shut down circuit, it is important to maintain adequate airflow over the heatsinks, especially when applying large loads.

Waveforms

In Figure 20, the Drain-Source voltage of the low side FETs is displayed relative to the gate voltage to highlight the ZVS performance of the bridge. The load is at the rated 50A. Notice that full ZVS is not achieved because the minimum resonance voltage is about 160VDC. Even though this not is an optimum design, 85% of the switching losses are still recovered. To improve the ZVS performance, a future version of a ZVS topology evaluation board will use FETs with less body capacitance to achieve optimum ZVS. Alternatively, improvements to the ZVS performance can be made by increasing the leakage inductance of the transformer or by using saturable inductor snubbers for the output SRs. For more information, see application note AN1246, “Techniques to Improve ZVS Full-bridge Performance.”

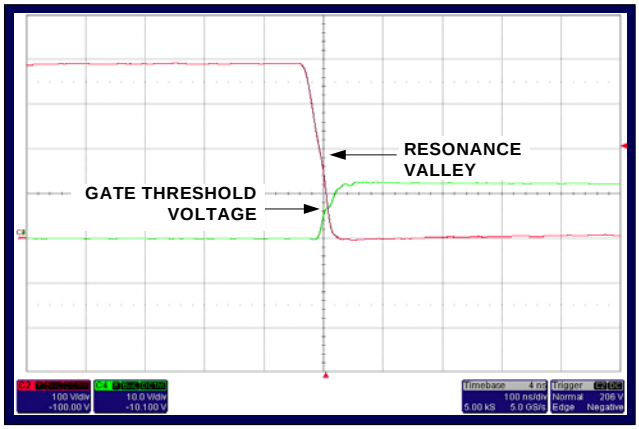


FIGURE 20. DRAIN SOURCE VOLTAGE OF THE LOW SIDE FET

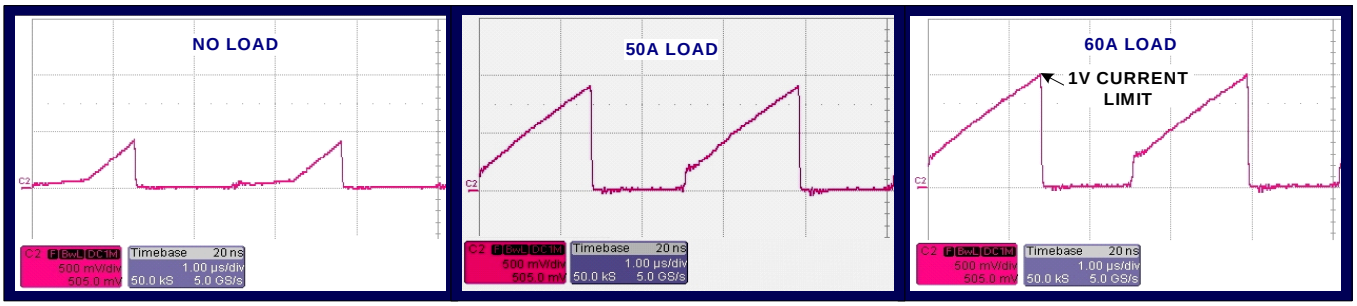


FIGURE 21. CURRENT SENSE VOLTAGE ON SP1 AT NO LOAD, 50A AND 60A (CURRENT LIMIT)

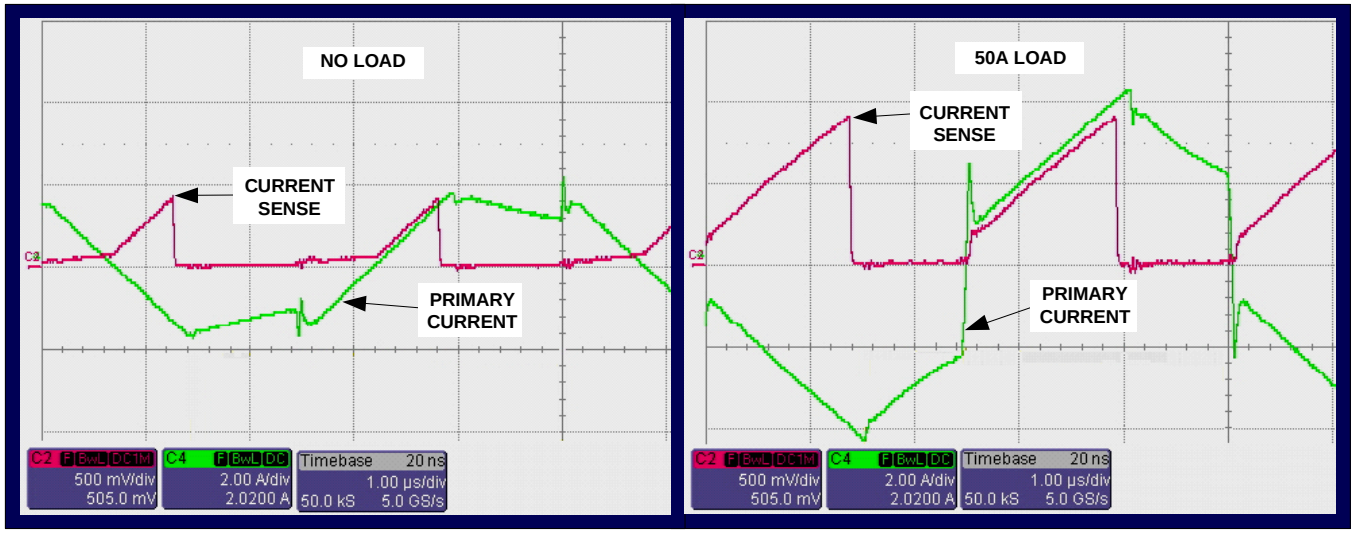


FIGURE 22. PRIMARY TRANSFORMER CURRENT

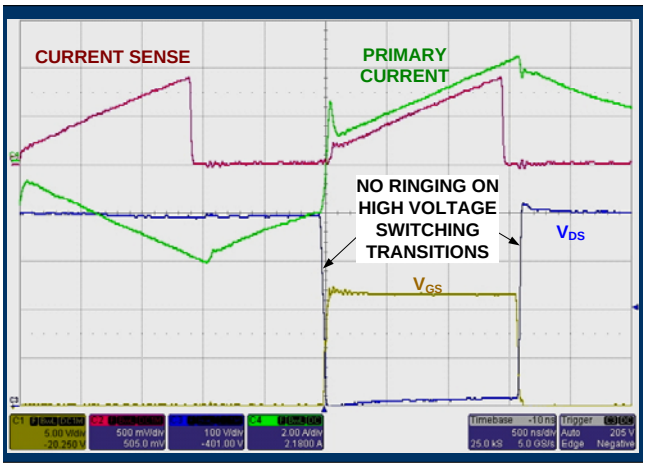


FIGURE 23. PRIMARY GATE DRIVE AND HIGH VOLTAGE SWITCHING ON BOTTOM BRIDGE FETS

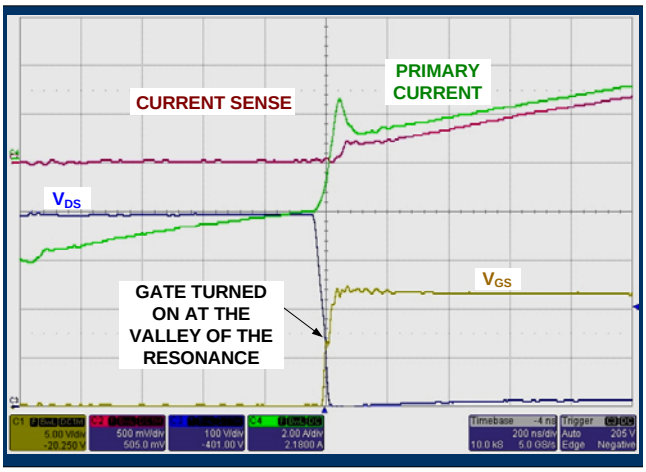


FIGURE 24. PRIMARY GATE DRIVE AND HIGH VOLTAGE SWITCHING ON BOTTOM BRIDGE FETS (EXPANDED SWEEP)

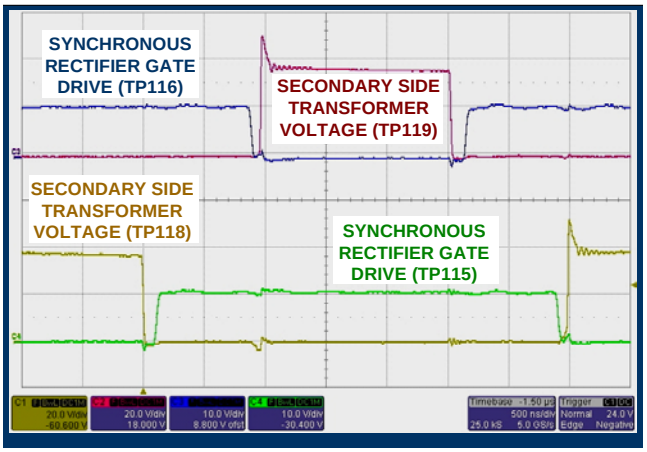


FIGURE 25. SECONDARY TRANSFORMER VOLTAGE AND SYNCHRONOUS GATE DRIVE VOLTAGE

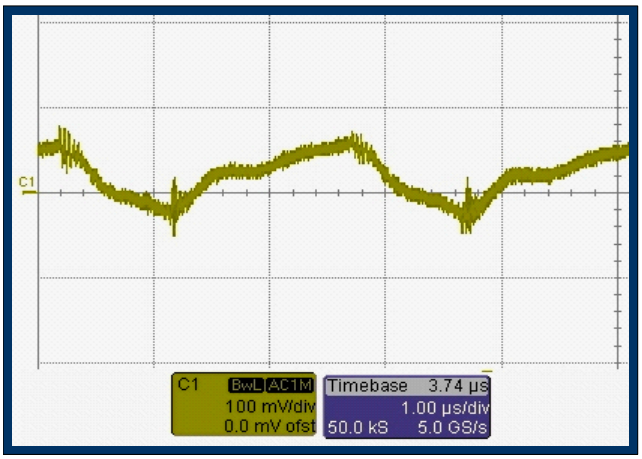


FIGURE 26. OUTPUT VOLTAGE RIPPLE, 20MHZ (SP101)

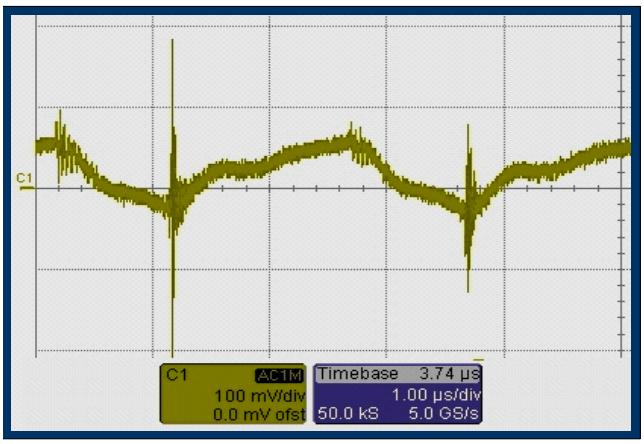


FIGURE 27. OUTPUT VOLTAGE RIPPLE AND NOISE, 1GHZ (SP101)

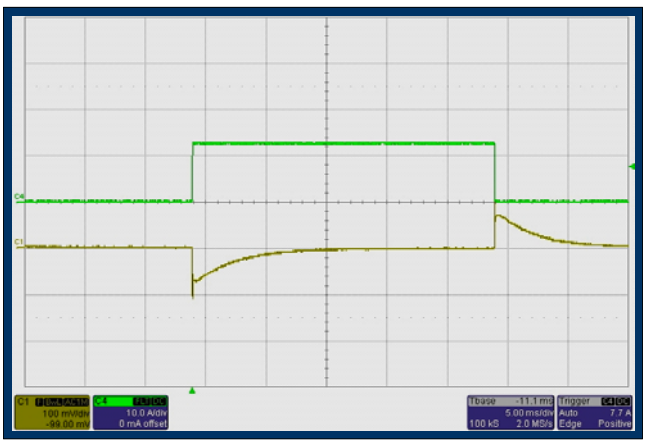


FIGURE 28. OUTPUT LOAD TRANSIENT, 0A TO 12A

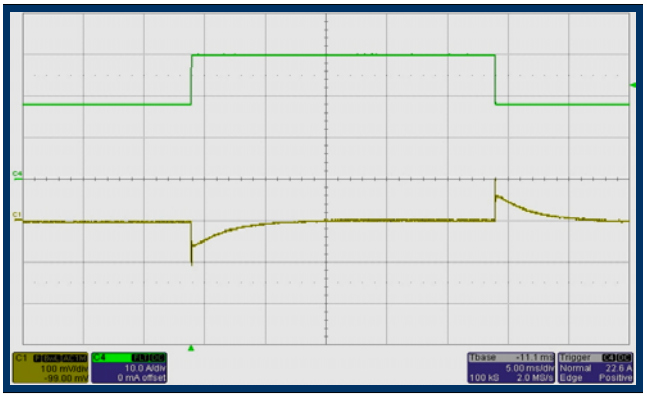


FIGURE 29. OUTPUT LOAD TRANSIENT, 12A TO 30A

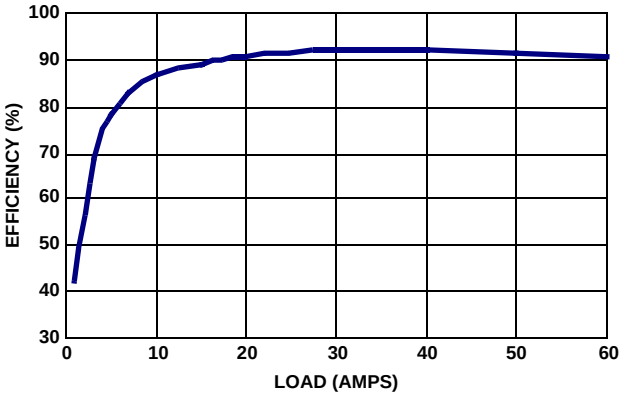


FIGURE 30. EFFICIENCY

TABLE 2. LINE AND LOAD REGULATION

V_{IN}	V_{OUT} AT NO LOAD	V_{OUT} AT 25A LOAD	V_{OUT} at 50A LOAD
425	11.833	11.783	11.763
400	11.845	11.799	11.773
375	11.849	11.808	11.779
350	11.852	11.815	11.784
325	11.856	11.821	11.787

References

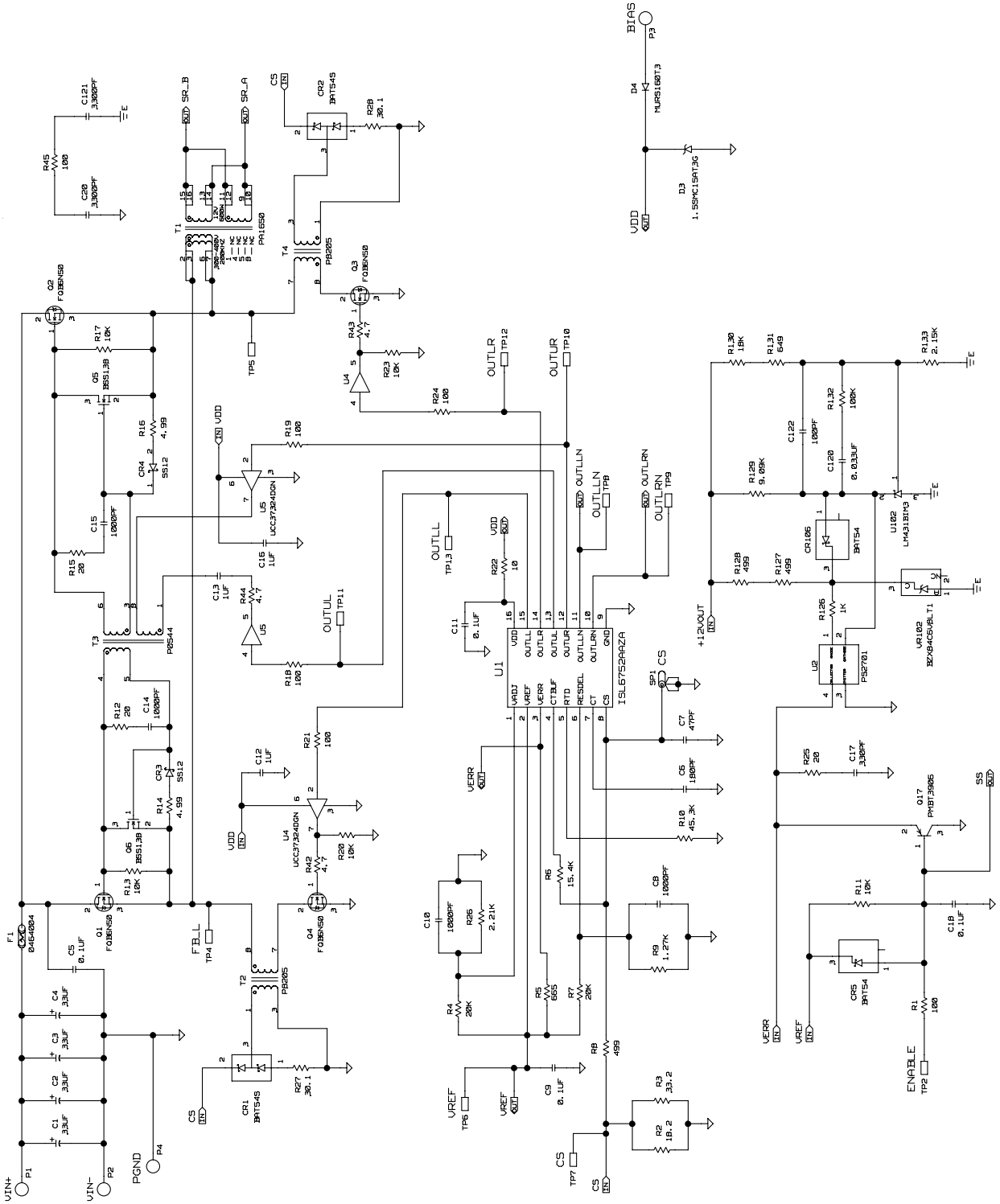
[1] Fred Greenfeld, Intersil Application Note AN1246, “Techniques to Improve ZVS Full-bridge Performance”

[2]Fred Greenfeld, Intersil Application Note AN1262, “Designing with the ISL6752, ISL6753 Full-Bridge Controllers”

TABLE 3. EFFICIENCY

V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	EFFICIENCY (%)	POWER	RATED POWER
400	0.07	11.84	1	41	12	2
400	0.13	11.83	3	67	35	6
400	0.19	11.82	5	77	59	10
400	0.25	11.82	5	77	59	10
400	0.35	11.80	10	86	118	20
400	0.50	11.79	15	89	177	29
400	0.66	11.79	20	90	236	39
400	0.97	11.78	30	91	353	59
400	1.29	11.77	40	92	471	78
400	1.61	11.76	50	91	588	98
400	1.95	11.75	60	91	705	118

ISL6752EVAL1Z Schematic



ISL6752EVAL1Z Schematic (Continued)

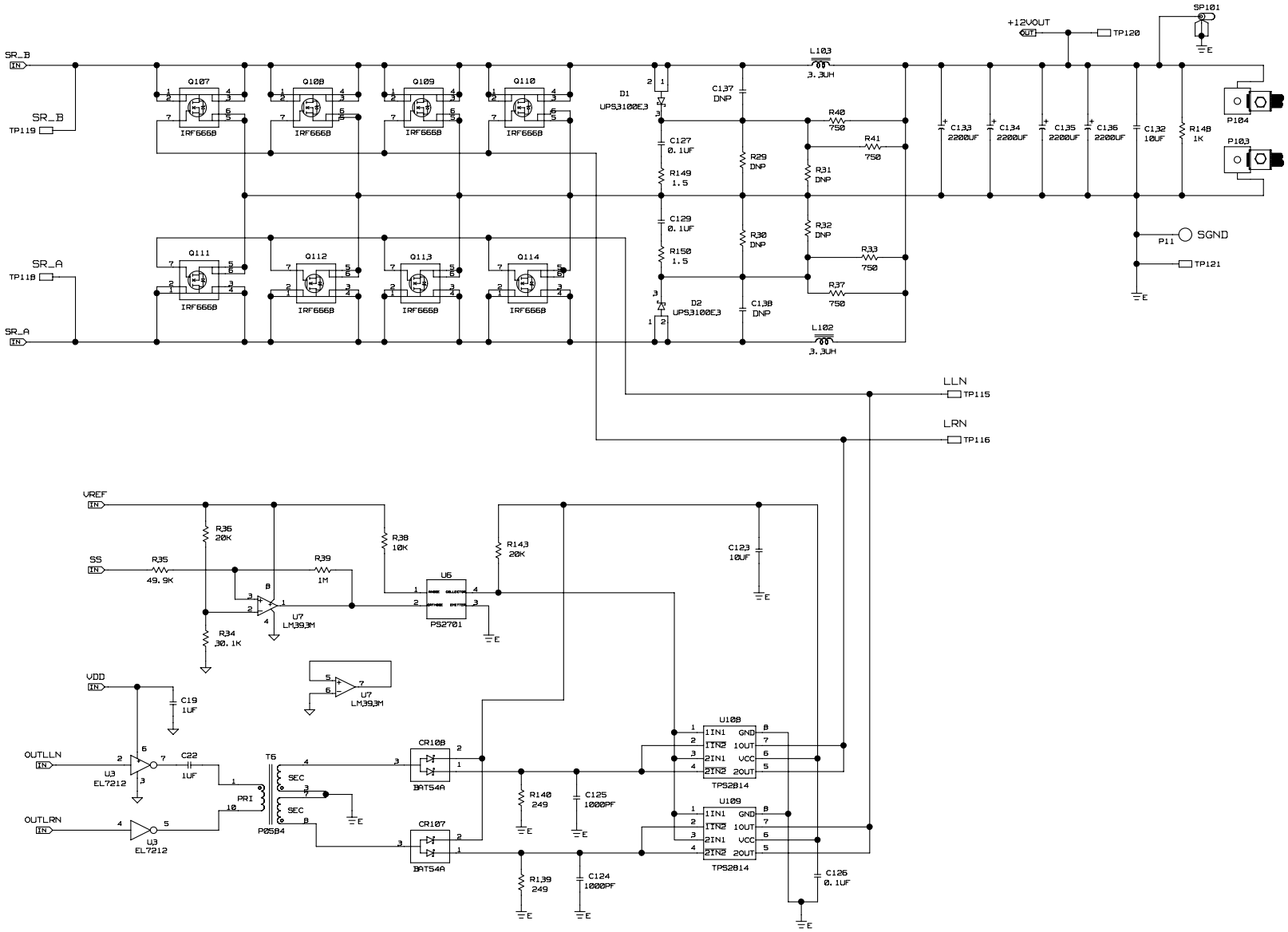


TABLE 4. ISL6752EVAL1Z BILL OF MATERIALS

PART NUMBER	REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	MANUFACTURER	DESCRIPTION
464004	F1	1	4.0A		250V	SMD	LITTELFUSE	NANO2 UMF Fast-Acting Fuse
08053D105KAT2A	C12, C13, C16, C19, C22	5	1µF	10%	25V	805	AVX	Multilayer Capacitor
1.5SMC15AT3G	D3	1				SMC	ON-SEMI	15V 1500W Transient Voltage Suppressor
131-4353-00	SP1, SP101	2				CONN	TEKTRONIX	Scope Probe Test Point PCB Mount
1514-2	P1 to P4, P11	5				THOLE	KEYSTONE	Test Point Turret 0.150 Pad 0.100 Thole
5016	TP2,TP4 to TP13,TP115, TP116, TP118 to TP121	17				SMT	KEYSTONE	Compact Surface Mount Test Point Pad
BAT54	CR5, CR106	2				SOT-23	DIODES	30V Schottky Diode
BAT54A	CR107, CR108	2				SOT-23	DIODES	30V Schottky Diode
BAT54S	CR1, CR2	2				SOT-23	DIODES	Schottky Barrier (Double) Diode
BSS138LT1	Q5, Q6	2				SOT-23	ON-SEMI	200mA 50V N-Channel Power MOSFET
BZX84C6V8LT1	VR102	1				SOT-23	ON-SEMI	6.8V 225mW Zener Voltage Regulator
C1608COG2A331J	C17	1	330pF	5%	100V	603	TDK	Multilayer Capacitor
C2012COG1H470K	C7	1	47pF	10%	50V	805	TDK	Multilayer Capacitor
C2012COG2A181J	C6	1	180pF	5%	100V	805	TDK	Multilayer Capacitor
C2012X7R2A102K	C8, C10, C14, C15	4	1000pF	10%	100V	805	TDK	Multilayer Capacitor
C4532X7R2J104K	C5	1	0.1µF	10%	630V	1812	TDK	Multilayer Capacitor
EL7212CS	U3	1				SOIC	INTERSIL	HS Dual Channel Power MOSFET Driver
ERJ6ENF3012	R34	1	30.1k	1%		805	PANASONIC	Precision Thick Film Chip Resistor
ERJ6ENF4R99	R14, R16	2	4.99	1%		805	PANASONIC	Precision Thick Film Chip Resistor
FQB6N50	Q1 to Q4	4				D2PAK	FAIRCHILD	500V N-Channel MOSFET
GA355QR7GF332KW01L	C20, C121	2	3300pF	10%	250V	2220	MURATA	Chip Monolithic Capacitor
	C124, C125	2	1000pF	10%	100V	603	GENERIC	Multilayer Capacitor
	C126	1	0.1µF	10%	25V	603	GENERIC	Multilayer Capacitor
	C122	1	100pF	5%	50V	805	GENERIC	Multilayer Capacitor
	C9, C11, C18	3	0.1µF	10%	100V	805	GENERIC	Multilayer Capacitor
	C127, C129	2	0.1µF	10%	100V	805	GENERIC	Multilayer Capacitor
	C120	1	0.033µF	10%	50V	805	GENERIC	Multilayer Capacitor
	C137, C138	2	DNP	5%	DNP	805	GENERIC	Multilayer Capacitor (DNP)
	C123	1	10µF	20%	25V	1206	GENERIC	Multilayer Capacitor
	C132	1	10µF	20%	25V	1206	GENERIC	Multilayer Capacitor

TABLE 4. ISL6752EVAL1Z BILL OF MATERIALS (Continued)

PART NUMBER	REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	MANUFACTURER	DESCRIPTION
	R130	1	18k	0.10%		805	GENERIC	Metal Film Chip Resistor
	R22	1	10	1%		805	GENERIC	Thick Film Chip Resistor
	R12, R15, R25	3	20	1%		805	GENERIC	Thick Film Chip Resistor
	R42 to R44	3	4.7	1%		805	GENERIC	Thick Film Chip Resistor
	R1, R18, R19, R21, R24	5	100	1%		805	GENERIC	Thick Film Chip Resistor
	R126	1	1k	1%		805	GENERIC	Thick Film Chip Resistor
	R11, R13, R17, R20, R23, R38	6	10k	1%		805	GENERIC	Thick Film Chip Resistor
	R132	1	100k	1%		805	GENERIC	Thick Film Chip Resistor
	R39	1	1M	1%		805	GENERIC	Thick Film Chip Resistor
	R9	1	1.27k	1%		805	GENERIC	Thick Film Chip Resistor
	R6	1	15.4k	1%		805	GENERIC	Thick Film Chip Resistor
	R2	1	18.2	1%		805	GENERIC	Thick Film Chip Resistor
	R4, R7, R36, R143	4	20k	1%		805	GENERIC	Thick Film Chip Resistor
	R133	1	2.15k	1%		805	GENERIC	Thick Film Chip Resistor
	R26	1	2.21k	1%		805	GENERIC	Thick Film Chip Resistor
	R139, R140	2	249	1%		805	GENERIC	Thick Film Chip Resistor
	R27, R28	2	30.1	1%		805	GENERIC	Thick Film Chip Resistor
	R3	1	33.2	1%		805	GENERIC	Thick Film Chip Resistor
	R10	1	45.3k	1%		805	GENERIC	Thick Film Chip Resistor
	R8, R127, R128	3	499	1%		805	GENERIC	Thick Film Chip Resistor
	R35	1	49.9k	1%		805	GENERIC	Thick Film Chip Resistor
	R131	1	649	1%		805	GENERIC	Thick Film Chip Resistor
	R5	1	665	1%		805	GENERIC	Thick Film Chip Resistor
	R129	1	9.09k	1%		805	GENERIC	Thick Film Chip Resistor
	R45	1	100	1%		1206	GENERIC	Thick Film Chip Resistor
	R148	1	1k	1%		1206	GENERIC	Thick Film Chip Resistor
	R149, R150	2	1.5	1%		2512	GENERIC	Thick Film Chip Resistor
	R33, R37, R40, R41	4	750	5%		2512	GENERIC	Thick Film Chip Resistor
	R29 to R32	4	DNP	1%		2512	GENERIC	Thick Film Chip Resistor (DNP)
IRF6668	Q107 to Q114	8				FET	IR	DIRECTFET Power MOSFET
ISL6752AAZA	U1	1				SSOP	INTERSIL	ZVS Full-Bridge Current-Mode Controller
KPA8CTP	P103, P104	2				CONN	BURNDY	Wire Connector Lug
LM393M	U7	1				ALL	NATIONAL	Low Power Low Offset Voltage Dual Comparator

TABLE 4. ISL6752EVAL1Z BILL OF MATERIALS (Continued)

PART NUMBER	REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	MANUFACTURER	DESCRIPTION
LMV431AIMF	U102	1				SOT23	NATIONAL	Low-Voltage (1.24V) Adjustable Shunt Regulator
MURS160T3	D4	1				SMB	ON-SEMI	Ultrafast Power Rectifier
P0544	T3	1				SMD	PULSE	Gate Drive Transformer
P0584	T6	1				SMD	PULSE	Offline Gate Drive Transformers
P8205	T2, T4	2				SMD	PULSE	Smt Current Sense Transformer
PA1650	T1	1				SMD	PULSE	Full Bridge Transformer
PMBT3906	Q17	1				SOT	Philips	-40V 200mA PNP Switching Transistor
PS2701-1	U2, U6	2				SOP	NEC	High Isolation SOP Multi Photocoupler
SER2814L-332KL	L102, L103	2	3.3µH			SMD	CoilCraft	Power Inductor High Current
SS12T3	CR3, CR4	2				SMA	ON-SEMI	1A 20V SCHOTTKY POWER RECTIFIER
TPS2814D	U108, U109	2				SOIC	TI	Dual High-speed MOSFET Driver
UCC37324DGN	U4, U5	2				MSOP	TI	Dual 4 Power Driver
UPS3100E3	D1, D2	2				POWER	DIODES	3A High Voltage Schottky Rectifier
UUG1C222MNR1MS	C133 to C136	4	2200µF	20%	16V	SMD	NICHICON	Aluminum Electrolytic Capacitor
UUG2W330MNR1ZD	C1 to C4	4	33µF	20%	450V	SMD	NICHICON	Aluminum Electrolytic Capacitor

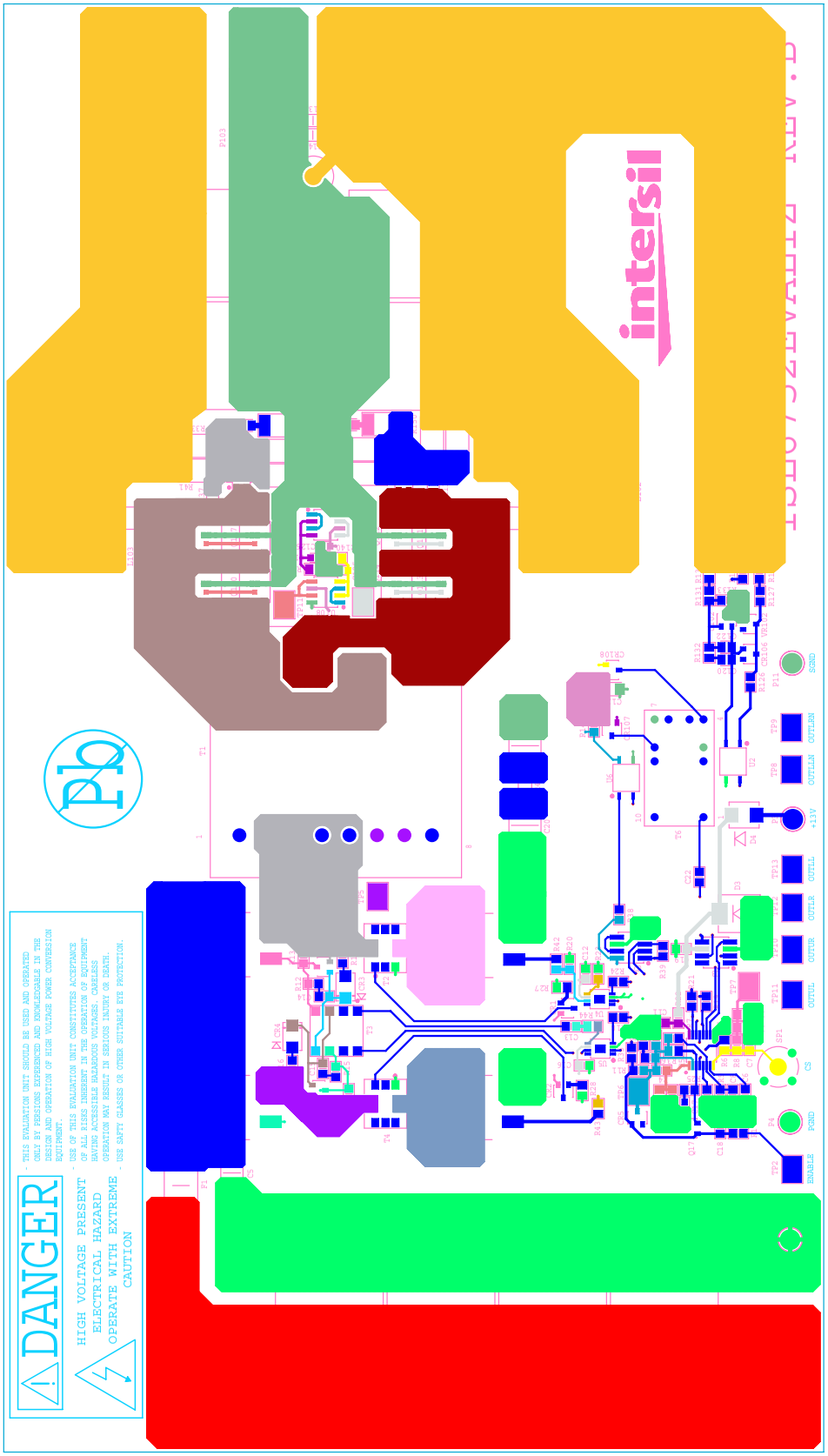


FIGURE 31. LAYER 1, TOP

ISL6752EVAL1Z Layout

ISL6752EVAL1Z Layout (Continued)

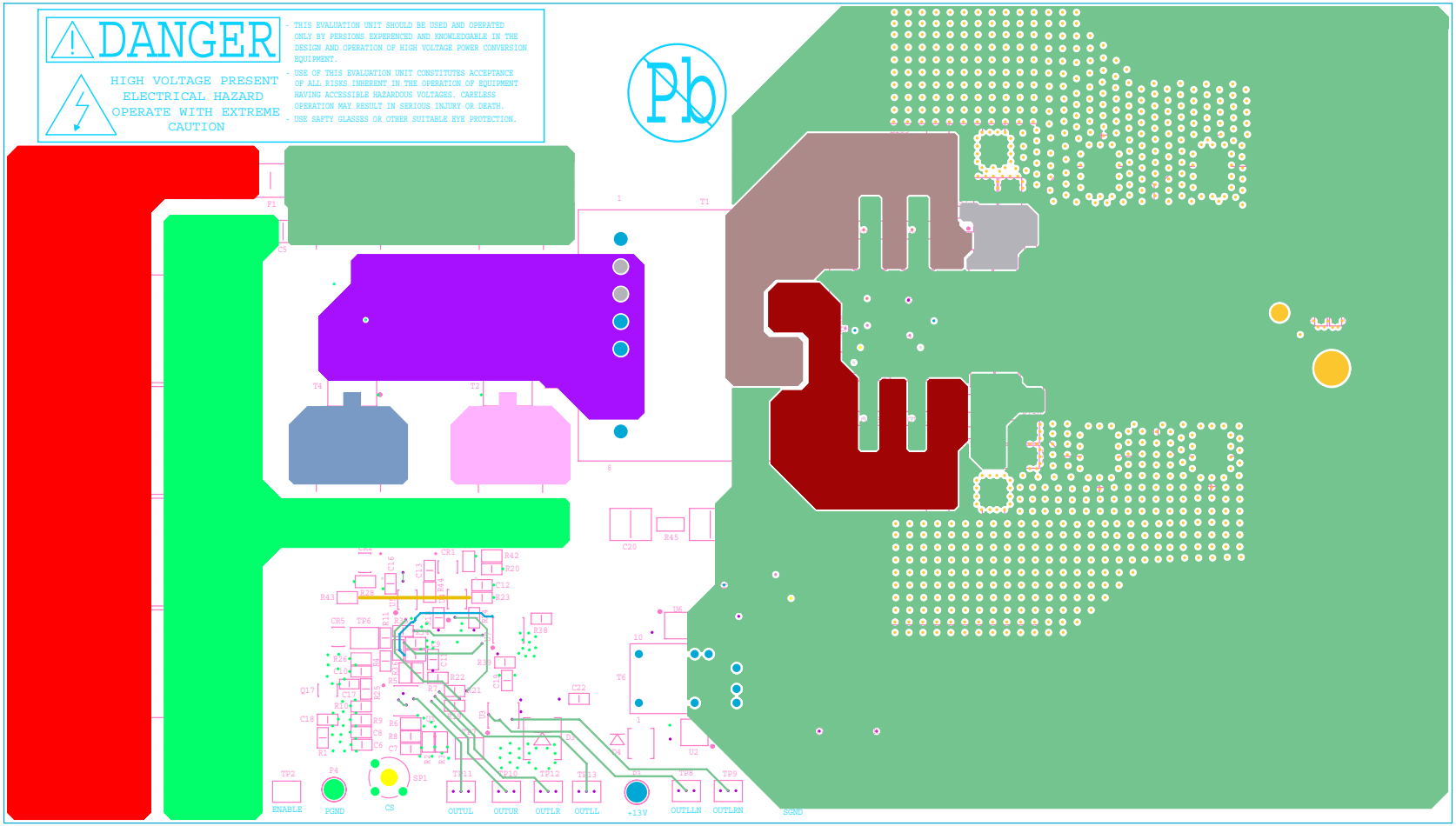


FIGURE 32. LAYER 2

ISL6752EVAL1Z Layout (Continued)

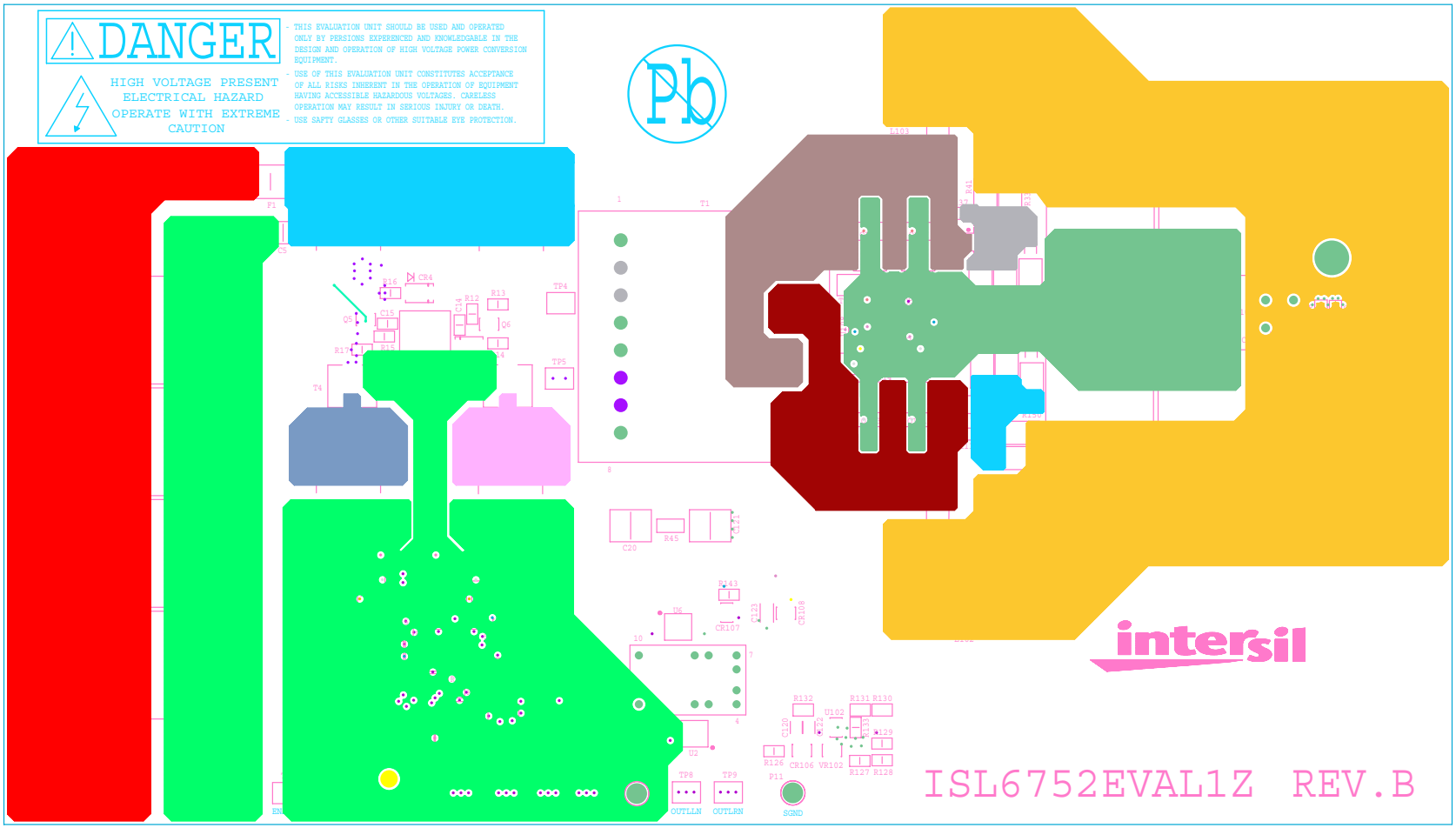


FIGURE 33. LAYER 3

ISL6752EVAL1Z Layout (Continued)

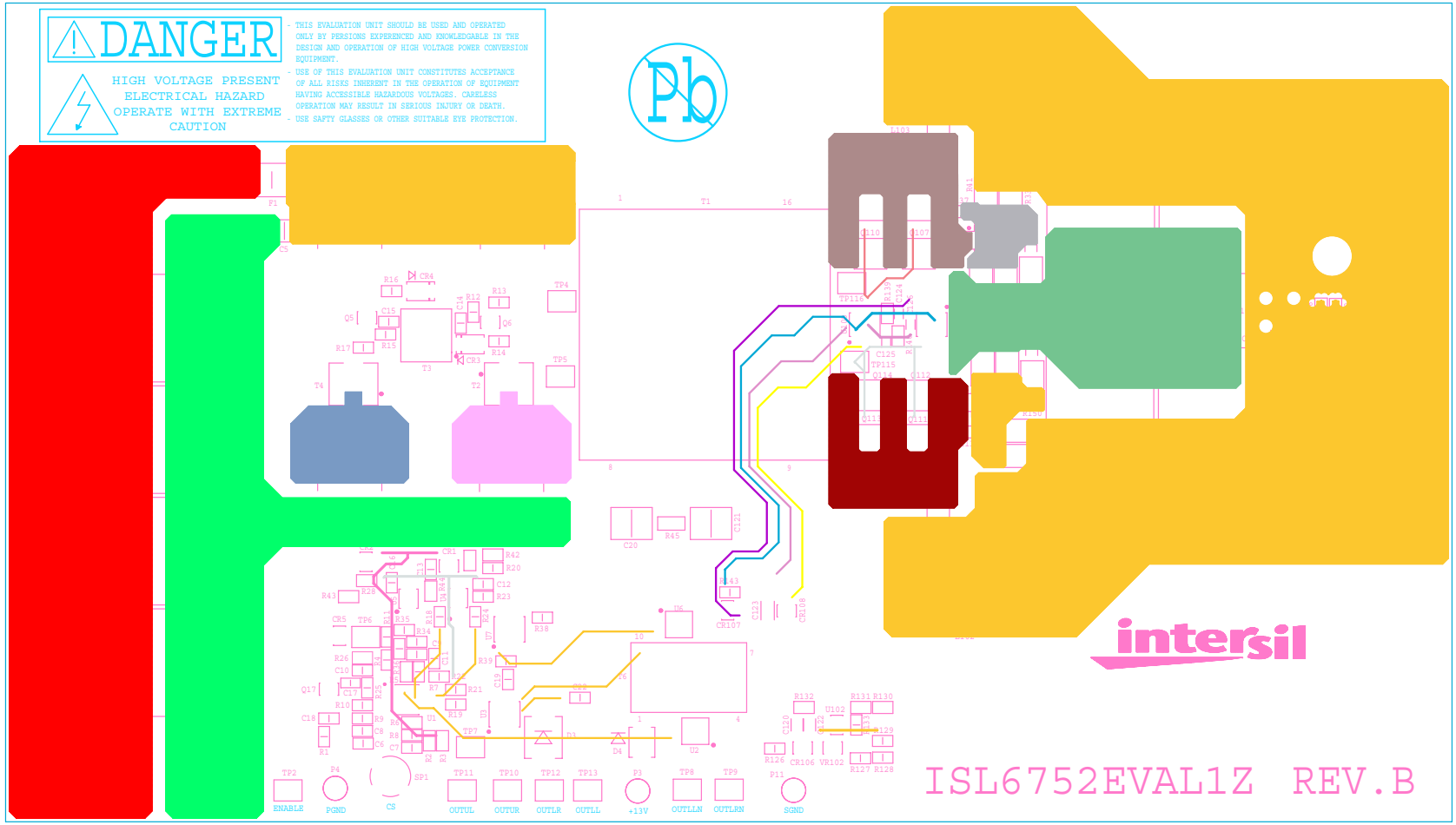


FIGURE 34. LAYER 4, BOTTOM