RAA23040x

3-ch Step-Down Switching Regulator + 1-ch LDO

R18DS0004EJ0102
Rev.1.02
Jul.09, 2013

Description

The RAA23040x is a power supply IC that has 3-ch step-down Switching Regulator containing power MOSFETs and 1-ch LDO.

Features

- Switching Regulator (ch1, ch3, ch4)
  - Synchronous rectification type step-down circuit
  - Integrated power MOSFETs
  - Internal phase compensator
  - Power good function (ch1)
  - Low power mode
    (ch1, ch3 and ch4 operate at low frequency and reduce the power consumption of the IC.)
  - Switching frequency: 1.3 MHz to 2 MHz (variable)
  - Internal timer-latch-type short-circuit protector
- LDO (ch2)
  - Internal over current protector (foldback-current limiting)
- Common part
  - Independent On/Off control for each channel
  - Internal digital soft-start function (adjustable soft-start time)
  - Internal discharge circuit
  - Internal timer-latch-type thermal shutdown circuit (shutdown temperature: 150°C or higher)
  - Internal recovery-type under voltage lockout circuit

PKG and Packing

Part No.	Package	Packing
RAA23040xGNP	32-pin VQFN	Embossed taping. 4,000pcs/reel
RAA23040xGFT	32-pin TQFP	Tray. 1,250pcs/Inner box

Product Lineup Table

The following 9 products are developed based on output voltage.

ch	RAA230401	RAA230402	RAA230403	RAA230404	RAA230405	RAA230406	RAA230407	RAA230408	RAA230409
1	1.8 V	2.5 V	3.0 V	3.3 V	1.8 V	2.5 V	3.0 V	3.3 V	Adjustable
2									
3	3.3 V				Adjustable				
4	Output voltage is selectable. 1.2 V preset voltage by internal resistor or adjustable by external resistor.								

Note: ch1, ch2: RAA230401 to RAA230408 output preset voltage by internal resistor. RAA230409 outputs adjustable voltage by external resistor.

ch3: RAA230401 to RAA230404 output preset voltage by internal resistor. RAA230405 to RAA230409 output adjustable voltage by external resistor.

ch4: All products have switchable output voltage between 1.2 V preset voltage by internal resistor and adjustable voltage by external resistor.

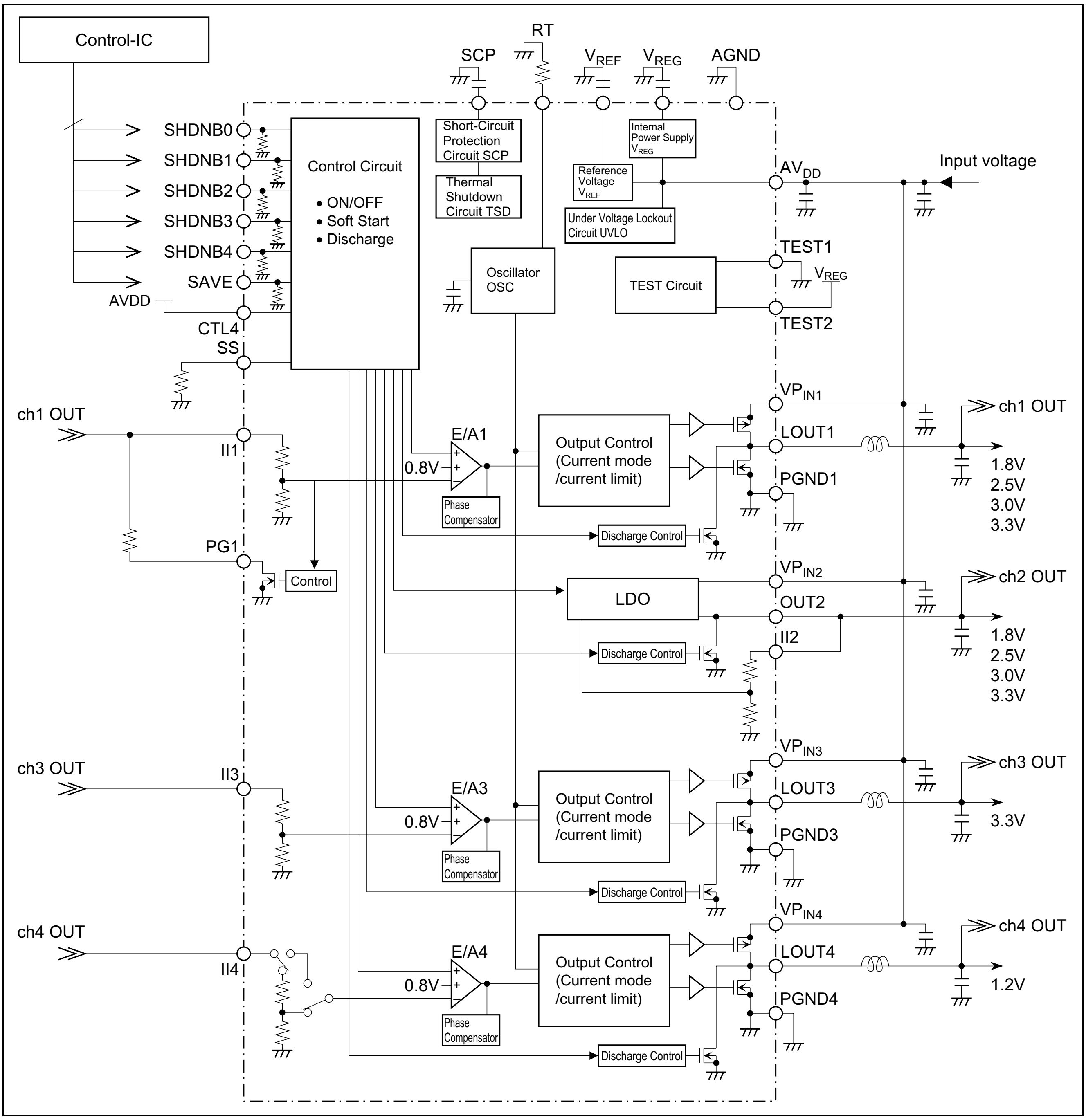
Constitution Example

- Input Voltage: 2.5 V to 5.5 V

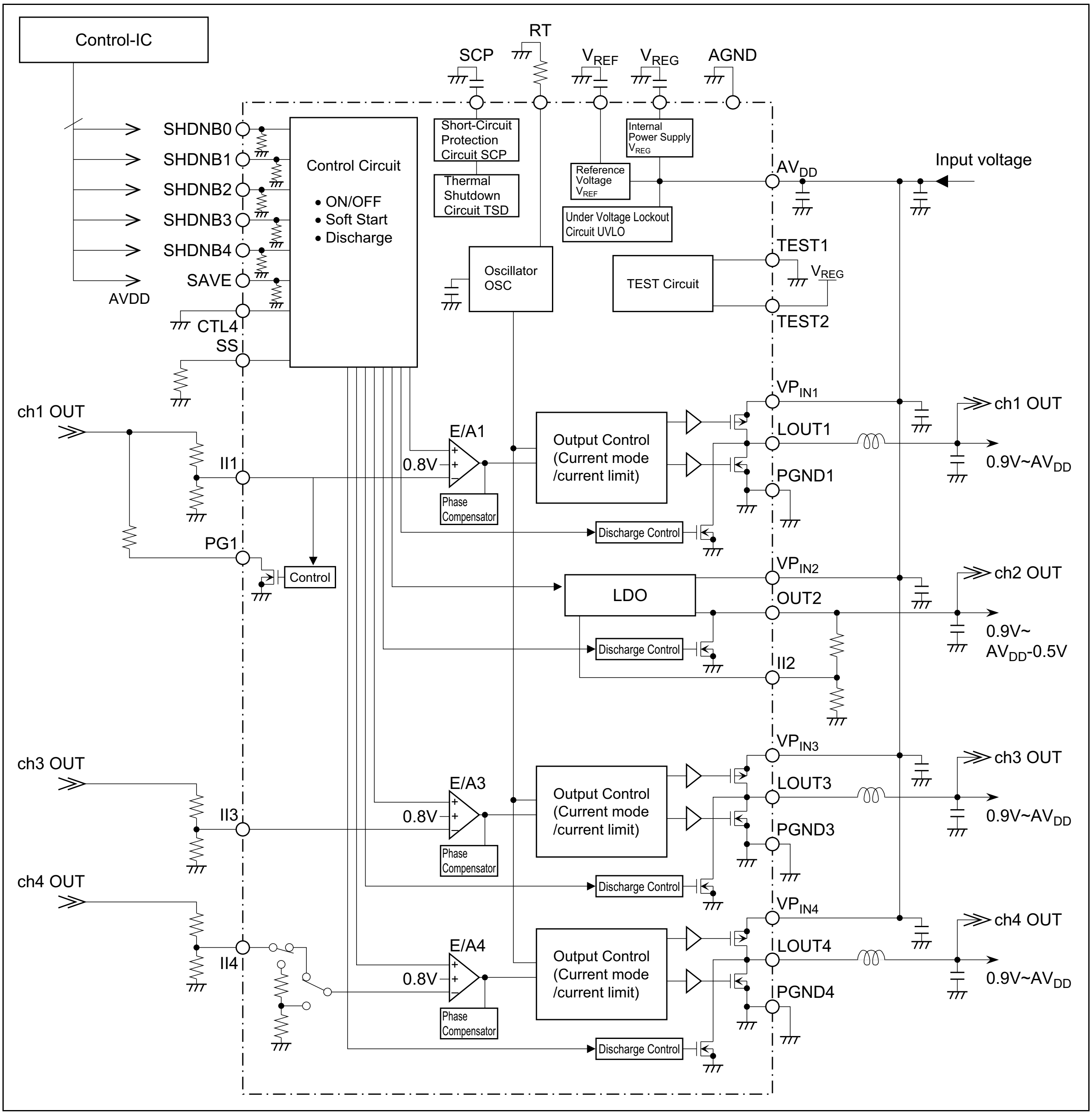
ch	Type	Power MOSFET	Output Voltage	Maximum Output Current Example
1	Synchronous rectification type step-down circuit (Current mode)	Integrated	0.9 V to VIN × 0.8 V	500 mA
2	LDO	—	0.9 V to VIN × 0.8 V	100 mA
3	Synchronous rectification type step-down circuit (Current mode)	Integrated	0.9 V to VIN × 0.8 V	1500 mA
4	Synchronous rectification type step-down circuit (Current mode)	Integrated	0.9 V to VIN × 0.8 V	1500 mA

Application Circuit Example

ch1 to ch3: Preset output voltage by internal resistor.
ch4: Preset output voltage by internal resistor is selected. (CTL4 = H)

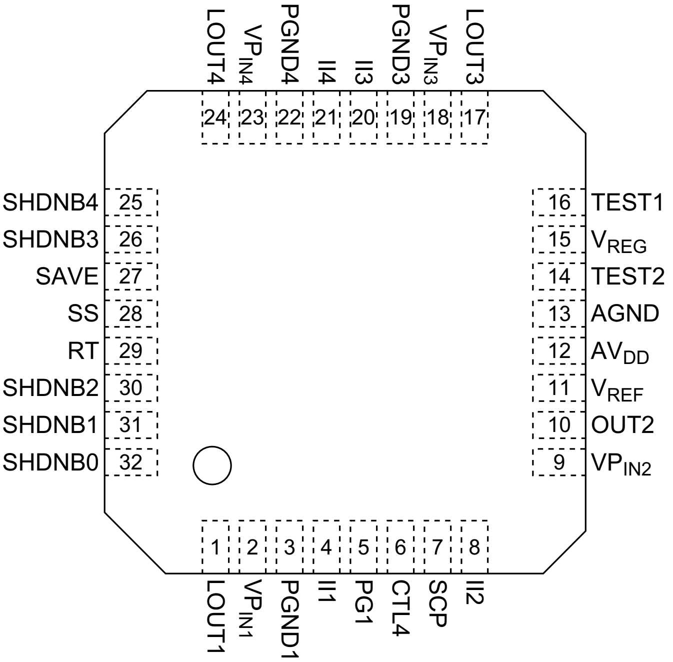


ch1 to ch3: Adjustable output voltage by external resistor.
ch4: Adjustable output voltage by external resistor is selected. (CTL4 = L)



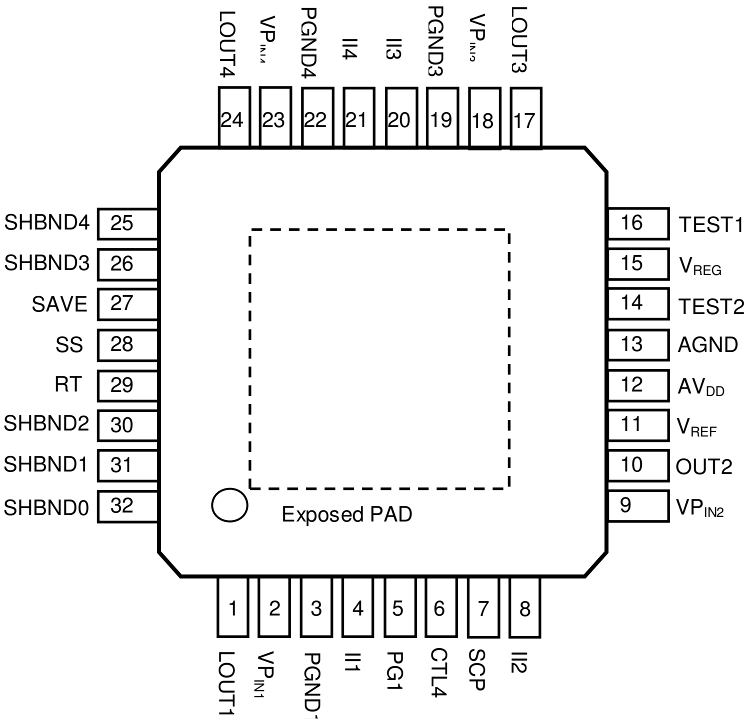
Pin Configuration

32-pin VQFN



(Top view)

32-pin TQFP



(Top view)

Pin Function

Pin No.	Symbol	I/O	Function
1	LOUT1	Output	Inductor connection for ch1
2	VP_{IN1}	Power supply	Output stage power input of ch1
3	PGND1	Ground	Power ground
4	II1	Input	Inverted input for error amplifier of ch1
5	PG1	Output	Power-good output of ch1 (open-drain)
6	CTL4	Input	Output voltage setting mode of ch4
7	SCP	—	Capacitor connection pin for timer latch
8	II2	Input	Inverted input for error amplifier of ch2
9	VP_{IN2}	Power supply	Output stage power input of ch2
10	OUT2	Output	Output of ch2
11	V_{REF}	Output	Reference voltage output
12	AV_{DD}	Power supply	Analog block power supply
13	AGND	Ground	Analog ground
14	TEST2	—	Test pin 2 (connect to V_{REG})
15	V_{REG}	Output	Internal power supply output
16	TEST1	—	Test pin 1 (connect to AGND)
17	LOUT3	Output	Inductor connection for ch3
18	VP_{IN3}	Power supply	Output stage power input of ch3
19	PGND3	Ground	Power ground
20	II3	Input	Inverted input for error amplifier of ch3
21	II4	Input	Inverted input for error amplifier of ch4
22	PGND4	Ground	Power ground
23	VP_{IN4}	Power supply	Output stage power input of ch4
24	LOUT4	Output	Inductor connection for ch4
25	SHDNB4	Input	Output ON/OFF of ch4
26	SHDNB3	Input	Output ON/OFF of ch3
27	SAVE	Input	Low power operation mode setting pin
28	SS	—	Resistance connection for soft start time setting
29	RT	—	Resistance connection for triangular wave generation
30	SHDNB2	Input	Output ON/OFF of ch2
31	SHDNB1	Input	Output ON/OFF of ch1
32	SHDNB0	Input	Output ON/OFF of IC

Absolute Maximum Ratings

(Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Ratings	Unit	Condition
Analog power supply (AV_{DD} pin)	AV_{DD}	–0.5 to +6.5	V	AV_{DD}
VP_{IN} pin applied voltage	VP_{IN}	–0.5 to +6.5	V	VP_{IN1} to VP_{IN4}
SHDNB pin applied voltage	V_{SHDNB}	–0.5 to +6.5	V	SHDNB0 to SHDNB4
CTL4 pin applied voltage	V_{CTL4}	–0.5 to +6.5	V	CTL4
SAVE pin applied voltage	V_{SAVE}	–0.5 to +6.5	V	SAVE
PG pin applied voltage	V_{PG}	–0.5 to +6.5	V	PG1
II pin applied voltage	V_{II}	–0.5 to +6.5	V	II1 to II4
VP_{IN1} pin sink current (peak)	$IP_{IN1(peak)-}$	600	mA	VP_{IN1}
VP_{IN2} pin sink current (DC)	$IP_{IN2(DC)-}$	200	mA	VP_{IN2}
VP_{IN3} pin sink current (peak)	$IP_{IN3(peak)-}$	2000	mA	VP_{IN3}
VP_{IN4} pin sink current (peak)	$IP_{IN4(peak)-}$	2000	mA	VP_{IN4}
LOUT1 pin output source current (peak)	$I_{LO1(peak)+}$	600	mA	LOUT1
OUT2 pin output source current (DC)	$I_{O2(DC)+}$	200	mA	OUT2
LOUT3 pin output source current (peak)	$I_{LO3(peak)+}$	2000	mA	LOUT3
LOUT4 pin output source current (peak)	$I_{LO4(peak)+}$	2000	mA	LOUT4
LOUT1, OUT2, LOUT3, LOUT4 pin output source current (DC)	$I_{LO1,O2,LO3,4(DC)-}$	100	mA	when discharge circuit is operation.
Total power dissipation	P_T	VQFN: 1850[*1] TQFP: 2100[1]	mW	$T_A \leq$ +25°C
Operating ambient temperature	T_A	–40 to +85	°C	
Junction temperature	T_J	–40 to +150	°C	
Storage temperature	T_{stg}	–55 to +150	°C	

Note:

*1 This is the value at $T_A \leq$ +25°C. At T_A > +25°C,
the total power dissipation is derated by –18.5 mW/°C (VQFN) or -21mW/°C (LQFP).
Board specification: VQFN:4-layers glass epoxy board. 76.2mm x 114.3mm x 1.664mm.
Copper coverage area: 50% (top and bottom layers)/95% (layers 2 and 3).
TQFP:4-layers glass epoxy board. 80mm x 80mm x 1.6mm. Renesas Evaluation Board for the case of that Exposed PAD is not soldered to GND copper pattern on board.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Condition

(Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Analog power supply voltage (AV_{DD} pin)	AV_{DD}	2.5	5.0	5.5	V	AV_{DD}
VP_{IN} pin applied voltage	VP_{IN}	—	AV_{DD}	—	V	VP_{IN1} to VP_{IN4}
SHDNB pin applied voltage	V_{SHDNB}	0	—	AV_{DD}	V	SHDNB0 to SHDNB4
CTL4 pin applied voltage	V_{CTL4}	0	—	AV_{DD}	V	CTL4
SAVE pin applied voltage	V_{SAVE}	0	—	AV_{DD}	V	SAVE
PG pin applied voltage	V_{PG}	0	—	AV_{DD}	V	PG1
II pin applied voltage	V_{II}	0	—	AV_{DD}	V	II1 to II4
Oscillation frequency	f_{OSC}	1300	—	2200	kHz	
Oscillator timing resistance	R_T	—	10	—	kΩ	R_T
Soft start resistance	R_{SS}	—	1000	—	kΩ	SS
SCP pin capacitance	C_{SCP}	—	0.1	—	μF	SCP
V_{REF} pin capacitance	C_{REF}	—	1.0	—	μF	V_{REF}
V_{REG} pin capacitance	C_{REG}	—	1.0	—	μF	V_{REG}
Operating junction temperature	T_{JO}	–40	—	+125	°C	

Electrical Characteristics

(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} to VP_{IN4} = 5.0 V, f_{OSC} = 2 MHz)

Parameter		Symbol	Min	Typ	Max	Unit	Condition
Total	Standby current	$I_{DD(STNBY)}$	—	1	2	µA	AI_{DD}+IP_{IN1}+IP_{IN2}+IP_{IN3}+IP_{IN4} SHDNB0 to SHDNB4 = AGND
	Circuit operation current 1	I_{DD1}	—	1.2	2	mA	AI_{DD}, SHDNB0 = AV_{DD} SHDNB1 to SHDNB4 = AGND SAVE = GND
	Circuit operation current 2	I_{DD2}	—	0.7	1.0	mA	AI_{DD}, SHDNB0 = AV_{DD} SHDNB1 to SHDNB4 = AGND SAVE = AV_{DD}
Reference voltage block (V_{REF})	Reference voltage	V_{REF}	0.98	1.00	1.02	V	I_{REF} = 0mA
	Temperature characteristic		—	0.5	—	%	T_A = –10°C to +60°C
Internal power supply block (V_{REG})	Internal power supply voltage	V_{REG}	2.3	2.4	2.5	V	I_{REG} = 0mA
Under voltage lock out circuit (UVLO)	Operation start voltage during rise time	$AV_{DD(L-H)}$	1.9	2.1	2.3	V	AV_{DD} pin voltage is detected
	Operation stop voltage	$AV_{DD(H-L)}$	1.7	1.9	2.1	V	AV_{DD} pin voltage is detected
Short-circuit protection circuit (SCP)	II1 input detection voltage (ch1)	$V_{TH(II)1}$	65	75	85	%	II1 pin, Ratio to the output voltage
	II3 input detection voltage (ch3)	$V_{TH(II)3}$	65	75	85	%	II3 pin, Ratio to the output voltage
	II4 input detection voltage (ch4)	$V_{TH(II)4}$	65	75	85	%	II4 pin, Ratio to the output voltage
	DLY detection voltage	$V_{TH(DLY)}$	0.6	0.9	1.2	V	SCP pin
	Short-circuit source current	I_{OUT}	0.6	1.0	1.4	µA	
Oscillation block	Frequency setting accuracy	f_{OSC}	–10	—	+10	%	R_T = 10kΩ
	Input stability	Δf_{OSC}	–3	—	+3	%	AV_{DD} = 2.5V to 5.5V
Soft start block	Soft start time	t_{ss}	—	2.0	4.0	ms	ch1 to ch4, R_{SS} = 1000kΩ
PWM block	Maximum duty	$D_{MAX.(PWM)}$	—	100	—	%	ch1, ch3, ch4
Output voltage accuracy (with resistor inside)	ch1 output voltage accuracy	V_{OUT1}	–2	—	+2	%	I_{O1} = 10mA, (with internal resistor)
	ch2 output voltage accuracy	V_{OUT2}	–1	—	+1	%	I_{O2} = 10mA, (with internal resistor)
	ch3 output voltage accuracy	V_{OUT3}	–2	—	+2	%	I_{O3} = 200mA, (with internal resistor)
	ch4 output voltage accuracy	V_{OUT4}	–2	—	+2	%	I_{O4} = 200mA, (with internal resistor)
E/A block (with resistor outside)	E/A 1 input threshold voltage	V_{ITH1}	0.784	0.800	0.816	V	Including input offset, (with external resistor)
	E/A 2 input threshold voltage	V_{ITH2}	0.792	0.800	0.808	V	Including input offset, (with external resistor)
	E/A 3 input threshold voltage	V_{ITH3}	0.784	0.800	0.816	V	Including input offset, (with external resistor)
	E/A 4 input threshold voltage	V_{ITH4}	0.784	0.800	0.816	V	Including input offset, (with external resistor)
Output block (ch1)	P-ch output ON resistance	R_{on-p1}	—	0.4	0.6	Ω	I_O = 100mA
	N-ch output ON resistance	R_{on-n1}	—	0.4	0.6	Ω	I_O = –100mA
Output block (ch3, ch4)	P-ch output ON resistance	R_{on-p1}	—	0.4	0.6	Ω	I_O = 100mA
	N-ch output ON resistance	R_{on-n1}	—	0.4	0.6	Ω	I_O = –100mA
Discharging circuit block	Output ON resistance1	R_{ondc1}	—	100	200	Ω	ch1, ch3, ch4, I_{DC} = 20mA
	Output ON resistance2	R_{ondc2}	—	200	400	Ω	ch2, I_{DC} = 20mA

Electrical Characteristics (cont.)

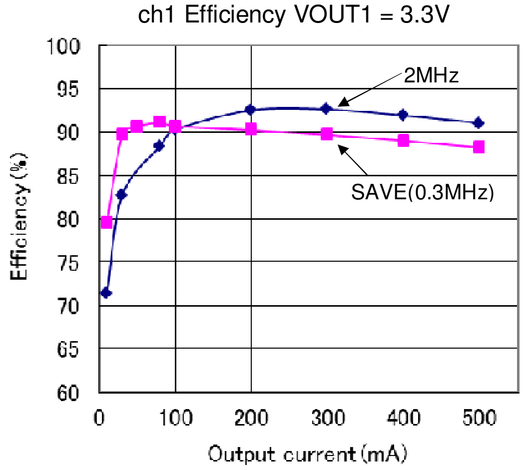
(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} to VP_{IN4} = 5.0 V, f_{OSC} = 2 MHz)

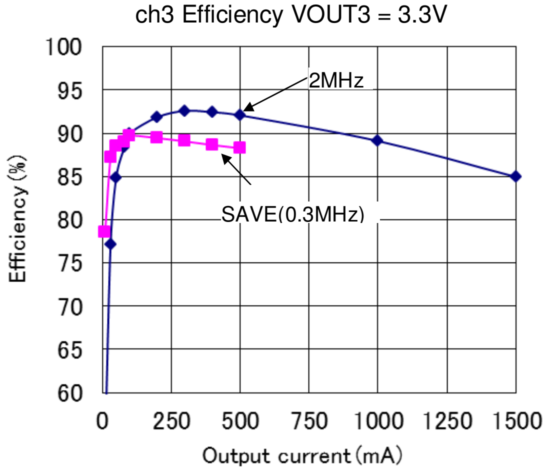
Parameter		Symbol	Min	Typ	Max	Unit	Condition
Series regulator block (ch2)	The voltage between the input and output	V_{DIF2}	0.5	—	—	V	I_{O2} = 20mA
	Input regulation	REG_{IN2}	—	—	50	mV	I_{O2} = 20mA, VP_{IN2} > VOUT2+0.5V
	Load regulation	REG_{L2}	—	—	50	mV	I_{O2} = 1mA to 100mA
	Output short-circuit current	$I_{O2short}$	—	80	—	mA	OUT2=AGND
	Peak output current	I_{O2peak}	150	—	—	mA	T.B.D.
Power-good circuit block (ch1)	Threshold voltage	$V_{TH(PG)1}$	86	90	94	%	PG1 = "HiZ"→"L", "L"→"HiZ" Detection of II1 pin Ratio to the output voltage
	PG pin output voltage	V_{PG}	—	—	0.1	V	I_{PG-} = 0.1mA
	PG pin leakage current	$I_{LEAK-PG}$	—	—	1	μA	SHDNB0 to SHDNB4 = AGND
	Delay time	t_{DLY-PG}	—	—	2	ms	Time from detecting of output startup until change form L to HiZ on PG pin
ON/OFF controller block	Threshold voltage	V_{TH}	0.8	—	2.0	V	SHDNB0 to SHDNB4, SAVE
	Input pull-down resistance	R_{IND}	200	400	700	kΩ	SHDNB0 to SHDNB4, SAVE

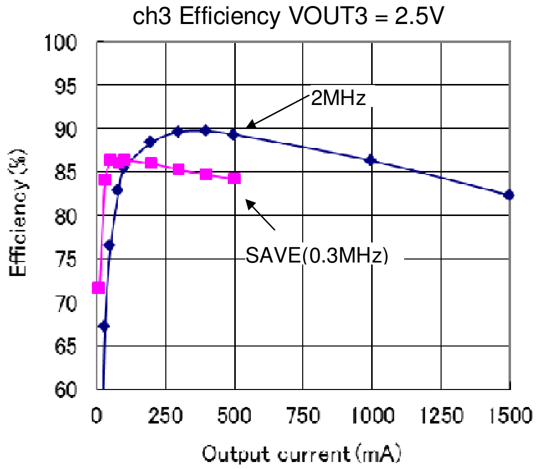
Typical Performance Characteristics

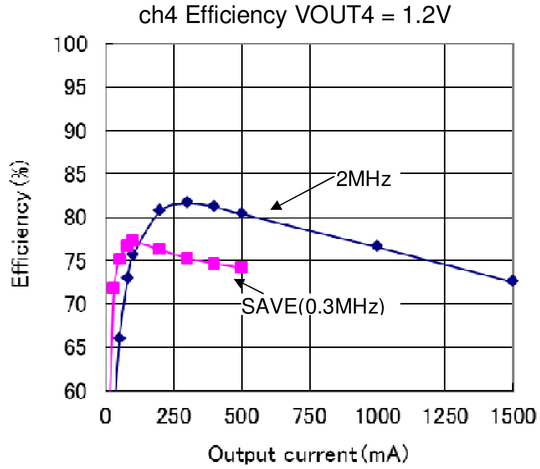
(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} to VP_{IN4} = 5.0 V, f_{OSC} = 2 MHz)

Efficiency vs. Output Current





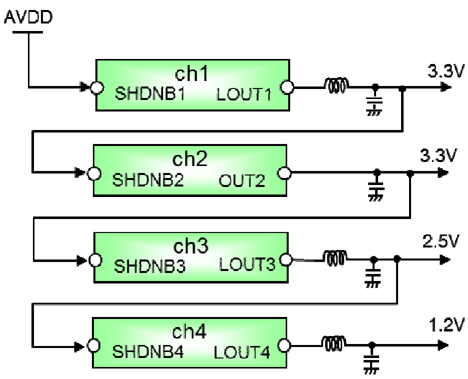




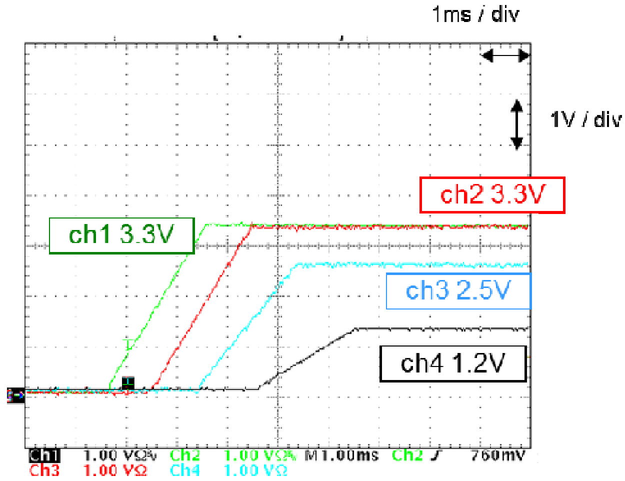
Start-up waveforms

Example 1 ch1(3.3V) ->ch2(3.3V) ->ch3(2.5V) ->ch4(1.2V)

Configuration

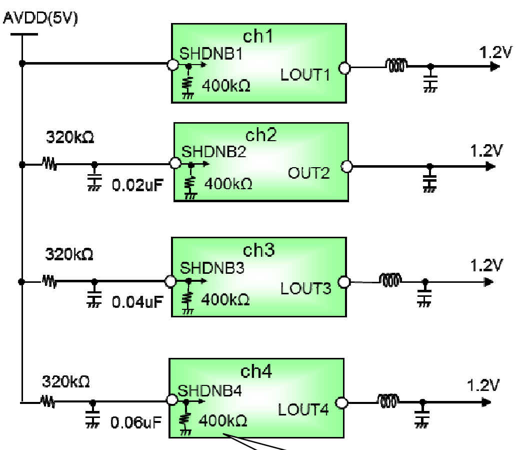


Waveform

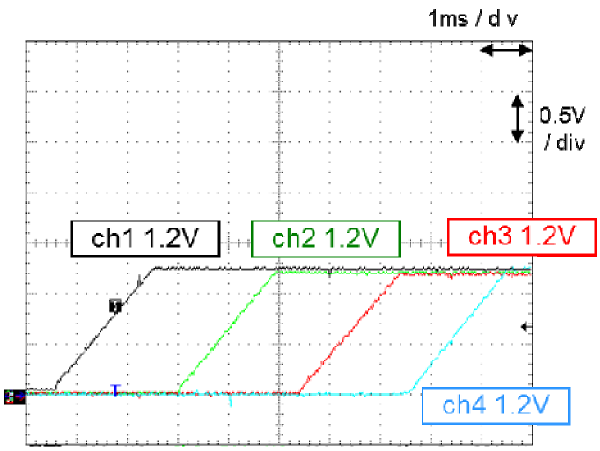


Example 2 ch1(1.2V) ->ch2(1.2V) ->ch3(1.2V) ->ch4(1.2V)

Configuration



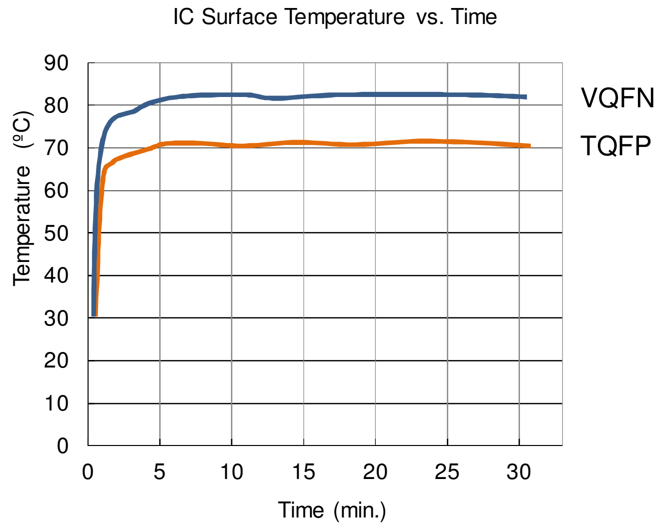
Waveform



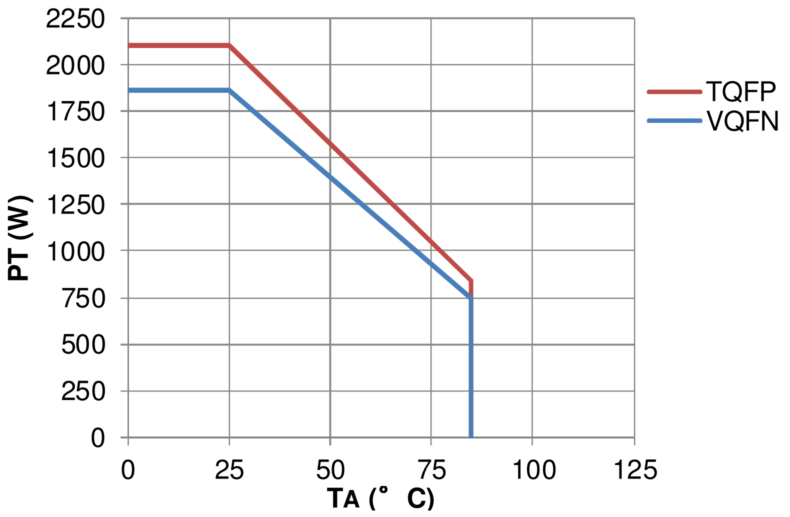
SHDNB pins have pull-down resistors (400kΩ). Please make sure that input voltage divided by external resistor on SHDNB pins shall not be lower than 1.4V.

IC Surface Temperature vs. Time

- All channel operating (normal mode)
- VIN=5V
- ch1: 3.3 V, 0.5 A ch2: 3.3 V, 0.1A ch3: 3.3 V, 1.5 A ch4: 1.2 V, 1.5 A
- T_A=25°C
- Measured on Renesas Evaluation board

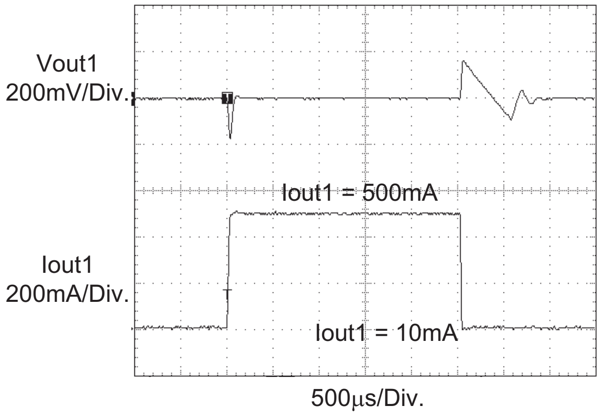


Temperature Derating Curve

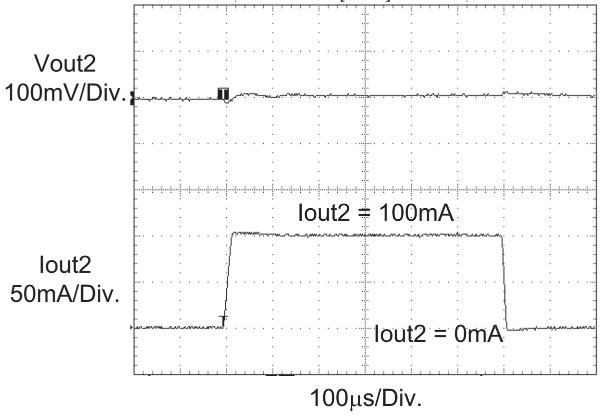


Load Transient Waveforms

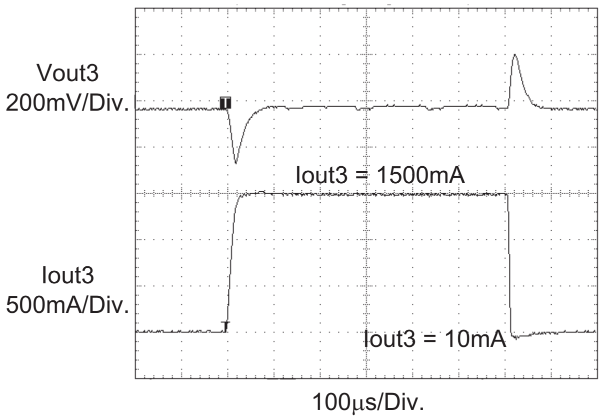
ch1 normal mode, Vout1 = 3.3V
L1 = 4.7μH, Cin1 = 10μF, Cout1 = 22μF



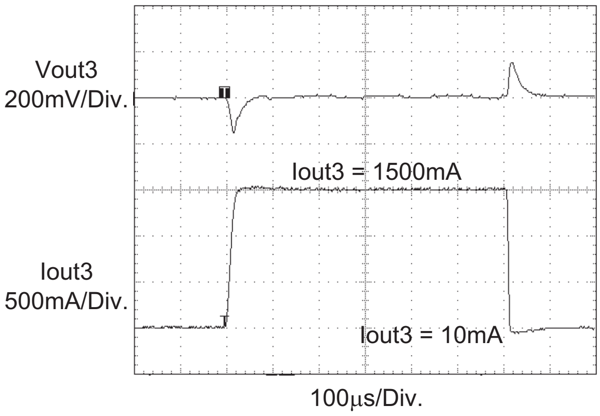
ch2, Vout2 = 3.3V
Cin2 = 10μF, Cout2 = 2.2μF



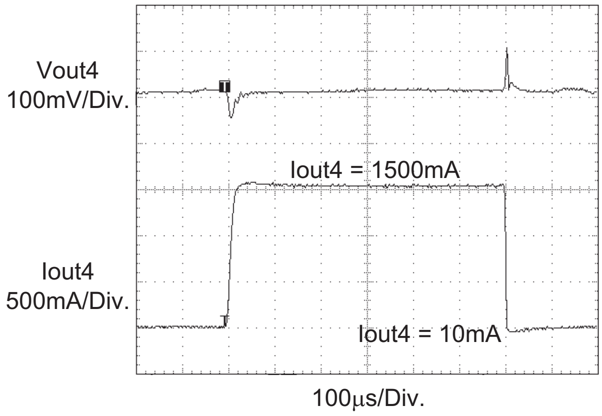
ch3 normal mode, Vout3 = 3.3V
L3 = 2.2μH, Cin3 = 10μF, Cout3 = 22μF



ch3 normal mode, Vout3 = 2.5V
L3 = 2.2μH, Cin3 = 10μF, Cout3 = 22μF



ch4 normal mode, Vout4 = 1.2V
L4 = 2.2uH, Cin4 = 10uF, Cout4 = 22uF



Control Block

SHDNB0 to SHDNB4: ON/OFF Setting

SHDNB0	SHDNB1	SHDNB2	SHDNB3	SHDNB4	Common Circuit	ch1	ch2	ch3	ch4
L	L or H	L or H	L or H	L or H	OFF	OFF	OFF	OFF	OFF
H	L	L	L	L	ON	OFF	OFF	OFF	OFF
H	H	L	L	L	ON	ON	OFF	OFF	OFF
H	L	H	L	L	ON	OFF	ON	OFF	OFF
H	L	L	H	L	ON	OFF	OFF	ON	OFF
H	L	L	L	H	ON	OFF	OFF	OFF	ON
H	H	H	H	H	ON	ON	ON	ON	ON

Note: L: Low level, H: High level
Common Circuit: Reference voltage block, internal power supply block, oscillator block and so forth
OFF: circuit stand-by, ON: circuit operation status

SAVE: IC Low Power Mode Setting

SAVE	IC Operation
L	Normal operation (ch1, ch3, ch4 operate at oscillation frequency set by RT)
H	Low power mode operation (ch1, ch3, ch4 operate at 15% oscillation frequency of normal operation)

Note: L: Low level, H: High level

CTL4: ch4 Output Voltage Setting

CTL4	ch4 Output Voltage Setting
L	External resistor setting
H	Internal resistor setting (fixed 1.2 V)

Note: L: Low level, H: High level

Output Status

V_{REG}, V_{REF} Pin Status

SHDNB0	V_{REG}	V_{REF}
L	AGND	AGND
H	2.4 V	1.0 V

Note: L: Low level, H: High level

ch1 to ch4 Output Pin Status

<table>
<tr><th rowspan="2">SHDNB0</th><th rowspan="2">SHDNB1 to SHDNB4</th><th>ch1</th><th>ch2</th><th>ch3</th><th>ch4</th></tr>
<tr><th>LOUT1</th><th>OUT2</th><th>LOUT3</th><th>LOUT4</th></tr>
<tr><td>L</td><td>L or H</td><td>HiZ
(Discharge circuit, OFF)</td><td>AGND
(Discharge circuit, ON)</td><td colspan="2">HiZ
(Discharge circuit, OFF)</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>PGND
(Discharge circuit, ON)</td><td>AGND
(Discharge circuit, ON)</td><td colspan="2">PGND
(Discharge circuit, ON)</td></tr>
<tr><td>H</td><td>Pulse
(VP_{IN1} or PGND)</td><td>ch2
(set voltage)</td><td>Pulse
(VP_{IN3} or PGND)</td><td>Pulse
(VP_{IN4} or PGND)</td></tr>
</table>

Note: L: Low level, H: High level, HiZ: High impedance

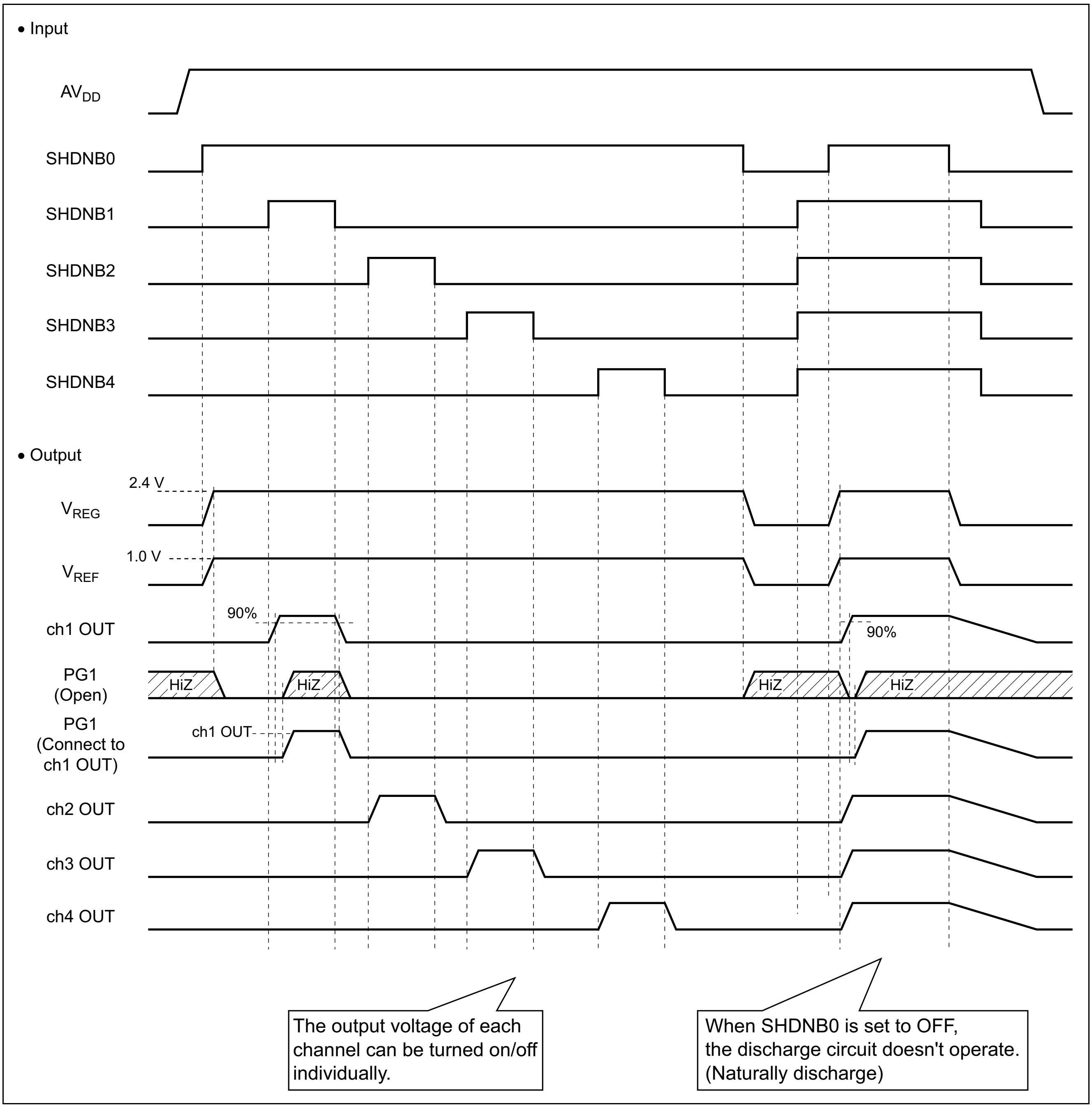
PG1 Pin Status

<table>
<tr><th colspan="2">IC Operation Status</th><th>PG1 Output Status</th></tr>
<tr><td colspan="2">SHDNB0 = L</td><td>HiZ</td></tr>
<tr><td rowspan="2">SHDNB0 = H</td><td>The ch1 output voltage is under 90% of the set voltage</td><td>L</td></tr>
<tr><td>The ch1 output voltage is over 90% of the set voltage</td><td>HiZ</td></tr>
</table>

Note: L: Low level, HiZ: High impedance

Caution: When using power good (PG1 pin), connect it to ch1 output.

Timing Chart



Operation of Each Block (Overview)

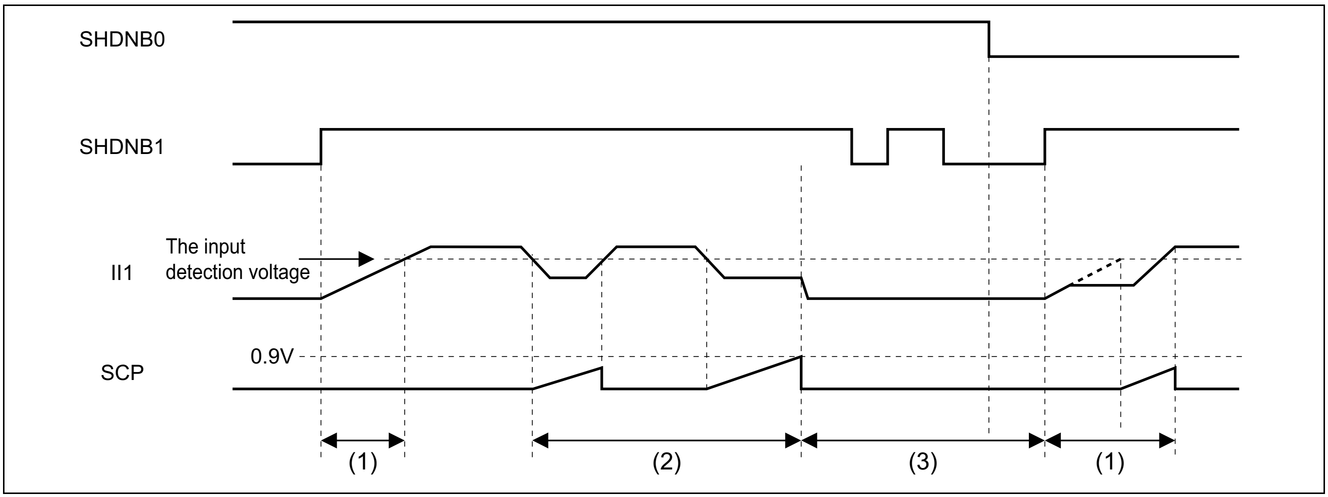
Short-Circuit Protection Circuit (ch1, ch3 and ch4)

When the voltage of ch1, ch3 and ch4 drops, the voltage of the E/A inverted input pin to which the output is being fed back also drops. If this inverted input pin voltage falls below the input detection voltage of the short-circuit protection circuit (under 75% of output voltage), the timer circuit starts operating and the capacitor connected to the SCP pin (CSCP) starts charging. When the voltage of the capacitor connected to the SCP pin reaches 0.9 V (TYP.), all the outputs are latched to OFF. At this time, common circuits (such as the reference voltage block, internal power supply block, and oscillator, etc.) continue operating.

As long as the voltage of any of the E/A inverted input pins of ch1 to ch4 is below the input detection voltage of the short-circuit protection circuit, the capacitor connected to the SCP pin continues charging.

When the short-circuit protection circuit is operating, to reset the latch circuit, either change the level of the SHDNB0 pin from high to low or drop the level of the power supply voltage (AV_{DD}) to the level below the operation stop voltage of the under voltage lockout circuit (1.7 V to 2.1 V).

- Timing Chart (when ch1 is short circuited)



(1) At starting
- — A short circuit will not be detected while a channel is undergoing a soft start (that is, short-circuit protection is not triggered). If a short circuit occurs while a channel is operating, short-circuit protection will start after the soft start time elapses following startup.
- — If a short circuit occurs in a channel that is operating while another channel is being soft-started, short-circuit protection will start immediately.

(2) Short-circuit protection operation
- — If a short circuit is detected in any of channel 1, 3 and 4 (channels whose II pin voltage is lower than the input detection voltage except channels that are being soft-started), the capacitor connected to the SCP pin starts charging. If short circuits occur in multiple channels, the capacitor connected to the SCP pin continues to charge until the short-circuit state of all channels is canceled (that is, until the II pin voltage is restored over the input detection voltage).
- — Once the SCP pin voltage reaches 0.9 V, output from all channels stops (and is latched to OFF).
- — Common circuits (such as the reference voltage block, internal power supply block, and oscillator, etc.) continue operating.

(3) Cancelling short-circuit protection
- — To reset the latch circuit, either change the level of the SHDNB0 pin from high to low, or drop the level of the power supply voltage (AV_{DD}) to the operation stop voltage of the under voltage lockout circuit (1.7 V to 2.1 V).

Thermal Shutdown Circuit (Timer Latch Type)

After overheating has been detected (shutdown temperature: 150°C or higher), the timer circuit starts operating and the capacitor connected to the SCP pin (CSCP) starts charging. When the voltage of the capacitor connected to the SCP pin reaches 0.9 V (TYP.), all the outputs are latched to OFF (as same as SCP). Common circuits (such as the reference voltage block, internal power supply block, and oscillator, etc.) continue operating.

When the thermal shutdown circuit is operating, to reset the latch circuit, either change the level of the SHDNB0 pin from high to low, or drop the level of the power supply voltage (AV_{DD}) to the operation stop voltage of the under voltage lockout circuit (1.7 V to 2.1 V).

Under Voltage Lockout Circuit (Auto Recovery Type)

(1) Under voltage lockout operation

When the power supply voltage (AV_{DD}) falls to the operation stop voltage (1.7 V to 2.1 V), output from all channels stops. Common circuits (such as the reference voltage block, internal power supply block, and oscillator, etc.) continue operating.

(2) Restoring output

Once AV_{DD} voltage is restored to the operation start voltage (1.9 V to 2.3 V), the under voltage lockout operation is canceled and output automatically resumes. The output voltage cannot be restored while the under voltage lockout circuit is operating, not even by manipulating the SHDNB0 pin.

Current Limiting

Ch1, ch3, and ch4 operate under the current control mode. If an overcurrent occurs, the current is limited on a pulse-by-pulse basis. If the current sensor detects an overcurrent, the current is limited and the switching operation of the Power MOSFET in the output stage stops until the next cycle.

When the current is limited, the output voltage of the channel on which the overcurrent occurred drops. If the II pin voltage falls below the input detection voltage, the short-circuit protection circuit starts operating.

Reference data (Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} to VP_{IN4} = 5.0 V, f_{OSC} = 2 MHz)

Item		Symbol	Min	Typ	Max	unit	Measurement condition
Current limit value	ch1 Current limet	I_{LIM1}	—	1.6	—	A	ch1OUT = 3.3V
	ch3, ch4 Current limet 1	I_{LIM34_1}	—	2.6	—	A	ch3OUT = ch4OUT = 3.3V
	ch3, ch4 Current limet 2	I_{LIM34_2}	—	2.1	—	A	ch3OUT = ch4OUT = 1.2V

Note: These data are for reference and not guaranteed as specifications.

Over Current Protection (ch2)

Ch2 have a fold back type current protection circuit. If load current exceeds 150 mA, protection operation is started and load current is limited (output short-circuit current: 80 mA).

Low Power Mode

This IC has the low power mode. By setting SAVE pin into a high level, the oscillation frequency of a switching regulator (ch1, ch3, ch4) is dropped on 15% oscillation frequency of normal operation, and the power consumption of the IC is reduced.

When switching to the low power mode, please switch the mode in a condition that the output current of a switching regulator (ch1, ch3, ch4) is below 100 mA.

Please be cautious of increasing the ripple voltage of each channel at the low power mode.

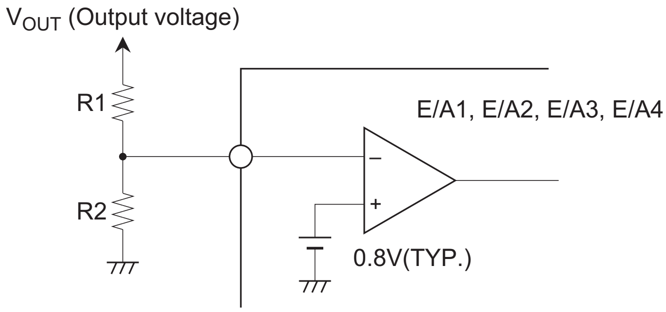
Advance on Designing

Setting Output Voltage (When the output voltage is set by external resistor)

The output voltage settings are shown in the figures below. The output voltage can be calculated by using the equations shown in these figures.

[Setting output voltage of ch1 to ch4 by external resistor]

$V_{OUT} = (1+R1/R2) \times 0.8$



Setting Oscillation Frequency

The oscillation frequency (f_{OSC}) can be arbitrarily set by the timing resistance (R_T) connected to the RT pin.

Approximate equation: $f_{OSC}[MHz] = -0.107 \times R_T[k\Omega] + 3.05$

Calculating the Soft Start Time

The soft start time (t_{SS}) can be arbitrarily set by the resistance (R_{SS}) connected to the SS pin.

Approximate equation: $t_{SS}[ms] = 1.8 \times R_{SS}[M\Omega] + 0.24$

Note: Soft start time is the same by all channels.

Calculating the Delay Time of the Short-circuit Protection Circuit

The following approximate expression is for calculating the delay time t_{DLY} of the short-circuit protection circuit.

The delay time of the short-circuit protection circuit (t_{DLY}) can be arbitrarily set by the capacitor (C_{SCP}) connected to the SCP pin.

Approximate equation: $t_{DLY}[s] = 0.9 \times C_{SCP}\ [\mu F]$

Pin handling when Short-circuit Protection Circuit is not used

When the short-circuit protection circuit is not used, connect the SCP pin to the AGND pin. At this time, closely monitor heating because the overheat protection circuit does not operate.

Handling of pins when not used

Connect unused pins as below.

Always connect AVDD pin, VPIN1 pin, VPIN2 pin, VPIN3 pin and VPIN4 pin with power supplies, and connect PGND1 pin, PGND3 pin, PGND4 pin and AGND with the ground.

When ch1 is not used:.

Pin number	Pin name	Connection
31	SHDNB1	AGND
2	VP_{IN1}	AV_{DD}, or VP_{IN} of other ch
1	LOUT1	PGND
3	PGND1	PGND
4	II1	AGND

When ch2 is not used:

Pin number	Pin name	Connection
30	SHDNB2	AGND
9	VP_{IN2}	AV_{DD}, or VP_{IN} of other ch
10	OUT2	AGND
8	II2	AGND

When ch3 is not used:

Pin number	Pin name	Connection
26	SHDNB3	AGND
18	VP_{IN3}	AV_{DD}, or VP_{IN} of other ch
17	LOUT3	PGND
19	PGND3	PGND
20	II3	AGND

When ch4 is not used:

Pin number	Pin name	Connection
25	SHDNB4	AGND
23	VP_{IN4}	AV_{DD}, or VP_{IN} of other ch
24	LOUT4	PGND
22	PGND4	PGND
21	II4	AGND
6	CTL4	AGND

When PG1 pin is not used

Pin number	Pin name	Connection
5	PG1	AGND

Inductor selection

It is recommended to choose a inductor which ripple current (ΔIL) becomes 20 to 40 % of Iout(max).

When ΔIL increases, inductor current peak raises, so ripple of Vout gets larger and power loss increases. But, large inductor is required to lower ΔIL.

ΔIL can be calculated by an equation below.

ΔIL = (Vin-Vout) / L x Vout / Vin x 1 / fsw

fsw : Switching frequency of DCDC, 1.3MHz to 2MHz

Peak current of inductor (ILpeak) can be calculated by an equation below.

ILpeak = Iout(max) + ΔIL / 2

Choose a inductor which saturation current is higher than ILpeak .

Inductor Example

ch	Output Current	Inductor	Manufacturer	Inductance (uH)	I_{TEMP} (A)	I_{SAT} (A)	Size (LxWxT, mm)
ch1	less than 0.5A	CPL2512T4R7M	TDK	4.7	0.65	0.65	2.5x1.5x1.2
		NRS2012T4R7MGJ	TAIYO YUDEN	4.7	0.82	0.76	2x2x1.2
		74479787247A	WURTH	4.7	1.5	0.27	2.5x2x1
		744028004	WURTH	4.7	0.85	0.7	2.8x2.8x1.1
ch3 ch4	less than 1A	VLS201612ET-2R2M	TDK	2.2	1.15	1.05	2x1.6x1.2
		NRS2012T2R2MGJ	TAIYO YUDEN	2.2	1.37	1.35	2x2x1.2
		744029002	WURTH	2.2	1.5	1.15	2.8x2.8x1.35
	1A to 1.5A	LQH44PN2R2MP0	MURATA	2.2	1.8	2.5	4x4x1.65
		NRS4018T2R2MDGJ	TAIYO YUDEN	2.2	2.2	3	4x4x1.8
		744025002	WURTH	2.2	1.8	2.4	2.8x2.8x2.8

Note I_{TEMP} : Rated current by temperature rising
I_{SAT} : Rated current by inductance loss
These inductors are examples. About inductor detail, contact each manufacturer.

Output capacitor selection

Each channel of RAA23040x has a phase compensation circuit which is optimized to each operation. In order to operate stably with the phase compensation, connect the output capacitor :

Switching Regulator (ch1, ch3, ch4) : over 22uF

LDO (ch2) : over 2.2uF

Ceramic capacitor can be used for output capacitor. It has low ESR, so VOUT ripple is decreased.

VOUT ripple ($\Delta Vrpl$) can be calculated by an equation below.

$$\Delta Vrpl = \Delta IL \times (ESR + 1 / (8 \times Cout \times fsw))$$

Input capacitor selection

Recommended input capacitor of switching regulator can be calculated by an equation below. Connect the capacitor that value is over calculated one.

$$Cin > (Iout(max) \times Vout / Vin) / (\Delta Vin \times fsw)$$

About LDO, connect the capacitor that value is over 1uF.

Notes on Use

Condition where Protection Circuits do not operate

When the SCP pin is connected to the AGND pin, the short-circuit protection circuit and thermal shutdown circuit do not operate.

Pin Connection

Be sure to apply the same voltage to AV_{DD} pin and VP_{IN} pin (except VP_{IN2}).

VP_{IN2} Input Voltage

VP_{IN2} input voltage should be same or less than AV_{DD}.

PG1 Connection

When using power good (PG1 pin), connect it to ch1 output. If PG1 is connected to AV_{DD}, PG1 outputs high (AV_{DD}) when SHDNB0 is low (because PG1 is high impedance when SHDNB0 is low).

Actual Pattern Wiring

To actually perform pattern wiring, separate the ground of the control signals from the ground of the power signals, so that these signals do not have a common impedance as much as possible. In addition, lower the high-frequency impedance by using a capacitor, so that noise is not superimposed on the V_{REF} pin, V_{REG} pin.

Connection of Exposed PAD (only TQFP package)

TQFP package has an exposed pad on the bottom to improve radiation performance. On the mounting board, connect this exposed pad to AGND.

Fixed Usage of Control Input Pin

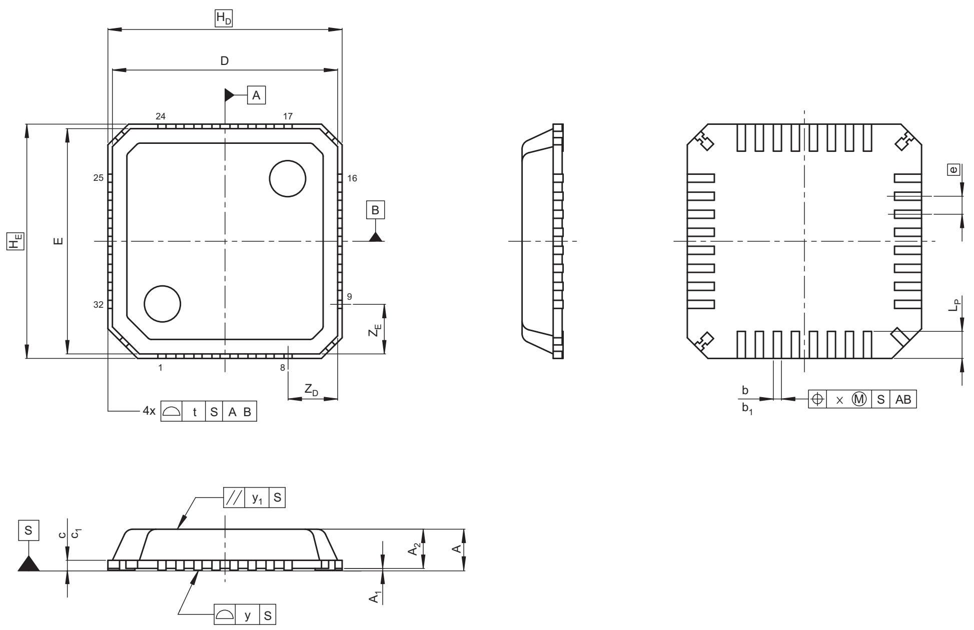
When using fixed input pins SHDNB0 to SHDNB4, CTL4 and SAVE input pins, connect each input to the pins listed below.

Input Pin	Connect Pin	
	Fixed to Low Level	Fixed to High Level
SHDNB0	AGND	AV_{DD}
SHDNB1	AGND	AV_{DD}
SHDNB2	AGND	AV_{DD}
SHDNB3	AGND	AV_{DD}
SHDNB4	AGND	AV_{DD}
CTL4	AGND	AV_{DD}
SAVE	AGND	AV_{DD}

Package Dimensions

32-pin VQFN 5 mm × 5 mm 0.4 mm pitch

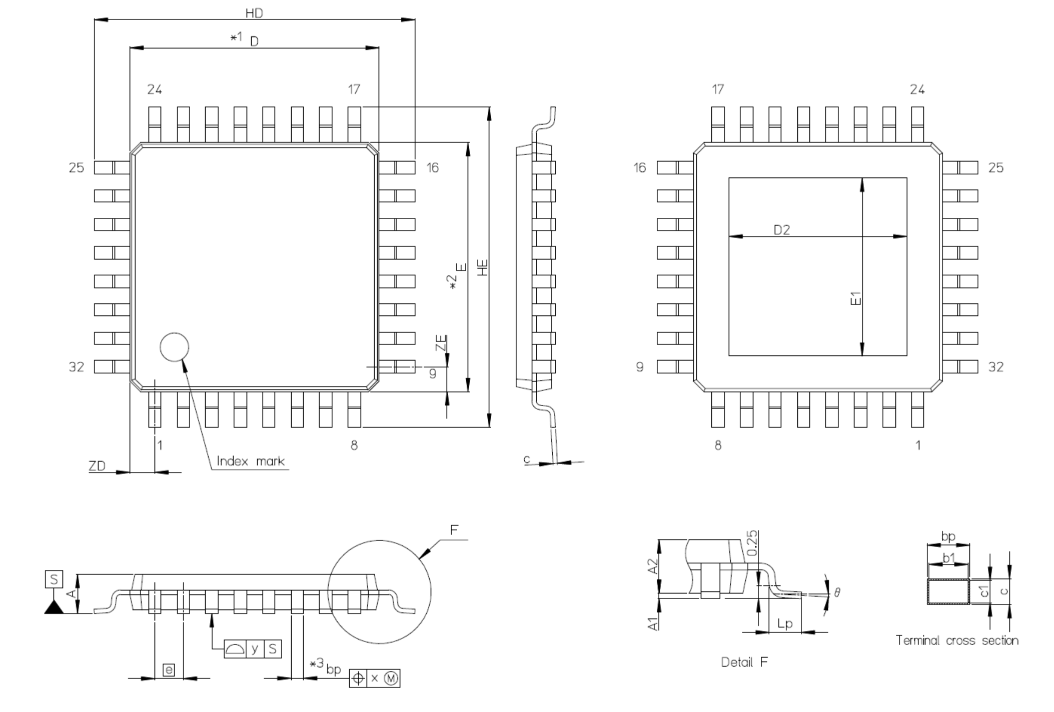
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VQFN32-5x5-0.40	PVQN0032LA-A	—	0.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.0	—
E	—	5.0	—
A_2	—	0.89	—
A	—	—	0.95
A_1	0.005	0.02	0.04
b	0.13	0.18	0.23
b_1	—	0.16	—
e	—	0.4	—
L_p	0.50	0.60	0.70
x	—	—	0.05
y	—	—	0.05
y_1	—	—	0.2
t	—	—	0.2
H_D	—	5.2	—
H_E	—	5.2	—
Z_D	—	1.1	—
Z_E	—	1.1	—
c	0.17	0.22	0.25
c_1	—	0.20	—

32-pin TQFP 7 mm × 7 mm 0.8 mm pitch

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HTQFP32-7x7-0.80	PTQP0032GA-A	32P6X-A	0.14g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	0.95	1.0	1.05
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.2
A1	0.05	0.1	0.15
bp	0.3	—	0.45
b1	0.3	0.35	0.4
c	0.09	—	0.2
c1	0.09	0.125	0.16
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.2
y	—	—	0.1
Lp	0.45	0.6	0.75
D2	—	5.0	—
E1	—	5.0	—
ZD	—	0.7	—
ZE	—	0.7	—

Rev.	Date	Description	
		Page	Summary
1.01	Oct 18, 2012	-	First Edition issued
1.02	Jul 09, 2013	1	Changed package name from LQFP to TQFP. Added packing unit.
		5	Added Pin Configuration of 32-pin TQFP.
		7	Added Total power dissipation and Board specification.
		9	Changed Short-circuit source current from Min 0.7uA to 0.6uA and Max 1.3uA to 1.4uA.
		10	Changed Output short-circuit current from Typ 40mA to 80mA. Added condition of Input regulation, Load regulation and Output short-circuit current.
		12	Added start-up waveforms.
		13	Added input voltage VIN condition. Changed output voltage/current condition. Added TQFP product's data. Added Temperature Derating Curve.
		16	Changed Output Pin Status of ch2 at SHDNB0=L from HiZ to GND.
		19	Added Reference data of Current limit value. Changed Output short-circuit current of Over Current Protection (ch2) from Typ 40mA to 80mA.
		21	Added Handling of pins when not use.
		22	Added Inductor selection
		23	Added Output capacitor selection and Input capacitor selection.
		24	Added Connection of Exposed PAD.
		26	Added Package Dimensions of TQFP package.

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE: Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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