# Evaluation Board for the AD7265/AD7266

# EVAL-AD7265/AD7266

## FEATURES

**Full-featured evaluation board for the AD7265 and AD7266**
**EVAL-CED1Z compatible**
**Standalone capability**
**On-board analog buffering and voltage reference**
**On-board single-ended-to-differential conversion**
**Various linking options**
**PC software for control and data analysis when used with EVAL-CED1Z**

## GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7265 and the AD7266, which are dual, 12-bit, high speed, low power successive approximation ADCs that operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 2 MSPS.

Full details on the AD7265 and the AD7266 are available in the device data sheets, which are available from Analog Devices, Inc., and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include an AD780, which is a pin programmable 2.5 V or 3 V ultrahigh precision band gap reference, nine AD8022 dual op amps, and a 7S04 digital buffer. Various link options are explained in Table 1.

Interfacing to this evaluation board is through a 96-way connector. This 96-way connector is compatible with the EVAL-CED1Z, which is available from Analog Devices. External sockets are provided for a number of signals, including the $V_{REF}$ input, the analog inputs, and the digital inputs and outputs.

## FUNCTIONAL BLOCK DIAGRAM

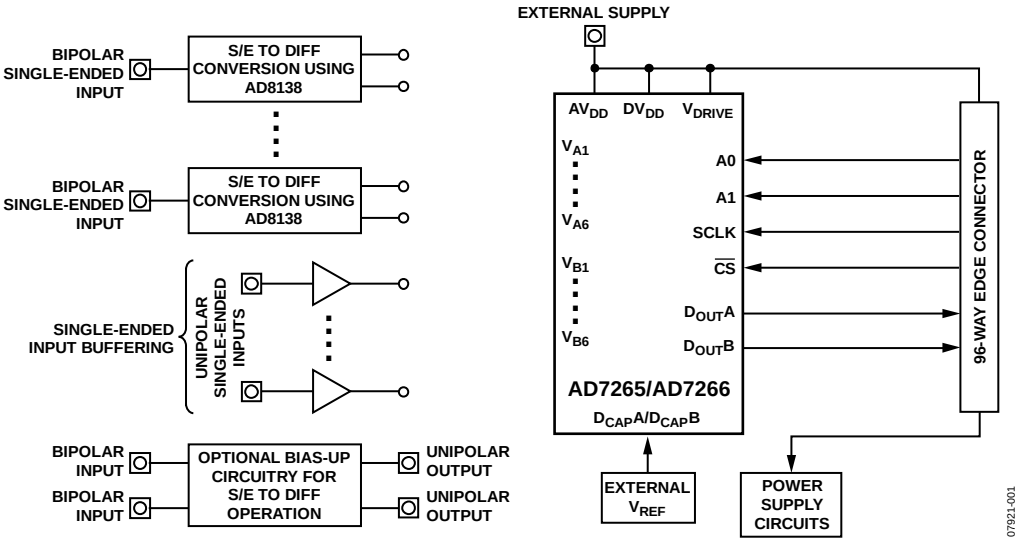


*Figure 1.*



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## REVISION HISTORY

**4/09—Revision 0: Initial Version**

# EVALUATION BOARD HARDWARE

## POWER SUPPLIES

When using this evaluation board with the EVAL-CED1Z, all supplies are provided from the EVAL-CED1Z through the 96-way connector. When using the board as a standalone unit, external supplies must be provided. This evaluation board has the following power supply inputs: +12 V, −12V, $A_{VDD}$ (+5 V), $D_{VDD}$ (+5 V), AGND, $V_{DRIVE}$, and DGND. The +12 V supply is only required if the external AD780 voltage reference and op amps are to be used.

The supplies are decoupled to the relevant ground plane with 10 μF tantalum and 0.1 μF multilayer ceramic capacitors at the point where they enter the board. The supply pins for the external reference are also decoupled to AGND with a 470 nF ceramic capacitor. The AD7265/AD7266 $AV_{DD}$ and $V_{DRIVE}$ supply pins are also decoupled to AGND, while $DV_{DD}$ is decoupled to DGND, with a 0.1 μF multilayer ceramic capacitor and a 10 μF tantalum capacitor at the device pins. Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, AGND and DGND. These are connected at one location close to the AD7265/AD7266.

## LINK OPTIONS

There are 49 link options that must be set correctly to select the appropriate operating setup before using the evaluation board. The functions of the link options are outlined in Table 1.

**Table 1. Link Function Descriptions**

| Link No. | Description |
|---|---|
| LK1 | This link option selects the source of the $V_{A1}$ analog input.<br>In Position A, $V_{A1}$ is supplied from the output of the unity gain buffer, U3-A, in which case a signal must be applied to the SVIN1 SMB socket via J13.<br>In Position B, $V_{A1}$ is supplied from the positive output (V1+) of the single-ended-to-differential converter, U5-B, in which case a single-ended signal must be applied to V1 DIFF via Socket J17.<br>In Position C, $V_{A1}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK2 | This link option selects the source of the $V_{A2}$ analog input.<br>In Position A, $V_{A2}$ is supplied from the output of the unity gain buffer, U3-B, in which case a signal must be applied to the SVIN2 socket via J14.<br>In Position B, $V_{A2}$ is supplied from the negative output (V1−) of the single-ended-to-differential converter, U5-A, in which case a single-ended signal must be applied to V1 DIFF via Socket J17.<br>In Position C, $V_{A2}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK3 | This link option selects the source of the $V_{A3}$ analog input.<br>In Position A, $V_{A3}$ is supplied from the output of the unity gain buffer, U3-A, in which case a signal must be applied to the SVIN1 socket via J13.<br>In Position B, $V_{A3}$ is supplied from the positive output (V2+) of the single-ended-to-differential converter, U6-B, in which case a single-ended signal must be applied to V2 DIFF via Socket J19.<br>In Position C, $V_{A3}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK4 | This link option selects the source of the $V_{A4}$ analog input.<br>In Position A, $V_{A4}$ is supplied from the output of the unity gain buffer, U3-B, in which case a signal must be applied to the SVIN2 socket via J14.<br>In Position B, $V_{A4}$ is supplied from the negative output (V2−) of the single-ended-to-differential converter, U6-A, in which case a single-ended signal must be applied to V2 DIFF via Socket J19.<br>In Position C, $V_{A4}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK5 | This link option selects the source of the $V_{A5}$ analog input.<br>In Position A, $V_{A5}$ is supplied from the output of the unity gain buffer, U3-A, in which case a signal must be applied to the SVIN1 socket via J13.<br>In Position B, $V_{A5}$ is supplied from the positive output (V1+) of the single-ended-to-differential converter, U5-B, in which case a single-ended signal must be applied to V1 DIFF via Socket J17.<br>In Position C, $V_{A5}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK6 | This link option selects the source of the $V_{A6}$ analog input.<br>In Position A, $V_{A6}$ is supplied from the output of the unity gain buffer, U3-B, in which case a signal must be applied to the SVIN2 socket via J14.<br>In Position B, $V_{A6}$ is supplied from the negative output (V1−) of the single-ended-to-differential converter, U5-A, in which case a single-ended signal must be applied to V1 DIFF via Socket J17.<br>In Position C, $V_{A6}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |

| Link No. | Description |
|---|---|
| LK7 | This link option selects the source of the $V_{B1}$ analog input.<br>In Position A, $V_{B1}$ is supplied from the output of the unity gain buffer, U4-A, in which case a signal must be applied to the SVIN3 socket via J15.<br>In Position B, $V_{B1}$ is supplied from the positive output (V3+) of the single-ended-to-differential converter, U7-B, in which case a single-ended signal must be applied to V3 DIFF via Socket J20.<br>In Position C, $V_{B1}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK8 | This link option selects the source of the $V_{B2}$ analog input.<br>In Position A, $V_{B2}$ is supplied from the output of the unity gain buffer, U4-B, in which case a signal must be applied to the SVIN4 socket via J16.<br>In Position B, $V_{B2}$ is supplied from the negative output (V3–) of the single-ended-to-differential converter, U7-A, in which case a single-ended signal must be applied to V3 DIFF via Socket J20.<br>In Position C, $V_{B2}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK9 | This link option selects the source of the $V_{B3}$ analog input.<br>In Position A, $V_{B3}$ is supplied from the output of the unity gain buffer, U4-A, in which case a signal must be applied to the SVIN3 socket via J15.<br>In Position B, $V_{B3}$ is supplied from the positive output (V4+) of the single-ended-to-differential converter, U8-B, in which case a single-ended signal must be applied to V4 DIFF via Socket J22.<br>In Position C, $V_{B3}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK10 | This link option selects the source of the $V_{B4}$ analog input.<br>In Position A, $V_{B4}$ is supplied from the output of the unity gain buffer, U4-B, in which case a signal must be applied to the SVIN4 socket via J16.<br>In Position B, $V_{B4}$ is supplied from the negative output (V4–) of the single-ended-to-differential converter, U8-A, in which case a single-ended signal must be applied to V4 DIFF via Socket J22.<br>In Position C, $V_{B4}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK11 | This link option selects the source of the $V_{B5}$ analog input.<br>In Position A, $V_{B5}$ is supplied from the output of the unity gain buffer, U4-A, in which case a signal must be applied to the SVIN3 socket via J15.<br>In Position B, $V_{B5}$ is supplied from the positive output (V3+) of the single-ended-to-differential converter, U7-B, in which case a single-ended signal must be applied to V3 DIFF via Socket J20.<br>In position C, $V_{B5}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK12 | This link option selects the source of the $V_{B6}$ analog input.<br>In Position A, $V_{B6}$ is supplied from the output of the unity gain buffer, U4-B, in which case a signal must be applied to the SVIN4 socket via J16.<br>In Position B, $V_{B6}$ is supplied from the negative output (V3–) of the single-ended-to-differential converter, U7-A, in which case a single-ended signal must be applied to V3 DIFF via Socket J20.<br>In Position C, $V_{B6}$ is tied to AGND. If this channel is not in use, this link should be in Position C. |
| LK13 | This link option selects the source or destination of the reference voltage applied to or received from the $D_{CAP}A$ pin of the AD7265/AD7266.<br>In Position A, an external reference signal can be applied to the $D_{CAP}A$ pin via J24, or the internal reference voltage from the AD7266/AD7265 can be accessed via J24. This link should be used in conjunction with LK19, which determines whether an internal or external reference is used with the device.<br>In Position B, the AD780 provides an external 2.5 V reference to the $D_{CAP}A$ pin. This link should be set up in conjunction with LK16.<br>If both Link Option A and Link Option B are inserted, the AD780 provides the reference voltage for the AD7265/AD7266, which is also output via J24. |
| LK14 | This link option selects the source or destination of the reference voltage applied to or received from the $D_{CAP}B$ pin of the AD7265/AD7266.<br>In Position A, an external reference signal can be applied to the $D_{CAP}B$ pin via J25, or the internal reference voltage from the AD7265/AD7266 can be accessed via J25. This link should be used in conjunction with LK19, which determines whether an internal or external reference is used with the device.<br>In Position B, the AD780 provides an external 2.5 V reference to the $D_{CAP}B$ pin. This link should be set up in conjunction with LK16.<br>If both Link Option A and Link Option B are inserted, the AD780 provides the reference voltage, which is output via J25. |
| LK15 | This link option selects the source of the $AV_{DD}$ and $DV_{DD}$ supply for the AD7265/AD7266.<br>In Position A, $V_{DD}$ (+5 V) is supplied from the EVAL-CED1Z.<br>In Position B, the $V_{DD}$ voltage must be supplied from an external source via J2. |

| Link No. | Description |
|---|---|
| LK16 | This link option sets the output reference voltage delivered by the AD780.<br>When this link is inserted, the AD780 output voltage is set to +3.0 V.<br>When this link is removed, the AD780 output voltage is set to +2.5 V. |
| LK17 | This link option selects the source of the $V_{DRIVE}$ supply for the AD7265/AD7266.<br>In Position A, $V_{DRIVE}$ is supplied from the EVAL-CED1Z. The value of $V_{DRIVE}$ in this case is 3.3 V.<br>In Position B, the $V_{DRIVE}$ supply must be supplied from an external source via J3. Note that the logic interface on the EVAL-CED1Z operates at 3.3 V. |
| LK18 | Not populated. |
| LK19 | This link option selects the logic input to the REF SELECT pin.<br>In Position A, the REF SELECT pin is tied to $V_{DRIVE}$ (Logic 1). Therefore, an external reference must be supplied through the $D_{CAP}A/D_{CAP}B$ pins.<br>In Position B, the REF SELECT pin is tied to DGND (Logic 0). Therefore, the internal on-chip 2.5 V reference is used. |
| LK20 | This link option selects the logic input to the RANGE pin.<br>In Position A, the RANGE pin is tied to $V_{DRIVE}$ (Logic 1). Therefore, the device is configured for an analogue input range of 0 V to 2 $V_{REF}$.<br>In Position B, the RANGE pin is tied to DGND (Logic 0). Therefore, the analogue input range is 0 V to $V_{REF}$. |
| LK21 | This link option selects the logic input to the SGL/$\overline{DIFF}$ pin.<br>In Position A, the ADC is tied to $V_{DRIVE}$ and, therefore, the ADC is configured to operate in single-ended mode.<br>In Position B, the ADC is tied to DGND and, therefore, the ADC is configured to operate in differential mode. |
| LK22 | This link option selects the source of the logic input to the A0 pin. It should be used in conjunction with LK23 and LK24 to determine the pair of channels to be simultaneously converted.<br>In Position A, the A0 pin is tied to a $V_{DRIVE}$, a high logic level.<br>In Position B, the logic level applied to the A0 pin is controlled via the channel selection option in the software.<br>In Position C, the A0 pin is tied to DGND, a low logic level.<br>In Position D, an external A0 logic level can be applied through the external socket, J6. |
| LK23 | This link option selects the source of the logic input to the A1 pin; it should be used in conjunction with LK22 and LK24, to determine the pair of channels to be simultaneously converted.<br>In Position A, the A1 pin is tied to $V_{DRIVE}$, a high logic level.<br>In Position B, the logic level applied to A1 is controlled via the channel selection icon in the software.<br>In Position C, the A1 pin is tied to DGND, a low logic level.<br>In Position D, an external A1 logic level can be applied through the external socket, J7. |
| LK24 | This link option selects the source of the logic input to the A2 pin; it should be used in conjunction with LK22 and LK23 to determine the pair of channels to be simultaneously converted.<br>In Position A, the A2 pin is tied to $V_{DRIVE}$, a high logic level.<br>In Position B, the logic level applied to A1 is controlled via the channel selection option in the software.<br>In Position C, the A2 pin is tied to DGND, a low logic level.<br>In Position D, an external A2 value can be applied through the external socket, J8. |
| LK25 | This link option selects the source of the $\overline{CS}$ input.<br>In Position A, the $\overline{CS}$ input is provided by the EVAL-CED1Z.<br>In Position B, the $\overline{CS}$ input is provided via the external SMB socket, J9. |
| LK26 | Not populated. |
| LK27 | This link option selects the source of the SCLK input.<br>In Position A, the SCLK input is provided via the external SMB socket, J10.<br>In Position B, the SCLK input is provided by the EVAL-CED1Z. |
| LK28 | This link option selects the destination of the serial data output ($D_{OUT}A$).<br>In Position A, the data is supplied to the EVAL-CED1Z.<br>In Position B, the data is supplied to the external SMB socket, J11. |
| LK29 | This link option selects the destination of the serial data output ($D_{OUT}B$).<br>In Position A, the data is supplied to the EVAL-CED1Z.<br>In Position B, the data is supplied to the external SMB socket, J12. |
| LK30 | Not populated. |

| Link No. | Description |
|---|---|
| LK31 | This link option adds a 50 Ω termination to AGND at the V1 DIFF socket (J17) for differential operation.<br>This link is removed when using the single-ended-to-differential converter.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to VI DIFF socket (J17). This link should be inserted if this circuit is not being used to ground the input to U5-B. |
| LK32 and LK34 | These link options are used in conjunction with each other to set up the AD8022 (U5) dual op amp configuration to convert either a bipolar or unipolar single-ended signal into a differential signal centered on the common-mode voltage.<br>Both links should be closed when the bipolar analog input signal biased around 0 V is applied to J17.<br>Both links should be open when a unipolar analog input biased around 2.5 V is applied to J17.<br>LK32 should be closed when this circuit is not being used. |
| LK33 | This link option selects the common-mode voltage applied to U5-A, the AD8022 dual op amp configuration used to perform single-ended-to-differential conversion on the analog input.<br>In Position A, an external common-mode voltage can be applied to U5-A via J18.<br>In Position B, the $+V_S$ input to the AD8022 is tied to AGND, in which case the AD8022 dual op amp is not used.<br>In Position C, a portion of $V_{REF}$ is applied to U5-A to set up the common-mode voltage. |
| LK35 | Not populated. |
| LK36 | This link option adds a 50 Ω termination to AGND at the V2 DIFF socket (J19) used for differential operation.<br>This link is removed when using the single-ended-to-differential converter.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to the V2 DIFF socket (J19). This link should be inserted if this circuit is not being used to ground the input to U6-B. |
| LK37 and LK39 | These link options are used in conjunction with each other to set up the AD8022 (U6) dual op amp configuration to convert either a bipolar or unipolar single-ended signal into a differential signal centered on the common-mode voltage.<br>Both links should be closed when the bipolar analog input signal biased around 0 V is applied to J19.<br>Both links should be open when a unipolar analog input biased around 2.5 V is applied to J19.<br>LK39 should be closed when this circuit is not being used. |
| LK38 | This link option selects the common-mode voltage applied to U6-A, the AD8022 dual op amp configuration used to perform single-ended-to-differential conversion on the analog input.<br>In Position A, an external common-mode voltage can be applied to U6-A via J19.<br>In Position B, the +IN input is tied to AGND, in which case the AD8022 dual op amp is not used.<br>In Position C, a portion of $V_{REF}$ is applied to U6-A to set up the common-mode voltage. |
| LK40 | Not populated. |
| LK41 | This link option adds a 50 Ω termination to AGND at the V3 DIFF socket (J20) for differential operation.<br>This link is removed when using the single-ended-to-differential converter.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to the V3 DIFF socket (J20). This link should be inserted if this circuit is not being used to ground the input to U7-B. |
| LK42 and LK44 | These link options are used in conjunction with each other to set up the AD8022 (U7) dual op amp configuration to convert either a bipolar or unipolar single-ended signal into a differential signal centered on the common-mode voltage.<br>Both links should be closed when the bipolar analog input signal biased around 0 V is applied to J20.<br>Both links should be open when a unipolar analog input biased around 2.5 V is applied to J20.<br>LK42 should be closed when this circuit is not being used. |
| LK43 | This link option selects the common-mode voltage applied to U7-A, the AD8022 dual op amp configuration used to perform single-ended-to-differential conversion on the analog input.<br>In Position A, an external common-mode voltage can be applied to U7-A via J21.<br>In Position B, the +IN input is tied to AGND, in which case the AD8022 dual op amp is not used.<br>In Position C, a portion of $V_{REF}$ is applied to U7-A to set up the common-mode voltage. |
| LK45 | Not populated. |
| LK46 | This link option adds a 50 Ω termination to AGND at the V4 DIFF socket (J22) for differential operation.<br>This link is removed when using the single-ended-to-differential converter.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to the V4 DIFF socket (J22). This link should be inserted if this circuit is not being used to ground the input to U8-B. |
| LK47 and LK49 | These link options are used in conjunction with each other to set up the AD8022 (U8) dual op amp configuration to convert either a bipolar or unipolar single-ended signal into a differential signal centered on the common-mode voltage.<br>Both links should be closed when the bipolar analog input signal biased around 0 V is applied to J22.<br>Both links should be open when a unipolar analog input biased around 2.5 V is applied to J22.<br>LK47 should be closed when this circuit is not being used. |

| Link No. | Description |
|---|---|
| LK48 | This link option selects the common-mode voltage applied to U8-A, the AD8022 dual op amp configuration used to perform single-ended-to-differential conversion on the analog input.<br>In Position A, an external common-mode voltage can be applied to U8-A via J23.<br>In Position B, the +IN input is tied to AGND, in which case the AD8022 dual op amp is not used.<br>In Position C, a portion of $V_{REF}$ is applied to U8-A to set up the common-mode voltage. |
| LK50 | This link option sets the dc bias voltage level that is applied to the optional bias-up circuit used in single-ended mode.<br>In Position A, the bias voltage is set to $V_{REF}/2$. This configuration is used in 0 V to 2 $V_{REF}$ mode to set up the bias voltage for a bipolar single-ended signal.<br>In Position B, the bias voltage is set to $V_{REF}/4$. This configuration is used in 0 V to $V_{REF}$ mode to set up the bias voltage for a bipolar single-ended signal. |
| LK51 | This link option adds a 50 Ω termination to AGND at the VIN A socket (J26) of the bias-up circuit for the single-ended input.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to the VIN A socket (J26). This link should be inserted if this circuit is not being used to ground the –IN input terminal of U10-A. |
| LK52 | This link option sets the dc bias voltage that is applied to the optional bias-up circuit used in single-ended mode.<br>In Position A, the bias voltage is set to $V_{REF}/2$. This configuration is used in 0 V to 2 $V_{REF}$ mode to set up the bias voltage for a bipolar single-ended signal.<br>In Position B, the bias voltage is set to $V_{REF}/4$. This configuration is used in 0 V to $V_{REF}$ mode to set up the bias voltage for a bipolar single-ended signal. |
| LK53 | This link option adds a 50 Ω termination to AGND at the VIN B socket (J27) of the bias-up circuit for the single-ended input.<br>When this link is inserted, a 50 Ω termination is added to the input signal applied to the VIN B socket (J27). This link should be inserted if this circuit is not being used to ground the –IN input terminal of U11-B. |
| LK54 | Not populated. |
| LK55 | Not populated. |
| LK56 | This link option is used to select the source of the V– (–12 V) supply, which is used to power the op amps.<br>In Position A, V– is supplied by the EVAL-CED1Z through the 96-way connector.<br>In Position B, V– is supplied from an external source via the power connector, J30. |
| LK57 | This link option is used to select the source of the V+ (+12 V) supply, which is used to power the op amps.<br>In Position A, V+ is supplied by the EVAL-CED1Z through the 96-way connector.<br>In Position B, V+ is supplied from an external source via the power connector, J30. |

## SETUP CONDITIONS

Take care to ensure that all link positions are set according to the required operating mode before applying power and signals to the evaluation board. There are a few different modes in which to operate the evaluation board. Either the user can operate the board with the EVAL-CED1Z or it can be used as a standalone board. The board can accept differential and single-ended analog input voltages.

Table 2 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, the assumption is that the user is operating with the EVAL-CED1Z. The links are set so that all power supplies and control signals are supplied by the EVAL-CED1Z. The board is configured for single-ended mode of operation on $V_{A1}$ and $V_{B1}$ with a 0 V to $V_{REF}$ input range. The AD780 provides an external reference voltage. If the differential mode of operation is required, the link positions must be configured as outlined in Table 4, Table 5, and Table 6.

**Table 2. Link Positions on the Packaged EVAL-AD7265/AD7266 (Single-Ended Mode of Operation, Channel $V_{A1}$ and $V_{B1}$ Selected)**

| Link No. | Position | Function |
|---|---|---|
| LK1 | A | $V_{A1}$ input is supplied from the output of the unity gain buffer U3-A. In this case, a unipolar signal must be applied to the SVIN1 socket via J13. |
| LK2 | C | $V_{A2}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{A2}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN2 SMB (J14). |
| LK3 | C | $V_{A3}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{A3}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN1 SMB (J13). |
| LK4 | C | $V_{A4}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{A4}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN2 SMB (J14). |
| LK5 | C | $V_{A5}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{A5}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN1 SMB (J13). |
| LK6 | C | $V_{A6}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{A6}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN2 SMB (J14). |
| LK7 | A | $V_{B1}$ is supplied from the output of the unity gain buffer U4-A. In this case, a unipolar signal must be applied to the SVIN1 socket via J15. |
| LK8 | C | $V_{B2}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{B2}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN4 SMB (J16). |
| LK9 | C | $V_{B3}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{B3}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN3 SMB (J15). |
| LK10 | C | $V_{B4}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{B4}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN4 SMB (J16). |
| LK11 | C | $V_{B5}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{B5}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN3 SMB (J15). |
| LK12 | C | $V_{B6}$ input is tied to AGND. Once power supplies are applied to the ADC, this link can be changed to Position A if $V_{B6}$ is to be converted. In this case, a unipolar signal should be applied to the SVIN4 SMB (J16). |
| LK13 | B | The AD780 voltage reference provides a 2.5 V reference to the $D_{CAP}A$ pin. |
| LK14 | B | The AD780 voltage reference provides a 2.5 V reference to the $D_{CAP}B$ pin. |
| LK15 | A | The $V_{DD}$ supply (5 V) for the AD7265/AD7266 is provided by the EVAL-CED1Z. |
| LK16 | Open | The AD780 reference voltage is set to output +2.5 V. |
| LK17 | A | The $V_{DRIVE}$ 3.3 V supply for the AD7265/AD7266 is provided by the EVAL-CED1Z. |
| LK19 | A | REF SELECT is tied to $V_{DRIVE}$ (Logic 1). The AD780 provides an external reference (2.5 V) to the AD7265/AD7266. |
| LK20 | B | RANGE is tied to DGND (Logic 0). The analog input range is 0 V to $V_{REF}$. |
| LK21 | A | SGL/$\overline{DIFF}$ is tied to $V_{DRIVE}$, enabling single-ended mode. If differential mode is required, then this link option should be in Position B. |
| LK22 | B | A0 is controlled by channel selection in the evaluation software. |
| LK23 | B | A1 is controlled by channel selection in the evaluation software. |
| LK24 | C | A2 is held low. This input must be changed manually by the user. |
| LK25 | A | $\overline{CS}$ is provided by the EVAL-CED1Z. |
| LK27 | B | SCLK is provided by the EVAL-CED1Z. |
| LK28 | A | Data from $D_{OUT}A$ is read by the EVAL-CED1Z. |
| LK29 | A | Data from $D_{OUT}B$ is read by the EVAL-CED1Z. |
| LK31 | Closed | The input to U5-B is tied to AGND because it is not used in single-ended mode. |
| LK32, LK34 | Closed | The inputs to U5-A are tied to AGND because they are not used in single-ended mode. |

| Link No. | Position | Function |
|---|---|---|
| LK33 | B | The input to U5-A is tied to AGND because it is not used in single-ended mode. |
| LK36 | Closed | The input to U6-B is tied to AGND because it is not used in single-ended mode. |
| LK37, LK39 | Closed | The inputs to U6-A are tied to AGND because they are not used in single-ended mode. |
| LK38 | B | The input to U6-A is tied to AGND because it is not used in single-ended mode. |
| LK41 | Closed | The input to U7-B is tied to AGND because it is not used in single-ended mode. |
| LK42, LK44 | Closed | The inputs to U7-A are tied to AGND because they are not used in single-ended mode. |
| LK43 | B | The input to U7-A is tied to AGND because it is not used in single-ended mode. |
| LK46 | Closed | The input to U8-B is tied to AGND because it is not used in single-ended mode. |
| LK47, LK49 | Closed | The inputs to U8-A are tied to AGND because they are not used in single-ended mode. |
| LK48 | B | The input to U8-A is tied to AGND because it is not used in single-ended mode. |
| LK50 | B | The bias input for U12-A is set to $V_{REF}/4$. |
| LK51 | Open | Bias-up circuit is in use. |
| LK52 | B | The bias input for U12-B is set to $V_{REF}/4$. |
| LK53 | Open | Bias-up circuit is in use. |
| LK56 | A | V− is supplied by the EVAL-CED1Z. |
| LK57 | A | V+ is supplied by the EVAL-CED1Z. |

**Table 3. Link Positions for Single-Ended Mode of Operation with a 0 V to 2 $V_{REF}$ Input Range When a Bipolar Single-Ended Signal Is Used**

| Link No. | Position | Function |
|---|---|---|
| LK20 | A | RANGE is tied to $V_{DRIVE}$ (Logic 1). The analog input range is 0 V to 2 $V_{REF}$. |
| LK21 | A | SGL/$\overline{\text{DIFF}}$ is tied to $V_{DRIVE}$, enabling single-ended mode. |
| LK50 | A | The bias input for U12-A is set to $V_{REF}/2$. |
| LK51 | Open | Bias-up circuit is in use. |
| LK52 | A | The bias input for U12-B is set to $V_{REF}/2$. |
| LK53 | Open | Bias-up circuit is in use. |

**Table 4. Link Positions for Differential Mode of Operation with a 0 V to $V_{REF}$ Input Range When a Bipolar Single-Ended Signal Is Used with the Single-Ended-to-Differential Converter**

| Link No. | Position | Function |
|---|---|---|
| LK1 | B | $V_{A1}$ is supplied from the positive output (V1+) of the single-ended-to-differential converter, U5-B, in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK2 | B | $V_{A2}$ is supplied from the negative output (V1-) of the single-ended-to-differential converter U5-A in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK20 | B | The RANGE pin is tied to DGND (Logic 0). Therefore, the analog input range is 0 V to $V_{REF}$. |
| LK21 | B | The ADC is tied to DGND and, therefore, the ADC is configured to operate in differential mode. |
| LK31 | Open | The single-ended-to-differential converter, U5-B, is in use. |
| LK32, LK34 | Closed | These links should be closed when the bipolar analog input signal biased around 0 V is applied to J17. |
| LK33 | C | A portion of $V_{REF}$ is applied to U5-A to set up the common-mode voltage. |

**Table 5. Link Positions for Differential Mode of Operation with a 0 V to 2 $V_{REF}$ Input Range When a Bipolar Single-Ended Signal Is Used with the Single-Ended-to-Differential Converter**

| Link No. | Position | Function |
|---|---|---|
| LK1 | B | $V_{A1}$ is supplied from the positive output (V1+) of the single-ended-to-differential converter, U5-B, in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK2 | B | $V_{A2}$ is supplied from the negative output (V1−) of the single-ended-to-differential converter, U5-A, in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK20 | A | The RANGE pin is tied to $V_{DRIVE}$ (Logic 1). Therefore, the device is configured for an analog input range of 0 V to 2 $V_{REF}$. |
| LK21 | B | The ADC is tied to DGND and, therefore, the ADC is configured to operate in differential mode. |
| LK31 | Open | The single-ended-to-differential converter, U5-B, is in use. |
| LK32, LK34 | Closed | These links should be closed as the bipolar analog input signal biased around 0 V is applied to J17. |
| LK33 | C | A portion of $V_{REF}$ is applied to U5 to set up the common-mode voltage. |

**Table 6. Link Positions for Differential Mode of Operation When a Unipolar Input Signal Is Used with the Single-Ended-to-Differential Converter**

| Link No. | Position | Function |
|---|---|---|
| LK1 | B | $V_{A1}$ is supplied from the positive output (V1+) of the single-ended-to-differential converter, U5, in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK2 | B | $V_{A2}$ is supplied from the negative output (V1−) of the single-ended-to-differential converter, U5, in which case a single-ended signal must be applied to V1 DIFF via Socket J17. |
| LK21 | B | The ADC is tied to DGND and, therefore, the ADC is configured to operate in differential mode. |
| LK31 | Open | The single-ended to differential converter, U5, is in use. |
| LK32, LK34 | Open | These links should be open as the bipolar analog input signal biased around 2.5 V is applied to J17. |
| LK33 | C | A portion of $V_{REF}$ is applied to U5-A to set up the common-mode voltage. |
| LK50 | A | The bias input for U12-A is set to $V_{REF}/2$. |

## SOCKETS

There are 25 SMB input/output sockets relevant to the operation of the AD7265/AD7266 on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board or for accessing an output signal from the AD7265/AD7266. When operating the board with the EVAL-CED1Z board, the only external sockets necessary are those used to supply the analog input signals to the ADC (that is, $V_{A1}$ to $V_{A6}$ and $V_{B1}$ to $V_{B6}$). All of the other sockets are optional and if they are not used, their signals are supplied by the EVAL-CED1Z. Most of these sockets are used when operating the board as a standalone unit because all the signals required are supplied from external sources. The functions of these sockets are outlined in Table 8.

## CONNECTORS

There are four connectors on the EVAL-AD7265/AD7266 as outlined in Table 7.

**Table 7. Connector Functions**

| Connector | Function |
|---|---|
| J1 | 96-way connector for the digital interface and power supply connections |
| J2 | External $V_{DD}$ power connector |
| J3 | External $V_{DRIVE}$ power connector |
| J30 | External +12 V, −12 V and AGND power connector |

**Table 8. Socket Functions**

| Reference Designator | Socket | Function |
|---|---|---|
| J5 | EXT COM2 | Subminiature BNC socket for an external common-mode voltage to be applied to U6. |
| J6 | A0 | Subminiature BNC socket for an external A0 logic level. |
| J7 | A1 | Subminiature BNC socket for an external A1 logic level. |
| J8 | A2 | Subminiature BNC socket for an external A2 logic level. |
| J9 | $\overline{CS}$ | Subminiature BNC socket for an external $\overline{CS}$ signal. |
| J10 | SCLK | Subminiature BNC socket for an external SCLK input. |
| J11 | DOUTA | Subminiature BNC socket for the $D_{OUT}A$ output. |
| J12 | DOUTB | Subminiature BNC socket for $D_{OUT}B$ output. |
| J13 | SVIN1 | Subminiature BNC socket for a unipolar signal that is buffered by U3-A and applied to the ADC. |
| J14 | SVIN2 | Subminiature BNC socket for a unipolar signal that is buffered by U3-B and applied to the ADC. |
| J15 | SVIN3 | Subminiature BNC socket for a unipolar signal that is buffered by U4-A and applied to the ADC. |
| J16 | SVIN4 | Subminiature BNC socket for a unipolar signal that is buffered by U4-B and applied to the ADC. |
| J17 | V1 DIFF | Subminiature BNC socket for a bipolar or unipolar single-ended input that is applied to the single-ended-to-differential conversion circuit (U5-B). |
| J18 | EXT COM1 | Subminiature BNC socket for an external common-mode voltage to be applied to U6. |
| J19 | V2 DIFF | Subminiature BNC socket for a bipolar or unipolar single-ended input that is applied to the single-ended-to-differential conversion circuit (U6-B). |
| J20 | V3 DIFF | Subminiature BNC socket for a bipolar or unipolar single-ended input that is applied to the single-ended to-differential conversion circuit (U7-B). |
| J21 | EXT COM3 | Subminiature BNC socket for an external common-mode voltage to be applied to U7. |
| J22 | V4 DIFF | Subminiature BNC socket for a bipolar or unipolar single-ended input that is applied to the single-ended to-differential conversion circuit (U8-B). |
| J23 | EXT COM4 | Subminiature BNC socket for an external common-mode voltage applied to U8. |
| J24 | DCAPA | Subminiature BNC socket for an external reference voltage to be applied to $D_{CAP}A$ or to access the internal reference from the AD7265/AD7266. |
| J25 | DACPB | Subminiature BNC socket for an external reference voltage to be applied to $D_{CAP}B$ or to access the internal reference from the AD7265/AD7266. |
| J26 | VIN A | Subminiature BNC socket for a bipolar single-ended input to be applied to Bias-Up Circuit A. |
| J27 | VIN B | Subminiature BNC socket for a bipolar single-ended input to be applied to Bias-Up Circuit B. |
| J28 | VBIASED-A | Output from Bias-Up Circuit A, which can be applied to SVINx for single-ended mode of operation. |
| J29 | VBIASED-B | Output from Bias-Up Circuit B, which can be applied to SVINx for single-ended mode of operation. |

## INTERFACING THE EVALUATION BOARD TO THE EVAL-CED1Z

Interfacing the EVAL-CED1Z board to the evaluation board is via a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2. Table 9 gives a description of the pins on the 96-way connector that are used to interface the EVAL-CED1Z to the EVAL-AD7265/AD7266.

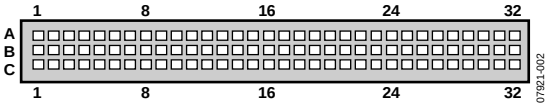


*Figure 2. Pin Configuration for the 96-Way Connector, J1*

**Table 9. The 96-Way Connector Pin Description**

| Signal | Description |
|---|---|
| DR1PRI | Data receive primary. This input is connected to the $D_{OUT}A$ pin of the AD7265/AD7266. |
| DR0SEC | Data receive secondary. This input is connected to the $D_{OUT}B$ pin of the AD7265/AD7266. |
| RSCLK0 | Receive clock. This continuous clock is connected to the SCLK pin of the AD7265/AD7266 via LK27. |
| TFS0 | Transmit frame sync. This output is connected to the $\overline{CS}$ pin of the AD7265/AD7266 via LK25 to frame the serial data transfer. |
| RFS0 | Receive frame sync. This input is connected to the TFS pin on the EVAL-CED1Z to frame the serial data read. |
| $V_{DD}$ | Analog +5 V supply. These lines are connected to the $V_{DD}$ line on the board via LK15. |
| $V_{DRIVE}$ | Digital +3.3 V supply. This is used to provide the $V_{DRIVE}$ supply to the board via LK17 for the digital logic. |
| −5 V | Analog −5 V supply. This supply is not used on the EVAL-AD7265/AD7266. |
| DGND | Digital ground. These lines are connected to the digital ground plane on the evaluation board. |
| AGND | Analog ground. These lines are connected to the analog ground plane on the evaluation board. |
| +12 V | +12 V supply ($V_{CC}$). This line is connected to the +12 V supply line on the board via LK57. |
| −12 V | −12 V supply ($V_{SS}$). This line is connected to the −12 V supply line on the board via LK56. |
| FL0 | Flag zero. This output is connected to the A0 pin of the AD7265/AD7266 via LK22. |
| GPIO3 | General-purpose input/output. This input is connected to the A1 pin of the AD7265/AD7266 via LK23. |

**Table 10. 96-Way Connector Pin Functions[1]**

| Pin | Row A | Row B | Row C |
|---|---|---|---|
| 1 | DT1PRI | GPIO3 | DR1PRI |
| 2 | TFS1 | | RFS1 |
| 3 | TSCLK1 | | RSCLK1 |
| 4 | DGND | DGND | DGND |
| 5 | DT0PRI | | DR0PRI |
| 6 | TFS0 | | RFS0 |
| 7 | TSCLK0 | | RSCLK0 |
| 8 | $V_{DRIVE}$ (+3.3 V) | $V_{DRIVE}$ (+3.3 V) | $V_{DRIVE}$ (+3.3 V) |
| 9 | | | |
| 10 | | | |
| 11 | DT0SEC | | GPIO6 |
| 12 | DGND | DGND | DGND |
| 13 | | | DR0SEC |
| 14 | GPIO5 | | GPIO7 |
| 15 | GPIO0 | | GPIO4 |
| 16 | DGND | DGND | DGND |
| 17 | FL0 | | GPIO2 |
| 18 | | | |
| 19 | | GPIO1 | |
| 20 | DGND | DGND | DGND |
| 21 | AGND | AGND | AGND |
| 22 | AGND | AGND | AGND |
| 23 | AGND | AGND | AGND |
| 24 | AGND | AGND | AGND |
| 25 | AGND | AGND | AGND |
| 26 | AGND | AGND | AGND |
| 27 | | AGND | |
| 28 | | AGND | |
| 29 | AGND | AGND | AGND |
| 30 | −12 V | AGND | +12 V |
| 31 | −5 V | −5 V | −5 V |
| 32 | $V_{DD}$ (+5 V) | $V_{DD}$ (+5 V) | $V_{DD}$ (+5 V) |

[1] The unused pins of the 96-way connector are not shown.

## TEST POINTS

There are two test points on the inputs to the AD7265/AD7266 on the evaluation board. Test points enable the user to have easy access to various signals on the EVAl-AD7265/AD7266, facilitating probing, evaluation, and debugging.

## OPERATING WITH THE EVAL-CED1Z

The evaluation board can be operated in a standalone mode or it can be operated in conjunction with the EVAL-CED1Z. This evaluation board controller is available from Analog Devices under the order entry, EVAL-CED1Z.

When interfacing the EVAL-AD7265/AD7266 directly to the EVAL-CED1Z board, all supplies and control signals to operate the AD7265/AD7266 board are provided by the EVAL-CED1Z. The AD7266 can operate at 2 MSPS with SCLK frequencies up to 32 MHz, and the AD7265 can operate with a 16 MHz SCLK to give a 1 MSPS throughput. The SCLK frequency supplied by the EVAL-CED1Z is fixed at 32 MHz for the AD7266. The software allows the user to change the throughput rate by effectively modifying the $\overline{CS}$ high time.

Software to communicate with the EVAL-CED1Z and AD7265/AD7266 is provided with the AD7266/AD7266 evaluation board package.

The 96-way connector on the EVAL-AD7265/AD7266 plugs directly into the 96-way connector on the EVAL-CED1Z. The evaluation board is powered from a 7 V, 15 W power supply that accepts input voltages from 100 V to 240 V ac, and contains the relevant adaptors for worldwide use.

Connection between the EVAL-CED1Z and the USB port of a PC is via a standard USB 2.0 connection cable that is provided as part of the EVAL-CED1Z package.

# EVALUATION BOARD SOFTWARE

## INSTALLING THE SOFTWARE

The EVAL-AD7265/AD7266 evaluation kit includes self-installing software on a CD-ROM for controlling and evaluating the performance of the AD7265/AD7266 when it is operated with the EVAL-CED1Z board. The software is compatible with Windows® 2000/XP®. If the setup file does not run automatically, **setup.exe** can be run from the CD-ROM.

When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The user interface on the PC is a dedicated program written especially for the AD7265/AD7266 when operating with the EVAL-CED1Z board.

Install the software before the USB cable is connected between the EVAL-CED1Z and the PC. This ensures that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

When the software is run for the first time with the EVAL-CED1Z connected to the PC, the PC automatically finds the new device and identifies it. Follow the onscreen instructions that appear automatically. This installs the drivers for the EVAL-CED1Z on the PC. If an error appears onscreen when the software is first opened, then the PC is not recognizing the USB device. To correct this error,

1. Right-click the **My Computer** icon, then select **Properties**. When the **System Properties** window opens, select the **Hardware** tab.
2. Click **Device Manager** in the **Hardware Tab** of the **System Properties** window.
3. Examine the devices listed under the **Universal Serial Bus Controller** heading.
4. If an unknown device is listed, right-click this option and select **Update Driver**.
   The **New Hardware Wizard** runs twice. Under **ADI Development Tools**, the hardware is listed as **ADI Converter Evaluation and Development Board (WF)**.
5. Reboot your PC.

## SETTING UP THE EVAL-CED1Z

This section describes how the evaluation board, the EVAL-CED1Z, and the software should be set up to begin using the complete system.

1. Install the AD7265/AD7266 evaluation board software.
2. Connect the EVAL-CED1Z and the evaluation board together via the 96-way connector. Apply power to the EVAL-CED1Z via the provided 7 V, 15 W power supply. At this stage, the green LED labeled **Power** on the EVAL-CED1Z should light up, which indicates that the EVAL-CED1Z is receiving power.
3. Connect the USB cable between the PC and the EVAL-CED1Z. A green LED positioned beside the USB connector on the EVAL-CED1Z lights up, indicating that the USB connection has been established.
4. The EVAL-AD7265/AD7266 are detected. Proceed through any dialog boxes that may appear (use the recommended options) to finalize the installation.
5. Start the EVAL-AD7265/AD7266 software.

The FPGA on the EVAL-CED1Z is automatically programmed when the software is opened. The two red LEDs (D14 and D15) on the EVAL-CED1Z now light up. This indicates that the EVAL-CED1Z is functional and ready to receive instructions.

## SOFTWARE OPERATION

With the hardware set up, you can now use the software to control the EVAL-CED1Z and the AD7266 or AD7265 evaluation board. To launch the software, from the **Analog Devices** menu, select the **AD7266/AD7265** submenu, and then click the **AD7266/AD7265** icon.

Figure 3 displays the main window that is opened. If an error message appears, click **OK** and restart the application after checking the connection between the adapter board and the USB port on the PC. Also check that the USB device is identified by the **Device Manager** as detailed in the Installing the Software Section.

The software that controls the EVAL-CED1Z and, therefore, the AD7265/AD7266 evaluation board, has two main windows.

Figure 3 shows the window that appears when the software is run. The main function of this window is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain. The window can be divided into three main sections: **Part Information**, **Data Capture**, and **Linearity**. The menu bar is located at the top portion of the window, with the **Part Information** panel on the left-hand side of the window. The **Data Capture** and **Linearity** tabs are in the center. The **Data Capture** tab consists of four subtabs: **Waveform**, **Histogram**, **FFT**, and **Summary**. The **Linearity** tab, which enables you to generate a linearity plot for the device, consists of three subtabs: **Histogram**, **INL**, and **DNL**.

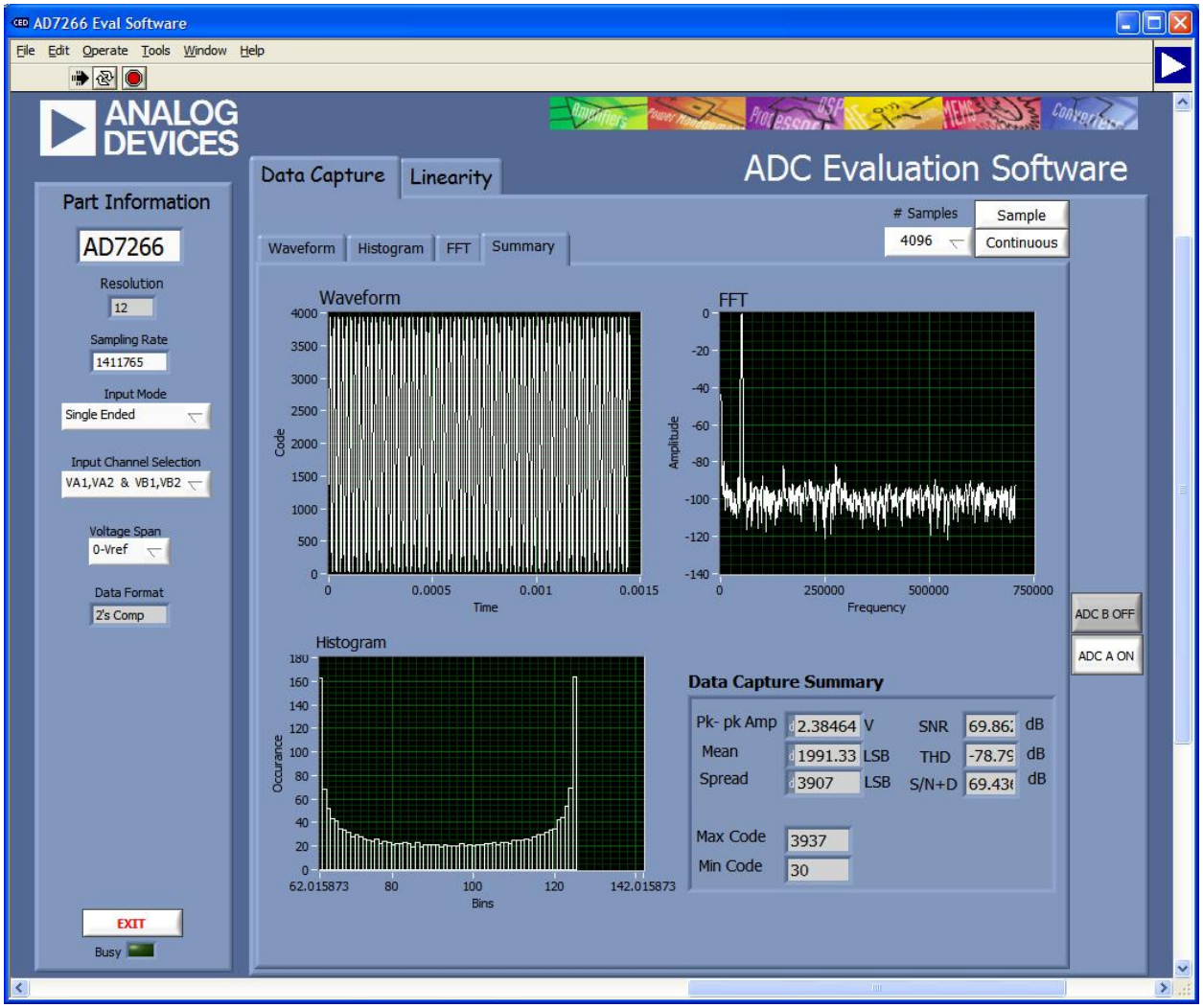


*Figure 3. AD7266 Main Window*

## USING THE SOFTWARE

### *Menu Bar*

The menu bar consists of the following menus: **File**, **Edit**, **Operate**, **Tools**, **Window**, and **Help**.

### *Part Information Panel*

The **Part Information** panel allows you to select the following configuration options:

- The part number box allows you to select the part being tested by typing in the appropriate part number, either AD7265 or AD7266.
- **Sampling Rate** allows you to set the sampling frequency. The maximum sampling frequency supported by the EVAL-AD7265/AD7266 is 1.4 MSPS for the AD7266 and 1 MSPS for the AD7265.
- **Input Mode** allows you to select from single-ended, differential, or pseudodifferential mode.
- **Input Channel Selection** allows you to select the pair of channels for conversion. This channel selection option must be used in conjunction with LK24 on the board. Alternatively, LK22, LK23, and LK24 can be used instead to select the channels for conversion in the hardware, in which case this option is not used.
- **Voltage Span** allows you to select between 0 V to $V_{REF}$ and 0 V to 2 $V_{REF}$ mode of operation.

The **Part Information** tab also provides the following information:

- **Resolution**. The software automatically sets the resolution at 12 bits.
- **Data Format**. The software automatically sets the data output format to straight binary or twos complement.

The **Part Information** tab also includes a **Busy** status indicator that lights when the evaluation board is busy, and an **Exit** button that allows you to quit the program.

### *Data Capture Tab*

In the **Data Capture** tab, you can select the number of samples to be captured from the **# Samples** drop-down box. The default number of samples is 4096; you are free to change this as required. The desired display option is selected by clicking one of the **Waveform**, **Histogram**, or **FFT** tabs.

#### Waveform Tab

The **Waveform** subtab displays a digital storage oscilloscope (DSO) that allows you to display a waveform. When samples are uploaded from the EVAL-CED1Z board, they are displayed here. The samples are displayed as integer code values.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out for a closer look at a sample, if required. The **Waveform Analysis** section, which is located beneath the waveform graph, contains information about the samples taken, for example, the minimum/maximum position or velocity, the spread, the standard deviation, and the mean.

The waveform graph displays the information for both ADC A and ADC B, or either ADC as desired. Two buttons located on the bottom right-hand side of the graph, labeled **ADC A ON/OFF** and **ADC B ON/OFF** are used to select which ADC's data is displayed. An indicator, located on the top right-hand corner of the graph, shows what color graph represents each ADC when the data from both ADCs is displayed.

#### Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the ADC's performance in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example, maximum and minimum codes captured.

#### FFT Tab

This tab displays a fast Fourier transform (FFT) plot. The FFT is typically used for examining the ADC's performance in the frequency domain. The **Spectrum Analysis** section contains information about the samples taken, for example, ac specifications. You can choose whether to display the information for ADC A, or ADC B, or both in the window using the **ADC A ON/OFF** and **ADC B ON/OFF** buttons, as explained in the Waveform Tab section.

#### Summary Tab

This tab shows a summary of the information displayed in each of the discrete tabs; that is, the waveform, histogram and FFT plots.

### *Linearity Tab*

In the **Linearity** tab, you can select the number of hits per code to be captured for the linearity analysis. The desired display option is selected by clicking the **Histogram**, **INL**, **DNL**, or **Summary** tabs. To initiate the data collection, click the **Get Linearity Data** button. The data collection and analysis takes a few seconds to complete. The greater the number of hits per code selected, the longer the analysis takes.

#### Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the ADC's performance in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example, maximum and minimum codes captured.

#### INL Tab

The **INL** tab displays an INL plot for the AD7266 or AD7265. This plot can be used to examine the dc performance of the ADC. The **Linearity Analysis** section contains information on the maximum and minimum INL error and the code at which this error occurred. It also shows the total number of hits per code and the number of samples taken.

### DNL Tab

The **DNL** tab displays a DNL plot for the AD7266 or AD7265. This plot can be used to examine the dc performance of the ADC in conjunction with the INL plot. The **Linearity Analysis** section contains information on the maximum and minimum DNL error and the code at which this error occurred.

## TAKING SAMPLES

To initiate a conversion and capture the sample data, you must click the **Sample** button or the **Continuous** button. Both the **Sample** and the **Continuous** buttons are located on the top right-hand corner of the **Data Capture** tab. When you click the **Sample** button, the software instructs the EVAL-CED1Z to take the required number of samples at the required frequency from the evaluation board. The AD7266 evaluation board runs with a sampling speed less than or equal to 2 MSPS, and the AD7265 evaluation board runs with a sampling speed less than 1 MSPS. You can choose the sampling frequency up to this rate and the number of samples to be taken.

The samples taken are then uploaded and displayed. An FFT and/or histogram can be calculated and displayed. If you click the **Continuous** button, the software repeats the process indefinitely until you click **Stop.** (The **Continuous** button switches to **Stop** when clicked). You can switch between displaying data from ADC A, ADC B, or both while the software is running continuously.

# EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-AD7265/AD7266 schematics, silkscreen, and layout can be found in Figure 4 to Figure 9.

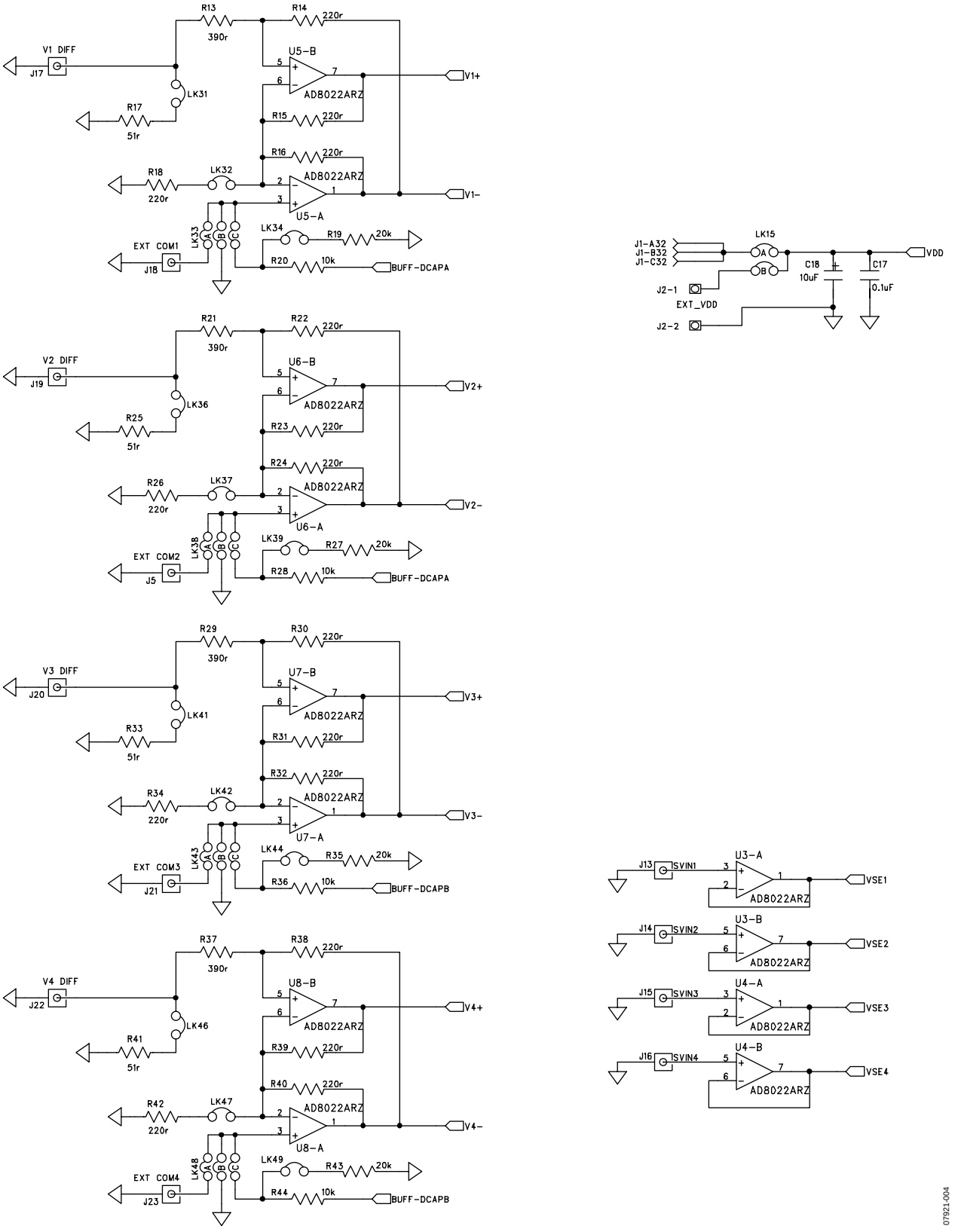


*Figure 4. AD7265/AD7266 Evaluation Board Circuit Diagram 1*

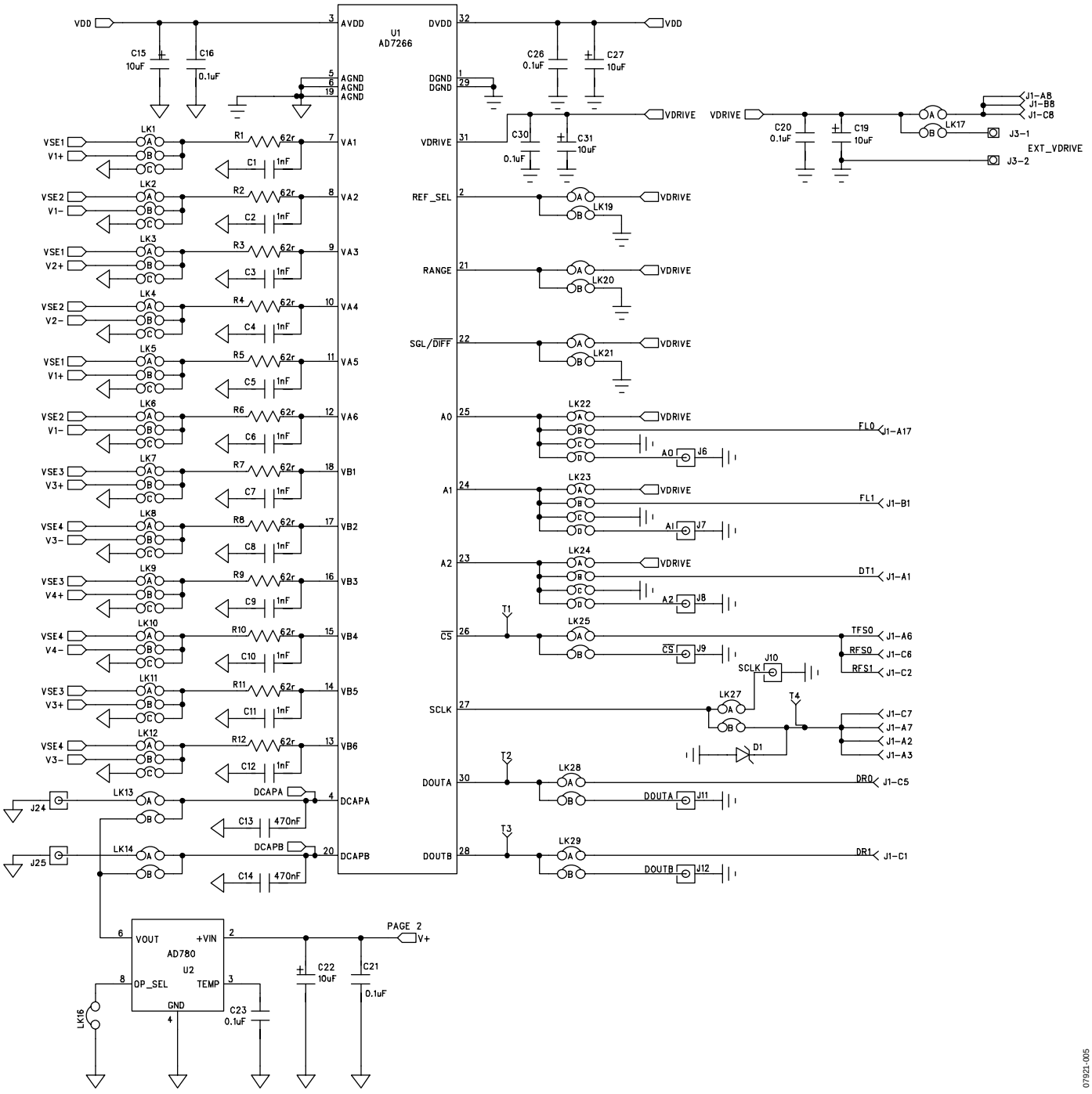


*Figure 5. AD7265/AD7266 Evaluation Board Circuit Diagram 2*

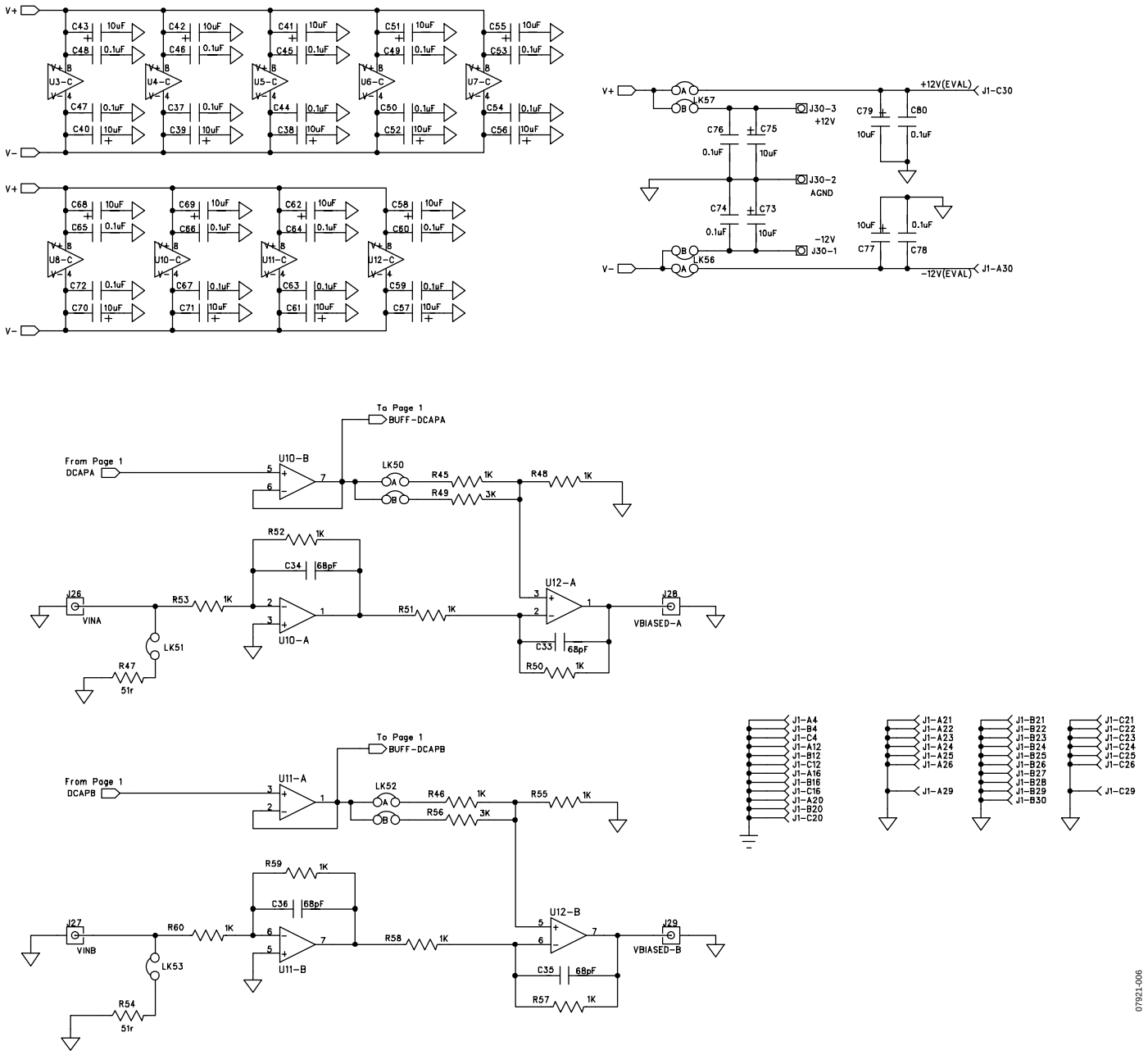


*Figure 6. AD7265/AD7266 Evaluation Board Circuit Diagram 3*

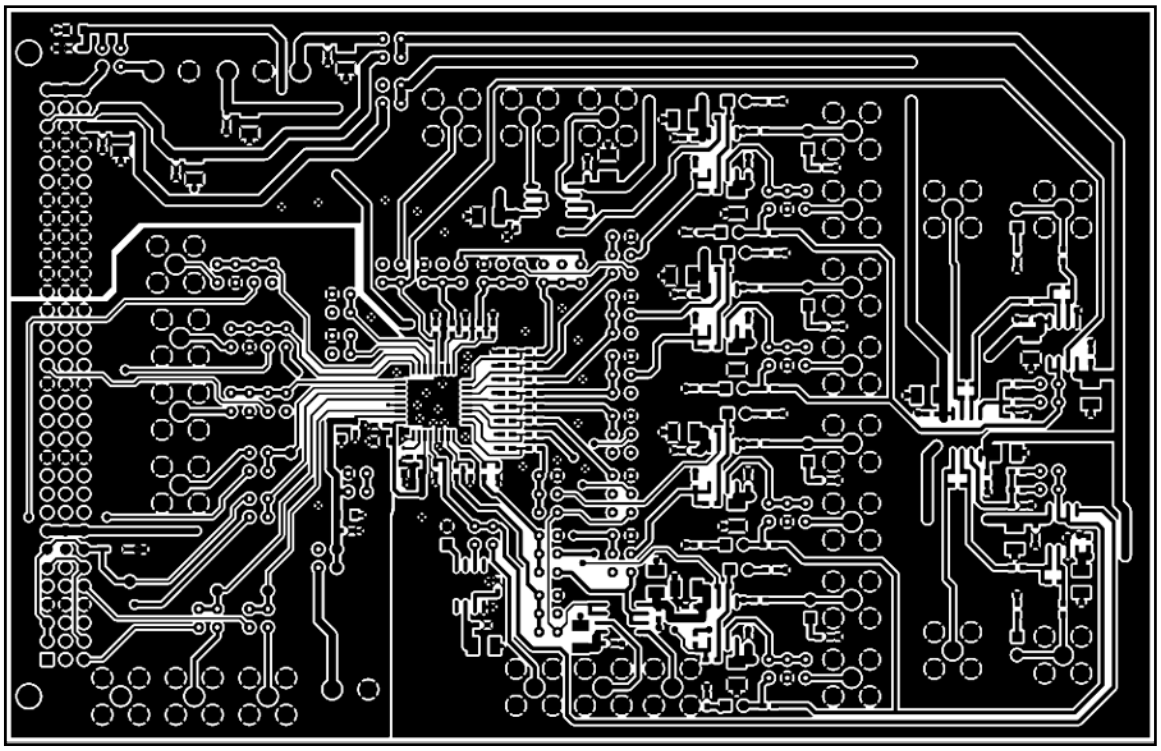


*Figure 7. AD7265/AD7266 Evaluation Board PCB Layout—Component Side*

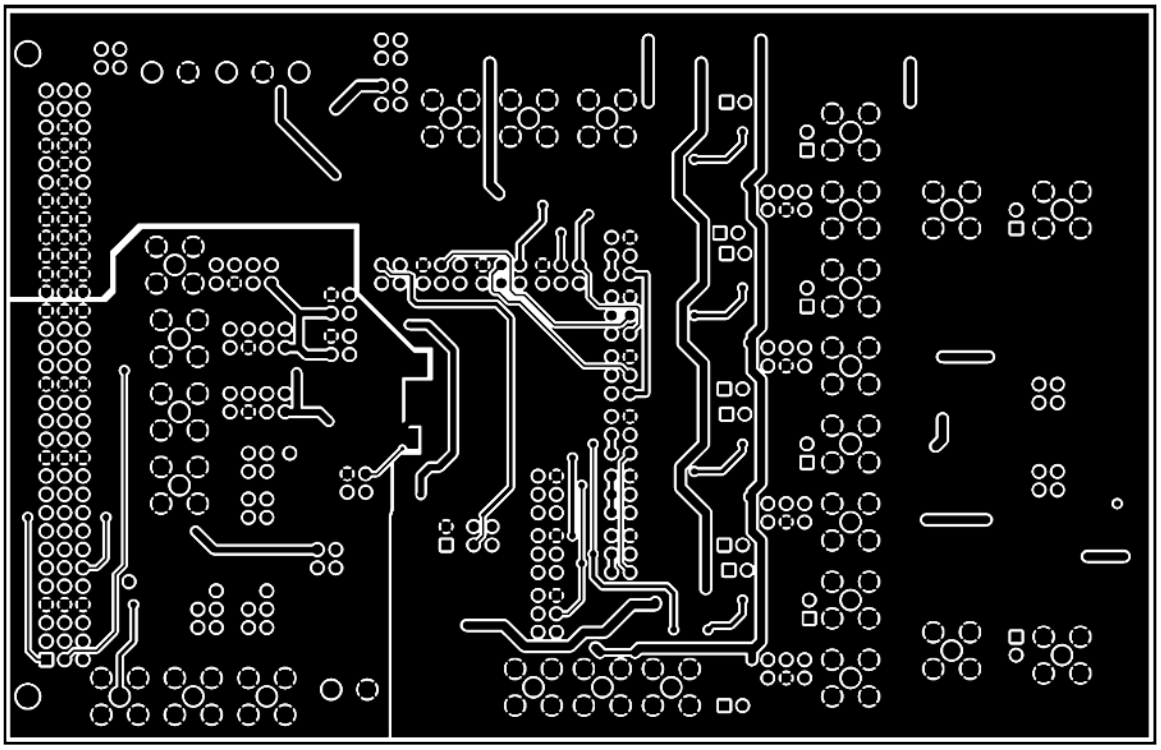


*Figure 8. AD7265/AD7266 Evaluation Board PCB Layout—Solder Side*

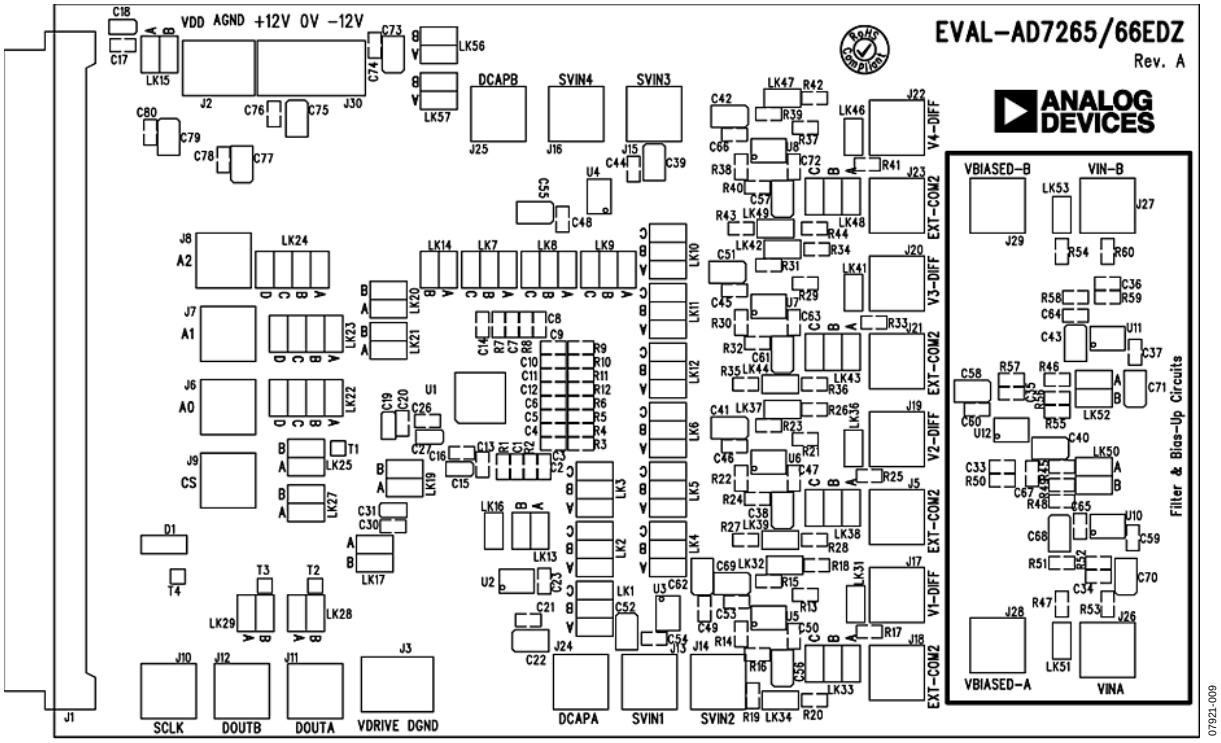


*Figure 9. AD7265/AD7266 Evaluation Board PCB Layout—Silkscreen*

# ORDERING INFORMATION

## BILL OF MATERIALS

**Table 11.**

| Qty | Reference Designator | Description | Supplier/Number[1] |
|---|---|---|---|
| 6 | R17, R25, R33, R41, R47, R54 | 51 Ω resistor | FEC 9331336 |
| 12 | R1 to R12 | 62 Ω resistor | FEC 9331433 |
| 16 | R14 to R16, R18, R22 to R24, R26, R30 to R32, R34, R38 to R40, R42 | 220 Ω resistor | FEC 9330801 |
| 4 | R13, R21, R29, R37 | 390 Ω resistor | FEC 9331131 |
| 12 | R45, R46, R48, R50 to R53, R55, R57 to R60 | 1 kΩ resistor | FEC 9330380 |
| 2 | R49, R56 | 3 kΩ resistor | FEC 9330976 |
| 4 | R20, R28, R36, R44 | 10 kΩ resistor | FEC 9330399 |
| 4 | R19, R27, R35, R43 | 20 Ω resistor | FEC 9330771 |
| 4 | C33 to C36 | 68 pF capacitor | FEC 722-066 |
| 12 | C1 to C12 | 1 nF capacitor | FEC 722-170 |
| 2 | C13, C14 | 470 nF capacitor | FEC 318-8851 |
| 29 | C16, C17, C20, C21, C23, C26, C30, C37, C44 to C50, C53, C54, C59, C60, C63 to C67, C72, C74, C76, C78, C80 | 0.1 µF capacitor | FEC 432-210 |
| 28 | C15, C18, C19, C22, C27, C31, C38 to C43, C51, C52, C55 to C58, C61, C62, C68 to C71, C73, C75, C77, C79 | 10 µF, 10 V capacitor | FEC 197-130 |
| 1 | U1 | AD7266 or AD7265 ADC | Analog Devices AD7266BSUZ, AD7265BSUZ |
| 1 | U2 | AD780 reference | Analog Devices AD780ARZ |
| 9 | U3 to U8 and U10 to U12 | AD8022 op amp | Analog Devices AD8022ARZ |
| 1 | D1 | 20 V Schottky diode | Digi-Key SD103CTPMSCT-ND |
| 57 | LK1 to LK57 | Jumper | FEC 1022244 |
| 1 | J1 | 96-way connecter, CON\41612\96 | FEC 1096832 |
| 2 | J2, J3 | Terminal block, 2-way power connector | FEC 3041359 |
| 1 | J30 | Terminal block, 3-way power connector | FEC 3041360 |
| 25 | J5 (EXT COM2), J6 (A0), J7 (A1), J8 (A2), J9 ($\overline{CS}$), J10 (SCLK), J11 (DOUTA), J12 (DOUTB), J13 (SVIN1), J14 (SVIN2), J15 (SVIN3), J16 (SVIN4), J17 (V1 DIFF), J18 (EXT-COM1), J19 (V2 DIFF), J20 (V3 DIFF), J21 (EXT COM3), J22 (V4 DIFF), J23 (EXT COM4), J24 (DCAPA), J25 (DCAPB), J26 (VIN A), J27 (VIN B), J28 (VBIASED-A), J29 (VBIASED-B) | SMB connector | FEC 1111349 |
| 2 | T1, T4 | Test points | FEC 8731144 |

[1] FEC refers to Farnell Electronics.

## ORDERING GUIDE

| Model | Description |
|---|---|
| EVAL-AD7265EDZ[1] | Evaluation Board for AD7265 |
| EVAL-AD7266EDZ[1] | Evaluation Board for AD7266 |
| EVAL-CED1Z[1] | Controller Board |

[1] Z = RoHS Compliant Part.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## NOTES


EB07921-0-4/09(0)