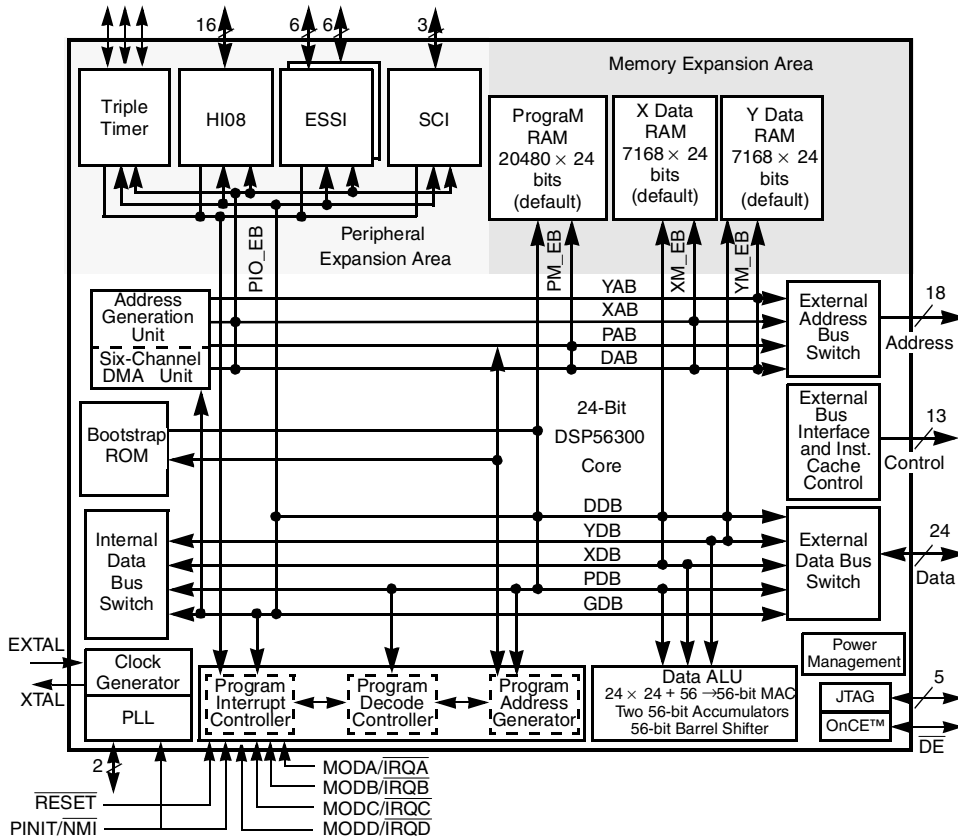


# DSP56309

## 24-Bit Digital Signal Processor



*The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.*

**Figure 1.** DSP56309 Block Diagram

The DSP56309 is a member of the DSP56300 core family of programmable CMOS DSPs. The DSP56300 core includes a barrel shifter, 24-bit addressing, an instruction cache, and direct memory access (DMA). The DSP56309 offers 100 million multiply-accumulates per second (MMACS) at 3.0–3.6 V using an internal 100 MHz clock. The large internal memory is ideal for wireless infrastructure and wireless local-loop applications. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low-power dissipation, thus enabling a new generation of wireless, multimedia, and telecommunications products.

**Note:** This document contains information on a new product. Specifications and information herein are subject to change without notice.

# Features

Table 1 lists the features of the DSP56309 device.

**Table 1.** DSP56309 Features

Feature	Description																														
<b>High-Performance DSP56300 Core</b>	<ul style="list-style-type: none"> <li>• 100 million multiply-accumulates per second (MMACS) with a 100 MHz clock at 3.3 V nominal</li> <li>• Data arithmetic logic unit (Data ALU) with fully pipelined <math>24 \times 24</math>-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control</li> <li>• Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts</li> <li>• Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two- and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals</li> <li>• Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination</li> <li>• Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)</li> </ul>																														
<b>Internal Peripherals</b>	<ul style="list-style-type: none"> <li>• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs</li> <li>• Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)</li> <li>• Serial communications interface (SCI) with baud rate generator</li> <li>• Triple timer module</li> <li>• Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled</li> </ul>																														
<b>Internal Memories</b>	<ul style="list-style-type: none"> <li>• <math>192 \times 24</math>-bit bootstrap ROM</li> <li>• <math>8 \text{ K} \times 24</math>-bit RAM total</li> <li>• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:</li> </ul> <table border="1"> <thead> <tr> <th>Program RAM Size</th> <th>Instruction Cache Size</th> <th>X Data RAM Size</th> <th>Y Data RAM Size</th> <th>Instruction Cache</th> <th>Switch Mode</th> </tr> </thead> <tbody> <tr> <td><math>20480 \times 24</math> bits</td> <td>0</td> <td><math>7168 \times 24</math> bits</td> <td><math>7168 \times 24</math> bits</td> <td>disabled</td> <td>disabled</td> </tr> <tr> <td><math>19456 \times 24</math> bits</td> <td><math>1024 \times 24</math>-bit</td> <td><math>7168 \times 24</math> bits</td> <td><math>7168 \times 24</math> bits</td> <td>enabled</td> <td>disabled</td> </tr> <tr> <td><math>24576 \times 24</math> bits</td> <td>0</td> <td><math>5120 \times 24</math> bits</td> <td><math>5120 \times 24</math> bits</td> <td>disabled</td> <td>enabled</td> </tr> <tr> <td><math>23552 \times 24</math> bits</td> <td><math>1024 \times 24</math>-bit</td> <td><math>5120 \times 24</math> bits</td> <td><math>5120 \times 24</math> bits</td> <td>enabled</td> <td>enabled</td> </tr> </tbody> </table>	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode	$20480 \times 24$ bits	0	$7168 \times 24$ bits	$7168 \times 24$ bits	disabled	disabled	$19456 \times 24$ bits	$1024 \times 24$ -bit	$7168 \times 24$ bits	$7168 \times 24$ bits	enabled	disabled	$24576 \times 24$ bits	0	$5120 \times 24$ bits	$5120 \times 24$ bits	disabled	enabled	$23552 \times 24$ bits	$1024 \times 24$ -bit	$5120 \times 24$ bits	$5120 \times 24$ bits	enabled	enabled
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<b>External Memory Expansion</b>	<ul style="list-style-type: none"> <li>• Data memory expansion to two <math>256 \text{ K} \times 24</math>-bit word memory spaces using the standard external address lines</li> <li>• Program memory expansion to one <math>256 \text{ K} \times 24</math>-bit words memory space using the standard external address lines</li> <li>• External memory expansion port</li> <li>• Chip select logic for glueless interface to static random access memory (SRAMs)</li> <li>• Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)</li> </ul>																														
<b>Power Dissipation</b>	<ul style="list-style-type: none"> <li>• Very low-power CMOS design</li> <li>• Wait and Stop low-power standby modes</li> <li>• Fully static design specified to operate down to 0 Hz (dc)</li> <li>• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)</li> </ul>																														
<b>Packaging</b>	<ul style="list-style-type: none"> <li>• 144-pin TQFP package in lead-free or lead-bearing versions</li> <li>• 196-pin molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions</li> </ul>																														

# Target Applications

The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.

## Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56309 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

**Table 2.** DSP56309 Documentation

Name	Description	Order Number
<i>DSP56309 Technical Data</i>	Description, features list, and specifications of the DSP56309	DSP56309
<i>DSP56309 User's Manual</i>	Detailed functional description of the DSP56309 memory configuration, operation, and register programming	DSP56309UM
<i>DSP56300 Family Manual</i>	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56309 product website

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