ISL28133EVAL1Z High-Gain Evaluation Board User's Guide

Introduction

The maximum useful signal range of a high gain DC amplifier is limited by the amplifiers own DC offset and low frequency noise. For battery powered amplifiers the problem is further compounded due to limits of low battery voltage. For example, the useful input voltage range of an ideal amplifier with 10kV/V gain operating from a 3V Lithium cell would be 300µV, which would drive the to the maximum possible +3V output. A standard low offset amplifier with 100µV VOS would reduce the maximum useful input voltage range from 300µV to 200µV, since the input offset voltage alone would drive the amplifier output to 10k times that, taking up 1V of the 3V total available voltage range. Further reductions due to offset voltage drift, low frequency 1/f noise, and the inability to swing the output close to the power supply rails can limit the best amplifiers to DC gains no higher than several hundred V/V.

The ISL28133 chopper stabilized rail-to-rail op amp features a low 8µV maximum VOS over-temperature and a 0.1Hz 1/f noise corner frequency enabling very high gain single-stage DC amplifiers that can operate from single cell batteries while consuming only 20µA of current. The ISL28133EVAL1Z evaluation board is configured as a precision high-gain (G = 10,000) differential amplifier and demonstrates the level of performance possible with this type of amplifier while operating from battery voltages as low as 2.4V.

Reference Documents

- ISL28133 Data Sheet, FN6560

Evaluation Board Key Features

The ISL28133EVAL1Z is designed to enable the IC to operate from a single supply, +2.4VDC to +5.5VDC or from split supplies, ±1.2VDC to ±2.75V. The board is configured for a single op amp connected for single-ended or differential input with a closed loop gain of 10,000. A single external reference voltage (VREF) pin and provisions for a user-selectable voltage divider-filter are included.

Power Supplies (Figure 2)

External power connections are made through the V+, V-, VREF, and Ground connections on the evaluation board. For single supply operation, the -V and Ground pins are tied together to the power supply negative terminal. For split supplies, +V and -V terminals connect to their respective supply terminals. De-coupling capacitors C2 and C4 provide low-frequency power-supply filtering, while four additional capacitors, C1, C5, C7 and C8, which are connected close to the part, filter out high frequency noise. Anti-reverse diodes D1 and D2 (optional) protect the circuit in the case of accidental polarity reversal.

The circuit can operate from a single supply or from dual supplies. The VREF pin can be connected to ground to establish a ground referenced input for split supply operation, or can be externally set to any reference level for single supply operation.

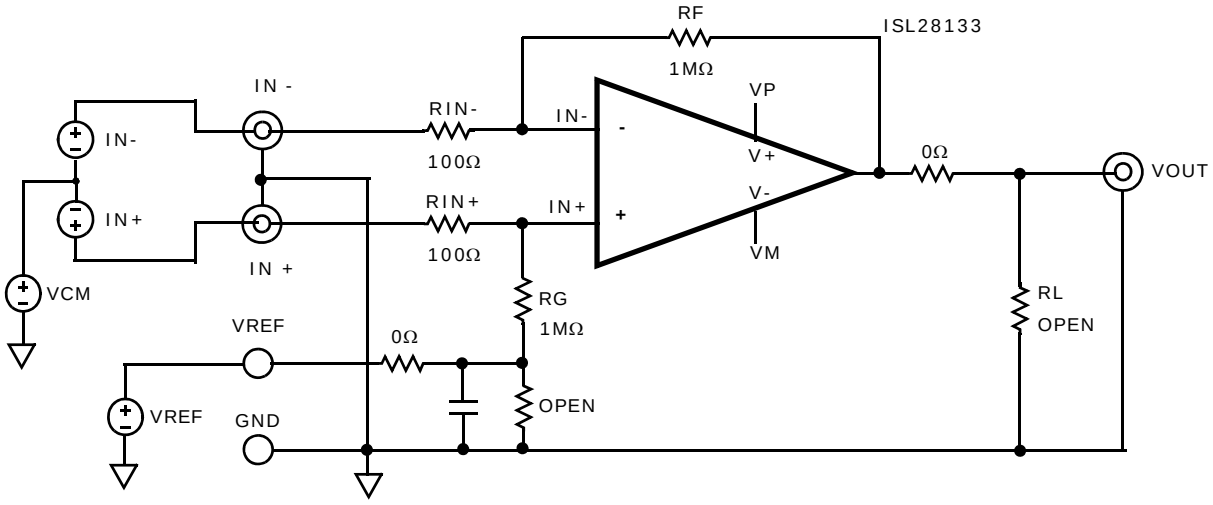


FIGURE 1. BASIC AMPLIFIER CONFIGURATION

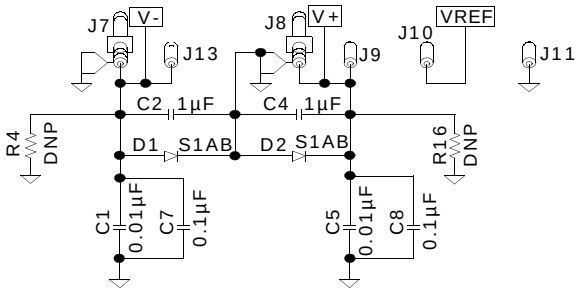


FIGURE 2. POWER SUPPLY CIRCUIT

Amplifier Configuration (Figure 2)

The schematic of the op amp with the components supplied is shown in Figure 2, with a closed loop gain of 10,000. The circuit implements a Hi-Z differential input with unbalanced common mode impedance. The differential amplifier gain is expressed in Equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \bullet (R_F / R_{IN}) + V_{REF} \quad \text{(EQ. 1)}$$

where: $R_F = R_G$ and $R_{IN+} = R_{IN-}$ and the differential input impedance is ~1M with V_{REF} at GND. The IN- input connects to the amplifier summing junction and it's impedance to ground is a low 100Ω. The impedance of the IN+ input to ground is much higher at 1.001MΩ to VREF.

For single-ended input inverting operation (G = -10001), the IN+ input is grounded and the signal is supplied to the IN- input. V_{REF} must be connected to a reference voltage between the V+ and V- supply rails. For non-inverting operation (G = 10,000), the IN- input is grounded and the signal is supplied to the IN+ input. The non-inverting gain is strongly dependent on any resistance from IN- to GND. For good gain accuracy, a 0Ω resistor should be installed on the empty R7 pads.

User-selectable Options (Figures 3 and 4)

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier inputs, the VREF input, outputs and the amplifier feedback loops.

A voltage divider and filter option (Figure 3) can be added to establish a power supply-tracking common mode reference at the VREF input. The inverting and non-inverting inputs have additional resistor placements for adding input attenuation, or to establish input DC offsets through the VREF pin.

The output (Figure 4) also has additional resistor and capacitor placements for filtering and loading.

NOTE: Operational amplifiers are sensitive to output capacitance and may oscillate. In the event of oscillation, reduce output capacitance by using shorter cables, or add a resistor in series with the output.

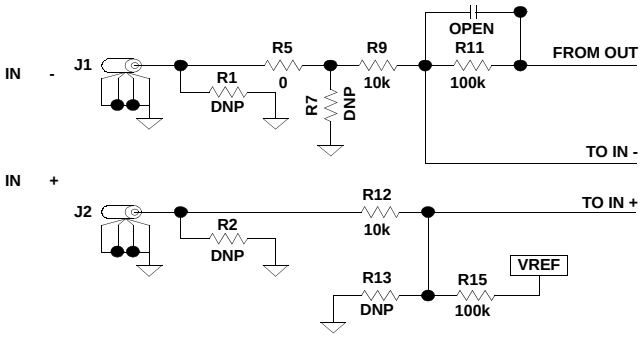


FIGURE 3. INPUT STAGE

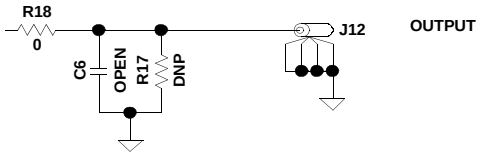
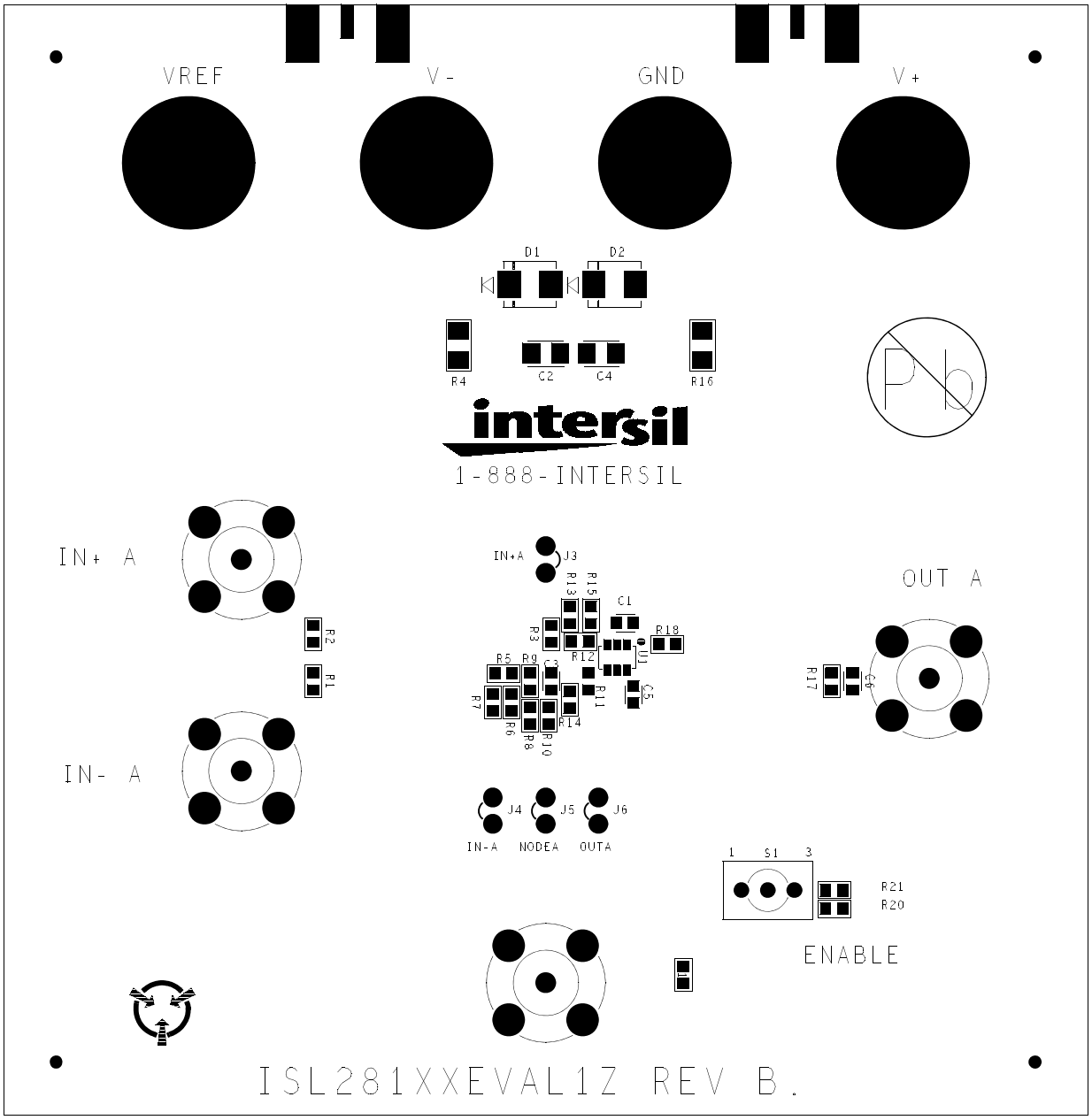


FIGURE 4. OUTPUT STAGE

TABLE 1. ISL28133EVAL1Z COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C2, C4	CAP, SMD, 0603, 1µF, 25V, 10%, X7R, ROHS	Power Supply Decoupling
C1, C5	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Power Supply Decoupling
C7, C8	CAP, SMD, 0603, 0.01µF, 25V, 10%, X7R , ROHS	Power Supply Decoupling
C3, C6	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	User selectable capacitors - not populated
D1, D2	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A, ROHS	Reverse Power Protection
U1 (ISL28133EVAL1Z)	ISL28133FHZ-T7, IC-RAIL-TO-RAIL OP AMP, SOT-23, ROHS	
R1-R4, R6-R8, R10, R13, R14, R16, R17, R19, R21	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	User selectable resistors - not populated
R5, R18	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	0Ω user selectable resistors
R9, R12	RES, SMD, 0603, 100, 1/10W, 1%, TF, ROHS	Gain resistors
R11, R15	RES, SMD, 0603, 1M, 1/10W, 1%, TF, ROHS	Gain resistors

ISL28133EVAL1Z Top View



ISL28133EVAL1Z Schematic Diagram