Unit: mm

TOSHIBA Diode Silicon Epitaxial Planar Diode

# **1SS397**

### High Voltage, High Speed Switching Applications

• Low forward voltage  $: V_F = 1.0V \text{ (typ.)}$ • High voltage  $: V_R = 400V \text{ (min.)}$ • Fast reverse recovery time:  $t_{rr} = 0.5\mu s \text{ (typ.)}$ • Small total capacitance  $: C_T = 2.5pF \text{ (typ.)}$ 

• Small package : SC-70

#### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	$V_{RM}$	420	V
Reverse voltage	V <sub>R</sub>	400	V
Maximum (peak) forward current	I <sub>FM</sub>	300	mA
Average forward current	Io	100	mA
Surge current (10ms)	I <sub>FSM</sub>	2	Α
Power dissipation	Р	100	mW
Junction temperature	Tj	125	°C
Storage temperature range	T <sub>stg</sub>	-55~125	°C

2.1±0.1 1.25±0.1 1.25±0.1 1.0000 1.0000 1.0

Weight: 0.006g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high

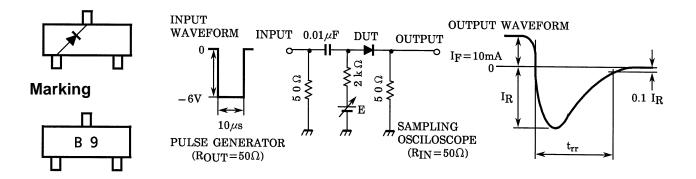
temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

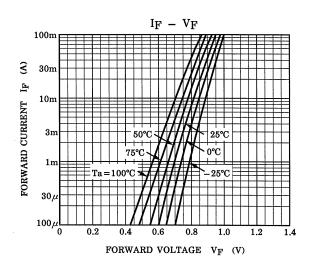
#### **Electrical Characteristics (Ta = 25°C)**

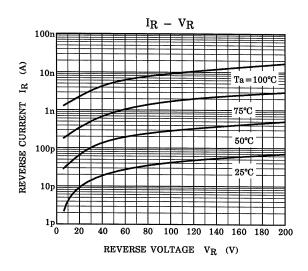
Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Forward voltage	V <sub>F (1)</sub>	_	I <sub>F</sub> = 10mA	_	0.8	_	V
	V <sub>F (2)</sub>	_	I <sub>F</sub> = 100mA	_	1.0	1.3	
Reverse current	I <sub>R (1)</sub>	_	V <sub>R</sub> = 300V	_	_	0.1	μΑ
	I <sub>R (2)</sub>	_	V <sub>R</sub> = 400V	_	-	1.0	
Total capacitance	C <sub>T</sub>	_	$V_R = 0$ , $f = 1MH_Z$	_	2.5	5.0	pF
Reverse recovery time	t <sub>rr</sub>	_	I <sub>F</sub> = 10mA (Fig.1)	_	0.5	_	μs

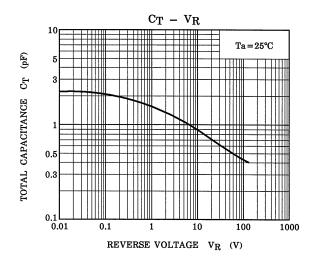
## Equivalent Circuit Fig.1 Reverse Recovery Time (trr) Test Circuit(Top View)

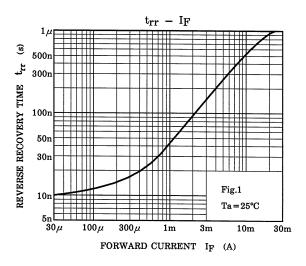


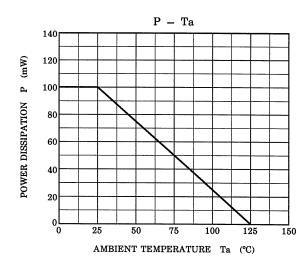
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