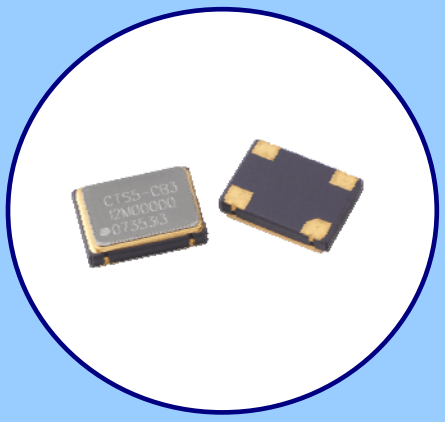
Model CB3 & CB3LV

HCMOS/TTL Clock Oscillator

FEATURES

- Standard 7.0mm x 5.0mm 4-Pad Surface Mount Package
- HCMOS/TTL Compatible Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 1 – 200 MHz
- Frequency Stability ±50 ppm Standard, ±25 ppm and ±20 ppm Available
- Operating Voltages +5.0Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- RoHS/Green Compliant (6/6)



APPLICATIONS

Applications for Model CB3 and CB3LV include digital video, networking equipment, wireless communications, broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, storage area networks, fiber channel, computers and peripherals, test and measurement, SONET/SDH/DWDM, base stations and Pico cells.

ORDERING INFORMATION

CB3 □ - □□ - □□□ M □□□□□□

SUPPLY VOLTAGE

LV = +3.3Vdc
Blank = +5.0Vdc

FREQUENCY IN MHz

M - indicates MHz and decimal point. [3]

FREQUENCY STABILITY

6 = ± 20 ppm [1]
5 = ± 25 ppm
3 = ± 50 ppm [std]
7 = ± 32 ppm [2]
2 = ± 100 ppm [2]

OPERATING TEMPERATURE RANGE

C = -20°C to +70°C [standard]
I = -40°C to +85°C [1]

1] 6I Stability/Temperature combination is not available.

2] These stabilities are not recommended for new designs.

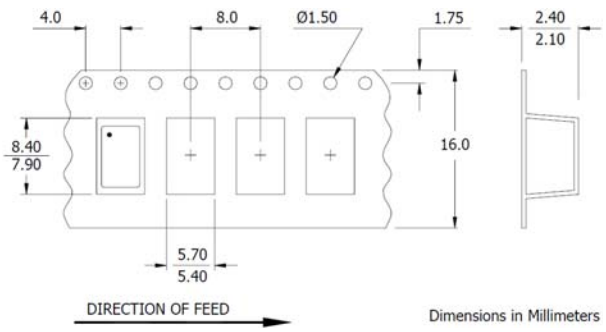
3] Frequency is recorded with only leading significant digits before the 'M' and 4 - 6 significant digits after the 'M' (including zeros).
[Ex. 3.579545 MHz, code as 3M579545; 14.31818 MHz, code as 14M31818; 125 MHz, code as 125M0000]

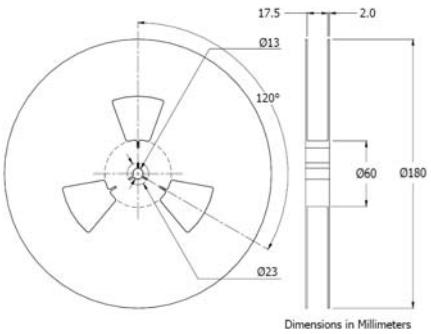
4] CTS Distributors may add a -T or -1 at the end of the part number to indicate Tape and Reel packaging.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]

Device quantity is 1,000 pieces maximum per reel.





ELECTRICAL CHARACTERISTICS

ELECTRICAL PARAMETERS

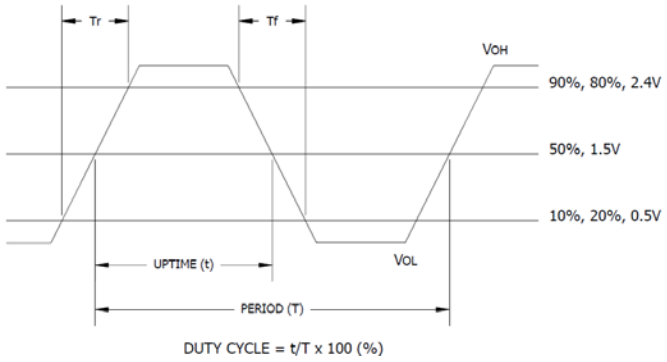
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	+7.0	V
Storage Temperature	T_{STG}	-	-40	-	+100	°C
Frequency Range						
CB3	f_O	-	1.5	-	107	MHz
CB3LV		-	1.5	-	200	
Frequency Stability	$\Delta f/f_O$	See Note 1 and Ordering Information	-	-	20,25,50 or 100	± ppm
Aging	Δf	First year	-	3	5	± ppm
Operating Temperature						
Commercial	T_A	-	-20	25	+70	°C
Industrial			-40		+85	
Supply Voltage						
CB3	V_{CC}	±10%	4.5	5.0	5.5	V
CB3LV			3.0	3.3	3.6	
Supply Current		Frequency Range				
		Tested load condition noted for typical values.				
CB3	I_{CC}	1.5MHz to 20MHz C_L=50pF	-	10	25	mA
		20.001MHz to 80MHz C_L=50pF	-	30	50	
		80.001MHz to 107MHz C_L=15pF	-	40	80	
CB3LV		1.5MHz to 20MHz C_L=15pF	-	7	12	
		20.001MHz to 80MHz C_L=15pF	-	20	40	
		80.001MHz to 200MHz C_L=15pF	-	30	60	
Output Load	C_L	1.5MHz to 50MHz	-	-	50	pF
		50.001MHz to 80MHz	-	-	30	
		80.001MHz to 200MHz	-	-	15	
Output Voltage Levels						
Logic '1' Level	V_{OH}	CMOS Load	90%V_{CC}	-	-	V
		10 TTL LOAD	V_{CC}-0.6V			
Logic '0' Level	V_{OL}	CMOS	-	-	10%V_{CC}	
		TTL Load			0.4	
Output Current						
Logic '1' Level	I_{OH}	V_{OH} = 3.9V/2.2V V_{CC} = 4.5V/3.0V	-	-	-16/-8	mA
Logic '0' Level	I_{OL}	V_{OL} = 0.4V V_{CC} = 4.5V/3.0V	-	-	+16/+8	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time		@ 10% - 90% Levels				
		Tested load condition noted for typical values.				
CB3	T_R, T_F	1.5MHz to 20MHz C_L=50pF	-	8	10	ns
		20.001MHz to 80MHz C_L=50pF	-	5	8	
		80.001MHz to 200MHz C_L=15pF	-	2.5	5	
CB3LV		1.5MHz to 20MHz C_L=15pF	-	6	8	
		20.001MHz to 80MHz C_L=15pF	-	3	5	
		80.001MHz to 200MHz C_L=15pF	-	1.5	3	
Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
Enable Function						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	2.0	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.8	
Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	200	ns
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	10	µA
Period Jitter, Pk-Pk	-	-	-	-	50	ps
Period Jitter, RMS	-	-	-	-	5	
Phase Jitter, RMS	-	Bandwidth 12kHz - 20MHz	-	-	1	

Notes:

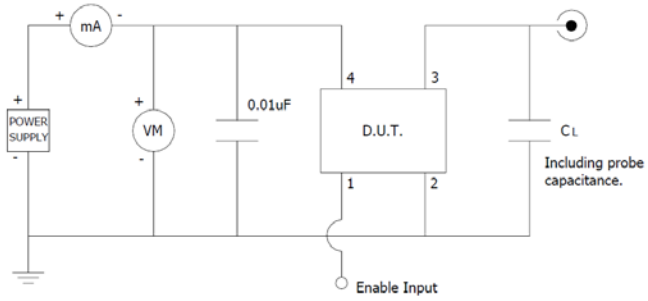
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

ELECTRICAL CHARACTERISTICS

LVCMOS OUTPUT WAVEFORM



TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

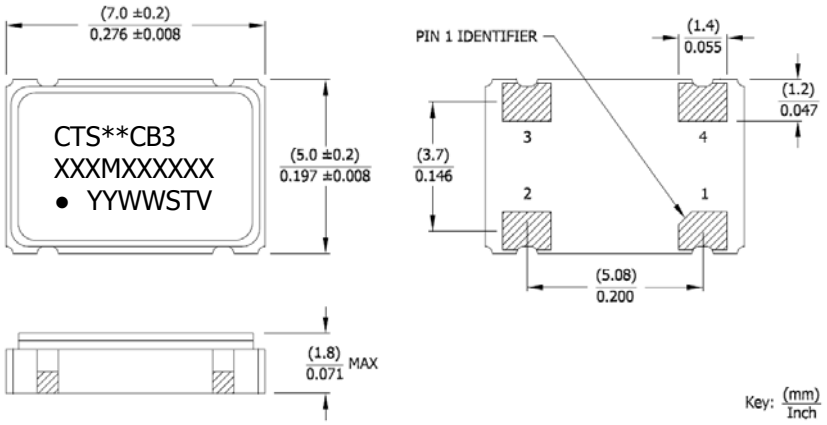
PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V_{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. ** – Manufacturing Site Code.
   [Note a dash may follow the site code and is acceptable.]
2. XXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 – 6 digits after the 'M' (including zeros).
   Ex. XMXXXXXX [3M579545]
   XXMXXXXX [14M31818]
   XXXMXXXX [125M0000]
3. YYWW – Date code, YY – year, WW – week.
4. ST – Frequency stability/temperature code.
   [Refer to Ordering Information.]
5. V – Voltage code. 3 = 3.3V, 5 = 5.0V.

NOTES

1. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020, 260°C maximum.
3. Moisture Sensitivity Level 1 per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.