

NTD110N02R, STD110N02R

Power MOSFET

24 V, 110 A, N-Channel DPAK



ON Semiconductor®

<http://onsemi.com>

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- AEC Q101 Qualified – STD110N02R
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

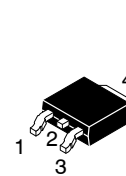
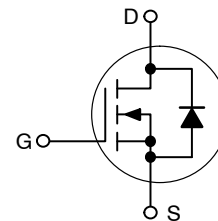
| Rating | Symbol | Value | Unit |
|---|-----------------|------------|--------------------|
| Drain-to-Source Voltage | V_{DSS} | 24 | V |
| Gate-to-Source Voltage – Continuous | V_{GS} | ± 20 | V |
| Thermal Resistance – Junction-to-Case | $R_{\theta JC}$ | 1.35 | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ | P_D | 110 | W |
| Drain Current | I_D | 110 | A |
| – Continuous @ $T_C = 25^\circ\text{C}$, Chip | I_D | 110 | A |
| – Continuous @ $T_C = 25^\circ\text{C}$ | I_D | 110 | A |
| Limited by Package | I_D | 32 | A |
| – Continuous @ $T_A = 25^\circ\text{C}$ | I_D | 32 | A |
| Limited by Wires | I_D | 110 | A |
| – Single Pulse ($t_p = 10 \mu\text{s}$) | I_D | 110 | A |
| Thermal Resistance | $R_{\theta JA}$ | 52 | $^\circ\text{C/W}$ |
| – Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 52 | $^\circ\text{C/W}$ |
| – Total Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 2.88 | W |
| – Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ | I_D | 17.5 | A |
| Thermal Resistance | $R_{\theta JA}$ | 100 | $^\circ\text{C/W}$ |
| – Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 100 | $^\circ\text{C/W}$ |
| – Total Power Dissipation @ $T_A = 25^\circ\text{C}$ | P_D | 1.5 | W |
| – Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ | I_D | 12.5 | A |
| Operating and Storage Temperature Range | T_J, T_{stg} | -55 to 175 | $^\circ\text{C}$ |
| Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_L = 15.5 \text{ Apk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$) | E_{AS} | 120 | mJ |
| Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

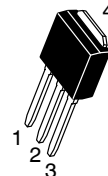
1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | I_D MAX |
|---------------|-----------------------|-----------|
| 24 V | 4.1 m Ω @ 10 V | 110 A |

N-Channel

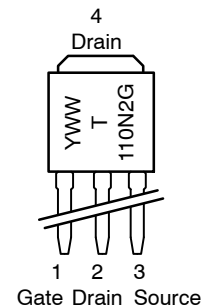
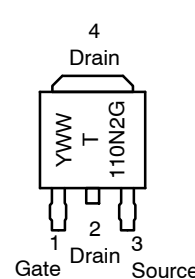


CASE 369AA
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



- Y = Year
- WW = Work Week
- T110N2 = Device Code
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD110N02R, STD110N02R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|---|----------------------|----|----|-----------|-------|
| Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 V, I _D = 250 μA) | V _{(BR)DSS} | 24 | 28 | | V |
| Positive Temperature Coefficient | | | 15 | | mV/°C |
| Zero Gate Voltage Drain Current (V _{DS} = 20 V, V _{GS} = 0 V) (V _{DS} = 20 V, V _{GS} = 0 V, T _J = 125°C) | I _{DSS} | | | 1.5 10 | μA |
| Gate-Body Leakage Current (V _{GS} = ±20 V, V _{DS} = 0 V) | I _{GSS} | | | ±100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | |
|--|---------------------|-----|--------------------------|------------|------------|
| Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μA) | V _{GS(th)} | 1.0 | 1.5 5.0 | 2.0 | V mV/°C |
| Negative Threshold Temperature Coefficient | | | | | |
| Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 V, I _D = 110 A) (V _{GS} = 4.5 V, I _D = 55 A) (V _{GS} = 10 V, I _D = 20 A) (V _{GS} = 4.5 V, I _D = 20 A) | R _{DS(on)} | | 4.1 5.5 3.9 5.5 | 4.6 6.2 | mΩ |
| Forward Transconductance (V _{DS} = 10 V, I _D = 15 A) (Note 3) | g _{FS} | | 44 | | Mhos |

DYNAMIC CHARACTERISTICS

| | | | | | |
|----------------------|--|------------------|--|--------------|----|
| Input Capacitance | (V _{DS} = 20 V, V _{GS} = 0 V, f = 1.0 MHz) | C _{iss} | | 2710 3440 | pF |
| Output Capacitance | | C _{oss} | | 1105 1670 | |
| Transfer Capacitance | | C _{rss} | | 450 640 | |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | |
|---------------------|--|---------------------|--|------------|----|
| Turn-On Delay Time | (V _{GS} = 10 V, V _{DD} = 10 V, I _D = 40 A, R _G = 3.0 Ω) | t _{d(on)} | | 11 22 | ns |
| Rise Time | | t _r | | 39 80 | |
| Turn-Off Delay Time | | t _{d(off)} | | 27 40 | |
| Fall Time | | t _f | | 21 40 | |
| Gate Charge | (V _{GS} = 4.5 V, I _D = 40 A, V _{DS} = 10 V) (Note 3) | Q _T | | 23.6 28 | nC |
| | | Q _{GS} | | 5.1 | |
| | | Q _{GD} | | 11 | |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|--------------------------------|---|-----------------|--|----------------------|-----|----|
| Forward On-Voltage | (I _S = 20 A, V _{GS} = 0 V) (Note 3) (I _S = 55 A, V _{GS} = 0 V) (I _S = 20 A, V _{GS} = 0 V, T _J = 125°C) | V _{SD} | | 0.82 0.99 0.65 | 1.2 | V |
| Reverse Recovery Time | (I _S = 30 A, V _{GS} = 0 V, dI _S /dt = 100 A/μs) (Note 3) | t _{rr} | | 36.5 | | ns |
| | | t _a | | 30 | | |
| | | t _b | | 25 | | |
| Reverse Recovery Stored Charge | | Q _{rr} | | 0.048 | | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD110N02R, STD110N02R

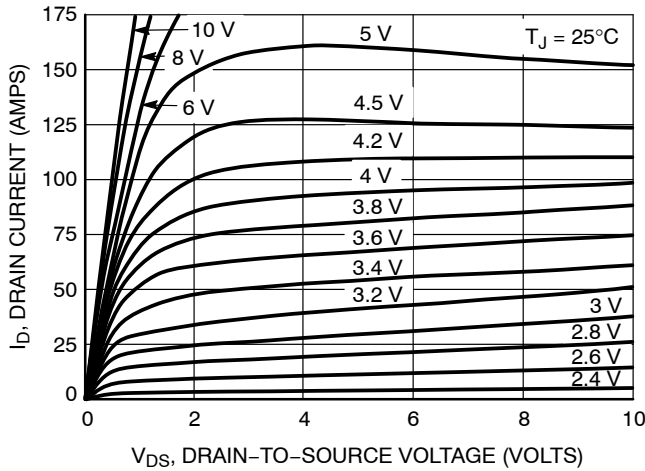


Figure 1. On-Region Characteristics

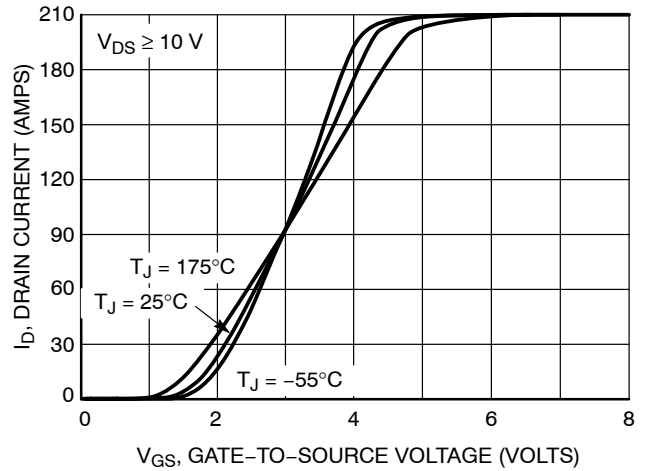


Figure 2. Transfer Characteristics

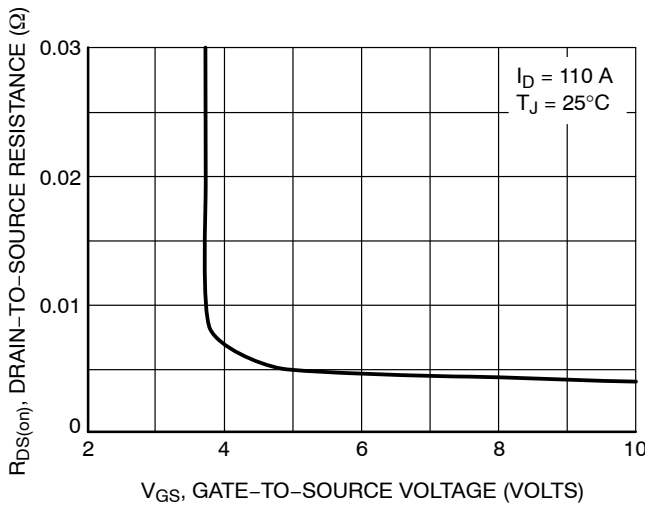


Figure 3. On-Resistance versus Gate-to-Source Voltage

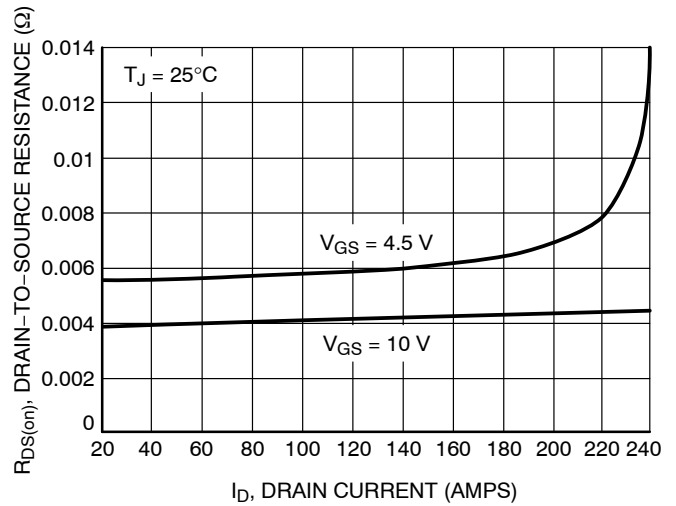


Figure 4. On-Resistance versus Drain Current and Gate Voltage

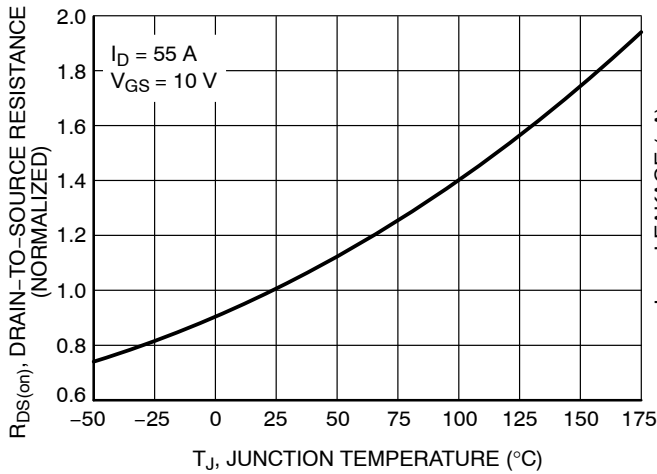


Figure 5. On-Resistance Variation with Temperature

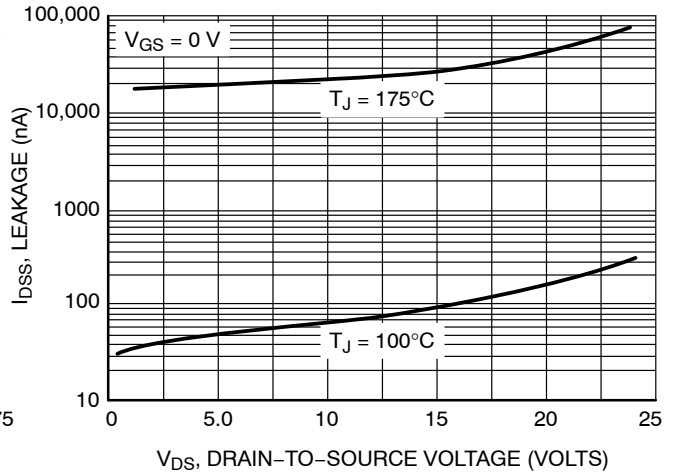


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD110N02R, STD110N02R

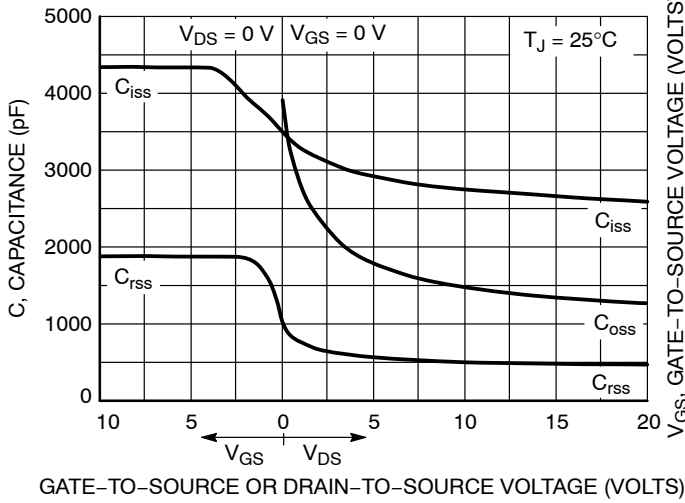


Figure 7. Capacitance Variation

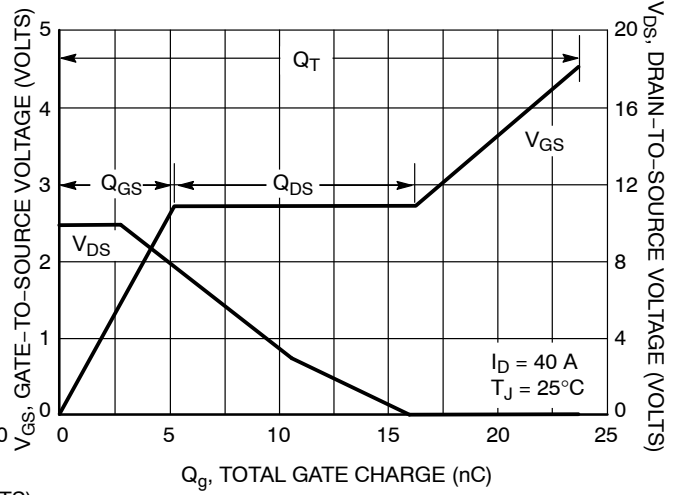


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

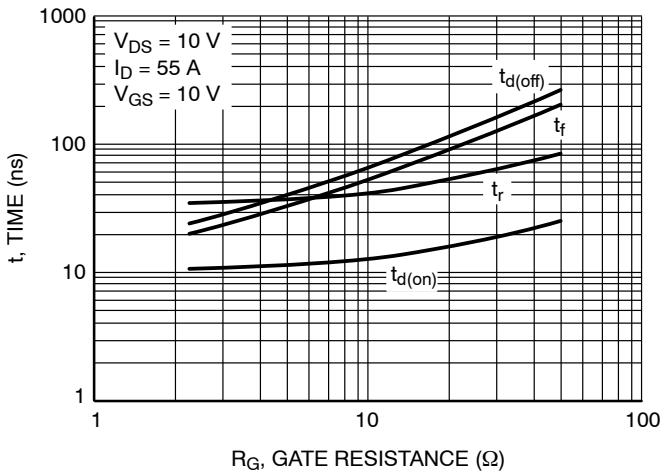


Figure 9. Resistive Switching Time Variation versus Gate Resistance

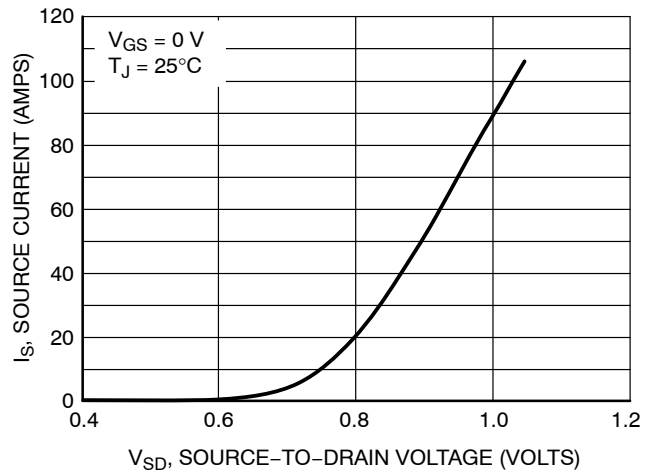


Figure 10. Diode Forward Voltage versus Current

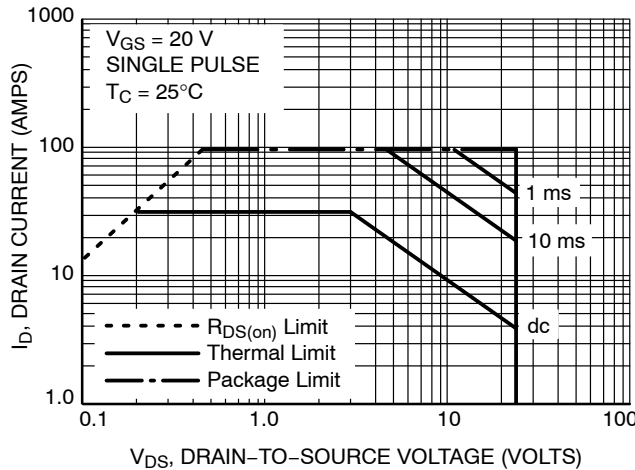


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD110N02R, STD110N02R

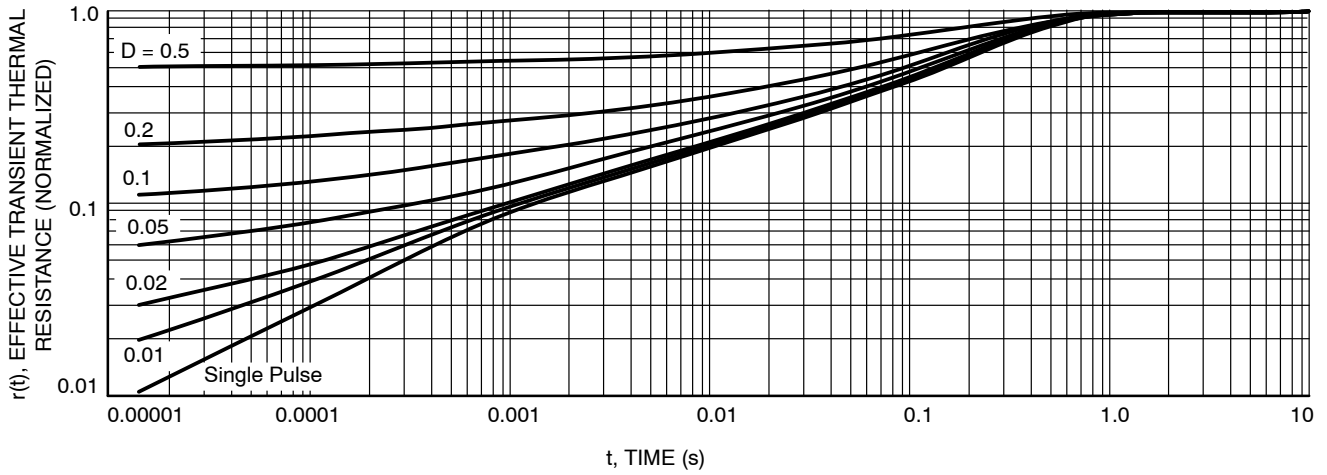


Figure 12. Thermal Response

ORDERING INFORMATION

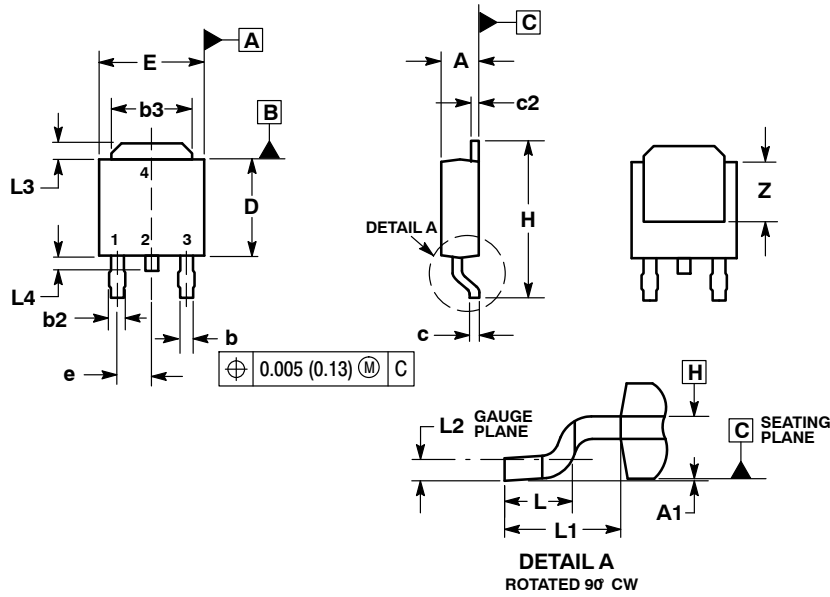
| Device | Package | Shipping [†] |
|---------------|-------------------|-----------------------|
| NTD110N02RT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| STD110N02RT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD110N02R, STD110N02R

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA-01 ISSUE B

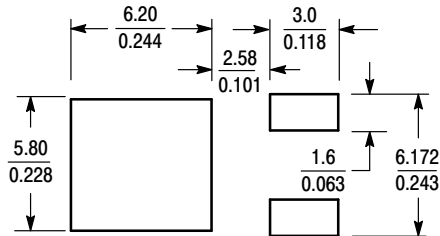


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

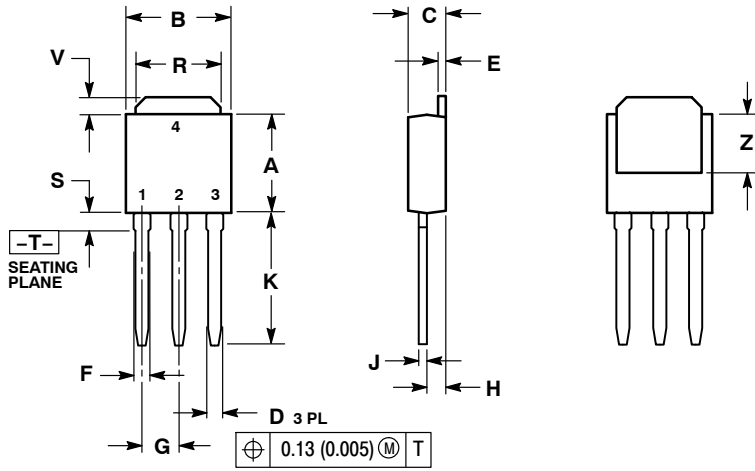
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD110N02R, STD110N02R

PACKAGE DIMENSIONS

IPAK
CASE 369D-01
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 | BSC | 2.29 | BSC |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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