2.1±0.1 1.7±0.1

> 0.16 +0.06/-0.05

> > 2-2T1D

Unit: mm

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSIV)

# SSM6J51TU

## **High Current Switching Applications**

Suitable for high-density mounting due to compact package

• Low on-resistance:  $R_{on} = 54 \text{ m}\Omega \text{ (max) } (@V_{GS} = -2.5 \text{ V})$   $85 \text{ m}\Omega \text{ (max) } (@V_{GS} = -1.8 \text{ V})$ 

 $150 \text{m} \Omega \text{ (max) } (@V_{GS} = -1.5 \text{ V})$ 

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V <sub>DS</sub>	-12	$(\vee)$
Gate-Source voltage		V <sub>GSS</sub>	±8	V
Drain current	DC	I <sub>D</sub>	-4	A
	Pulse	I <sub>DP</sub>	-8	∧
Drain power dissipation		P <sub>D</sub> (Note 1)	500	mW
Channel temperature		T <sub>ch</sub>	150	°C
Storage temperature range		T <sub>stg</sub>	-55~150	{⟨c

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e.

Weight: 7 mg (typ.)

JEDEC JEITA

**TOSHIBA** 

1,2,5,6 Drain

Gate Source

operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board.

(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm<sup>2</sup>)

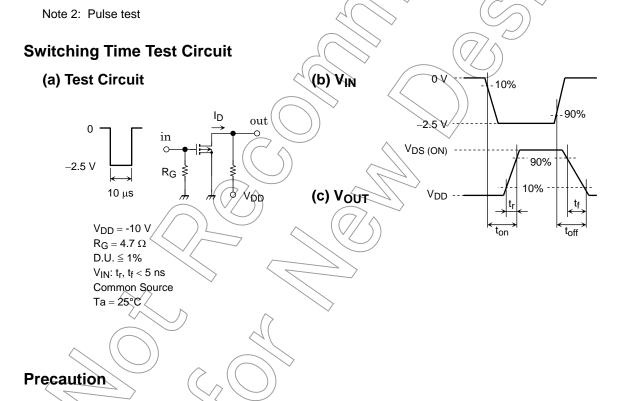
# Marking Equivalent Circuit (top view)

## **Handling Precaution**

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

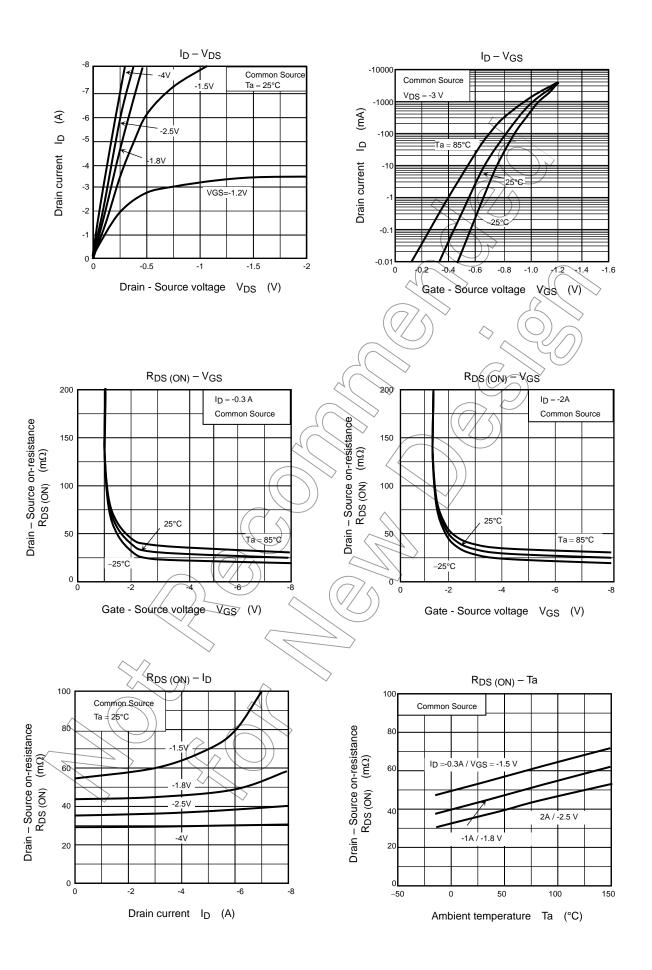
## **Electrical Characteristics (Ta = 25°C)**

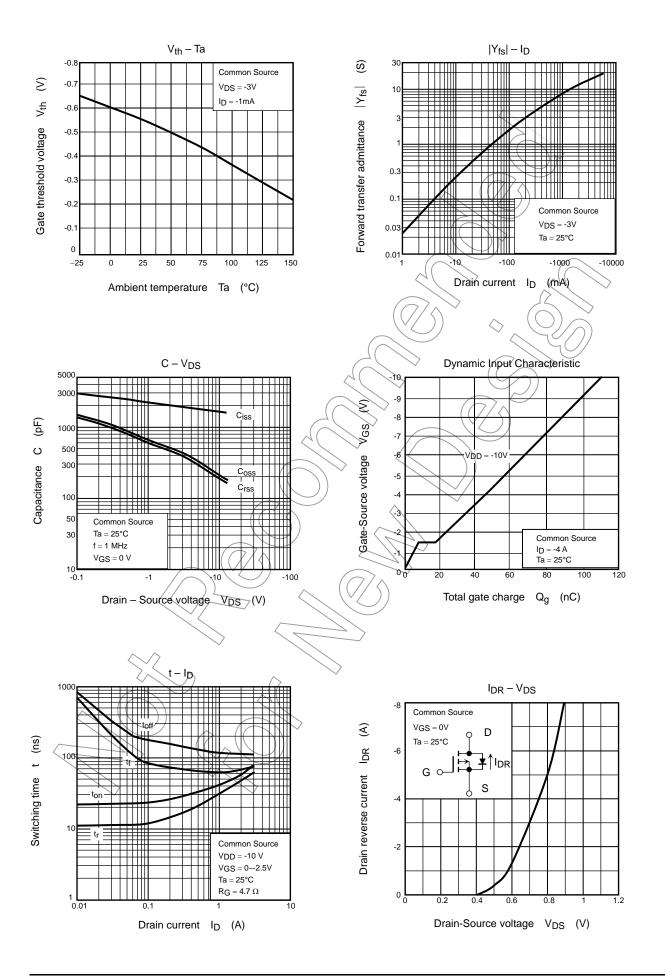
Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage current		I <sub>GSS</sub>	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$	_	-	±10	μА	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0$	-12	-	_	· V	
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-4	-	_		
Drain cut-off curre	ent	I <sub>DSS</sub>	$V_{DS} = -12 \text{ V}, V_{GS} = 0$		1	-10	μΑ	
Gate threshold vo	ltage	V <sub>th</sub>	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	) } ~	-1.0	V	
Forward transfer a	admittance	Y <sub>fs</sub>	$V_{DS} = -3 \text{ V}, I_D = -2.0 \text{ A}$ (Note 2)	6.0	12.0	=	S	
Drain-Source on-resistance		R <sub>DS</sub> (ON)	$I_D = -2.0 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 2)	<u>)</u>	38	54		
			$I_D = -1.0 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 2)	<u> </u>	48	85	mΩ	
			$I_D = -0.3 \text{ A}, V_{GS} = -1.5 \text{ V}$ (Note 2)	_	60	150		
Input capacitance		C <sub>iss</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f \neq 1 \text{ MHz}$	-	1700	-		
Reverse transfer of	capacitance	C <sub>rss</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	- /	(190	$\rightarrow$	pF	
Output capacitand	ce	C <sub>oss</sub>	V <sub>DS</sub> = −10 V, V <sub>GS</sub> ≠ 0, f = 1 MHz	-	210	> -	pF	
Switching time	Turn-on time	t <sub>on</sub>	$V_{DS} = -10 \text{ V}, I_{D} = -2.0 \text{ A},$	(	57	) -	- ns	
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0 \sim -2.5 \text{ V}, R_G = 4.7 \Omega$	1	120/	_		

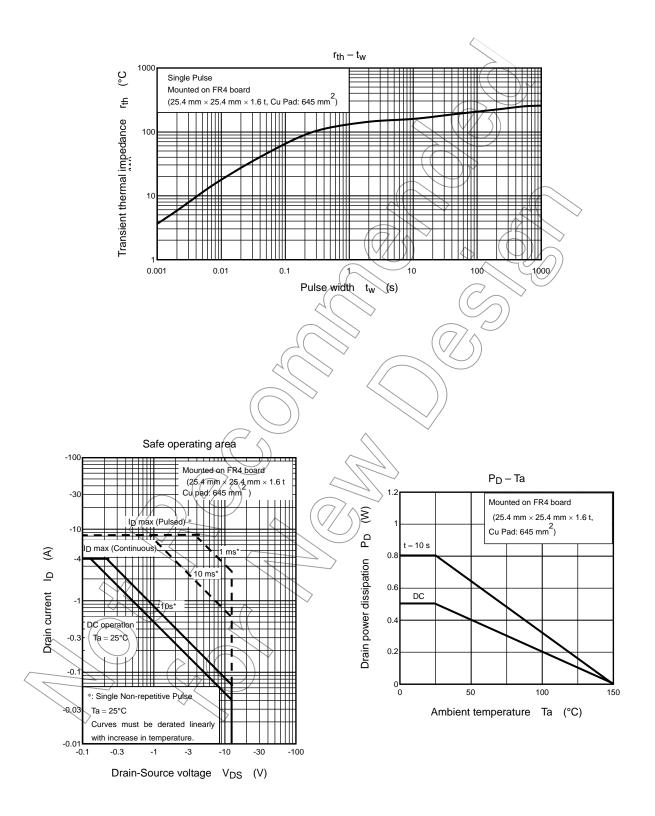


 $V_{th} \ can \ be \ expressed \ as \ the \ voltage \ between \ the \ gate \ and \ source \ when \ the \ low \ operating \ current \ value \ is \ ID = -1 mA \ for \ this \ product.$  For normal switching operation,  $V_{GS}$  (on) requires a higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS}$  (off)  $< V_{th}$   $< V_{GS}$  (on).) Be sure to take this into consideration when using the device.

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