TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π -MOSV)

TPC8012-H

Switching Regulator Applications DC/DC Converter Applications

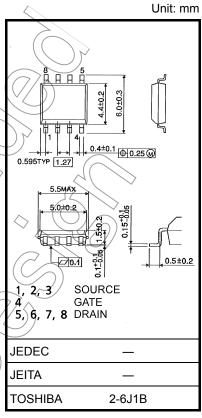
- Low drain-source ON-resistance: RDS (ON) = 0.28Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 1.35 S$ (typ.)
- Low leakage current: $I_{DSS} = 100 \mu A \text{ (max) (V}_{DS} = 200 \text{ V)}$
- Enhancement mode: $V_{th} = 3.0 \text{ to } 5.0 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA})$

Maximum Ratings (Ta = 25°C)

Characteristics			Symbol	Rating	Unit	
Drain-source voltage			V_{DSS}	200	\ \ \	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)			V_{DGR}	200	V	
Gate-source voltage			V_{GSS}	±30	V	
Drain current	DC (N	lote 1)	I _D	1.8	Α	
	Pulse (N	lote 1)	IDP	7.2		
Drain power dissipation (t = 10 s)			PD	1.9	$\langle \langle w \rangle$	
(Note 2a)			10	VI.3		
Drain power dissipation $(t = 10 s)$			PD	1.0	, W	
(Note 2b)				1.0	\backslash	
Single-pulse avalanche energy			FAC	2.05	(Cm)	
(Note 3) E _{AS} 2.05						
Avalanche current			JAR	1.8	→ A	
Repetitive avalanche	energy)	EAR	0.19	mJ	
(1	Note 2a) (N	(ote 4)	_/ LAR	0,10		
Channel temperature		$\langle \rangle$	Tch	150	°C	
Storage temperature range			T _{stg}	-55 to 150	°C	

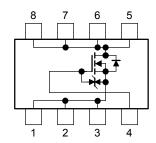
Note: For Notes 1 to 4, refer to the next page.

This transistor is an electrostatic-sensitive device. Handle with care.



Weight: 0.085 g (typ.)

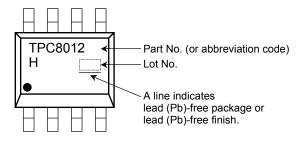
Circuit Configuration



Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient $(t=10 \; s) \eqno(Note \; 2a)$	R _{th (ch-a)}	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	R _{th (ch-a)}	125	°C/W

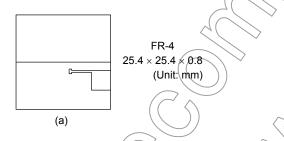
Marking (Note 5)

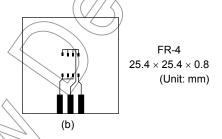


Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a)

(b) Device mounted on a glass-epoxy board (b)





Note 3: $V_{DD} = 50 \text{ V}$, $T_{Ch} = 25^{\circ}\text{C}$ (initial), L = 1.0 mH, $R_{C} = 25 \Omega$, $L_{AR} = 1.8 \text{ A}$

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: • on the lower left of the marking indicates Pin 1

* Weekly code: (Three digits)

Week of manufacture

(01 for first week of the year, continuing up to 52 or 53)

Year of manufacture

(The last digit of the calendar year)

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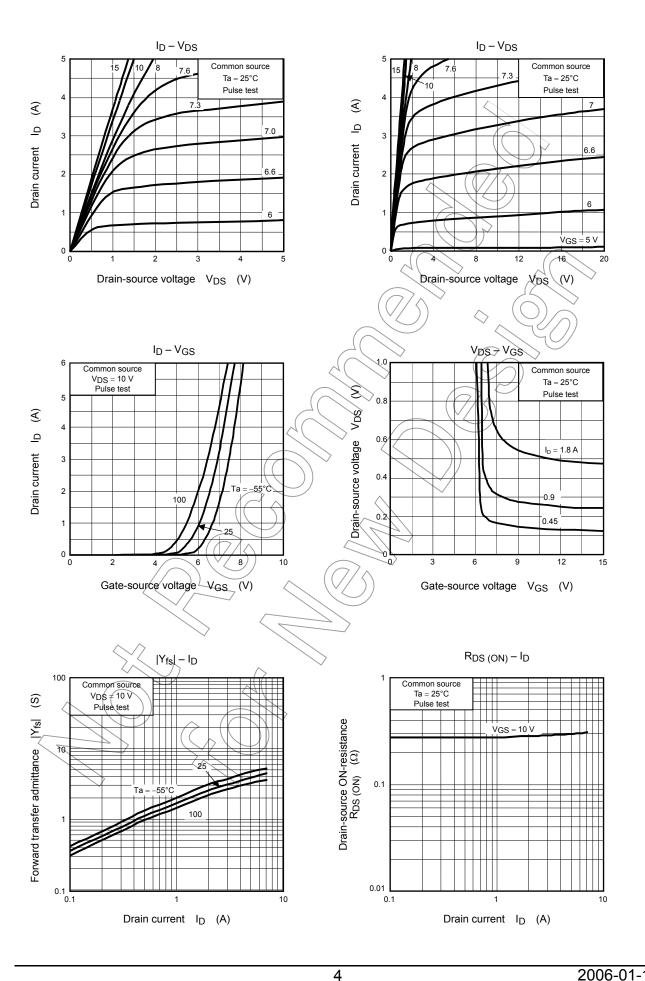
Electrical Characteristics (Ta = 25°C)

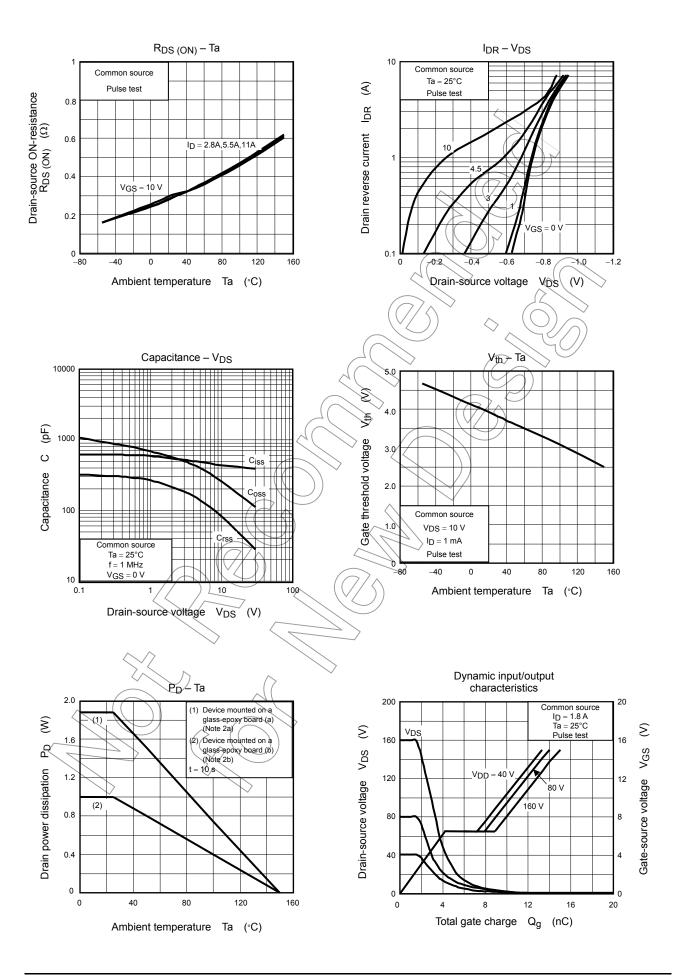
Ch	aracteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I _{GSS}	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μΑ
Drain cutoff curre	ent	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		_	100	μА
Drain-source bre	akdown voltage	V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	200	_		V
Gate threshold vo	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	3.0	_	5.0	V
Drain-source ON	-resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 0.9 A	(F	0.28	0.40	Ω
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 0.9 A	0,65	1.35	_	S
Input capacitance		C _{iss}))	440	_	
Reverse transfer capacitance		C _{rss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f \neq 1 \text{ MHz}$	_	80	_	pF
Output capacitance		Coss		_	260		
Switching time	Rise time	t _r	10 V □ □ □ = 0.9 Å	_	23	//	ns
	Turn-on time	t _{on}	V _{GS} 10 V		28	> —	
	Fall time	t _f	R = 111		22) _	113
	Turn-off time	t _{off}	V _{DD} ≃ 100 V Duty ≦ 1%, t _W ≥ 10 μs	(A)	73		
Total gate charge (gate-source plus		Qg	$V_{DD} \simeq 160 \text{ V}, V_{GS} = 10 \text{ V},$) –	11	_	_
Gate-source charge 1		Qgs	ID = 1.8 A	_	6	_	nC
Gate-drain ("Miller") charge		Qgd		_	5	_	

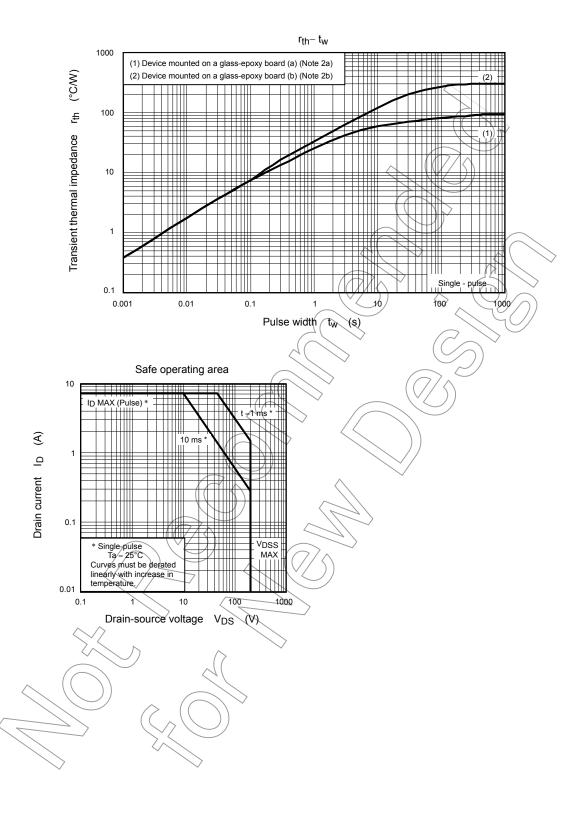
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Fest Condition	Min	Тур.	Max	Unit
Drain reverse current Pulse (Note 1)) I _{DRP}		_	_	7.2	Α
Forward voltage (diode)	V _{DSF}	$I_{DR} = 1.8 \text{Å}, V_{GS} = 0 \text{V}$	_	_	-1.5	V

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