

RJK0302DPB

Silicon N Channel Power MOS FET Power Switching

REJ03G1340-0600

Rev.6.00

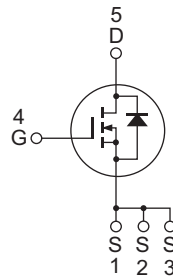
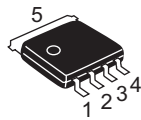
Apr 19, 2006

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 2.6 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	+16/-12	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP} ^{Note 2}	20	A
Avalanche energy	E_{AR} ^{Note 2}	40	mJ
Channel dissipation	P_{ch} ^{Note 3}	60	W
Channel to Case Thermal Resistance	θ_{ch-C}	2.09	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

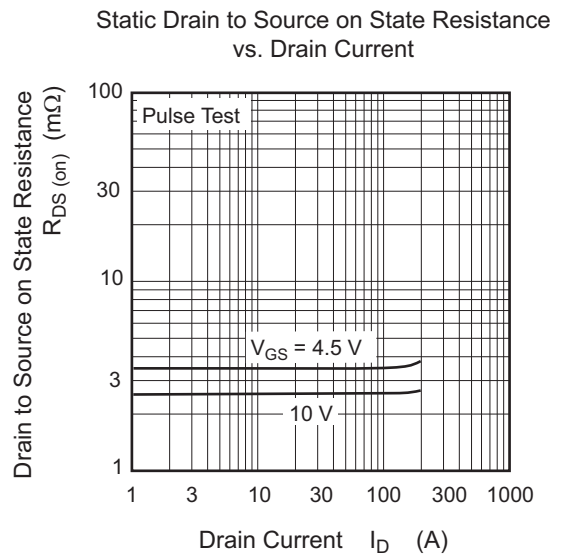
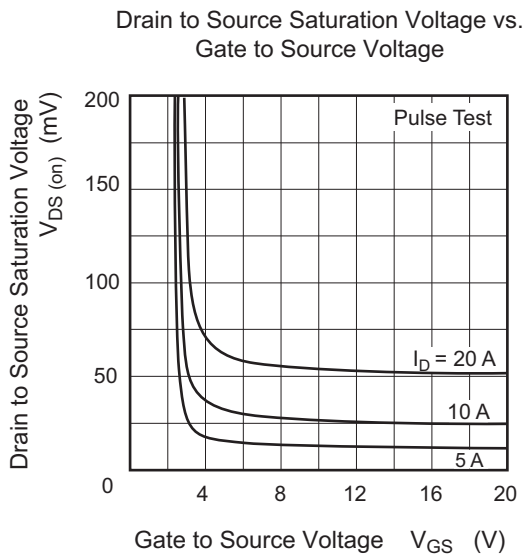
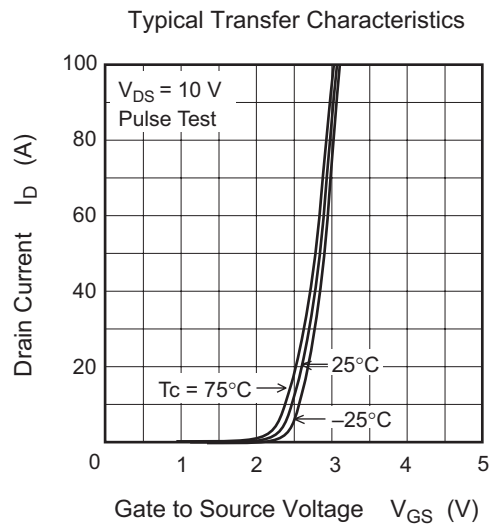
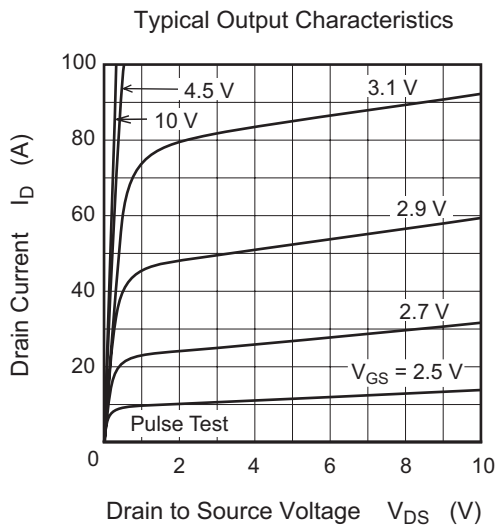
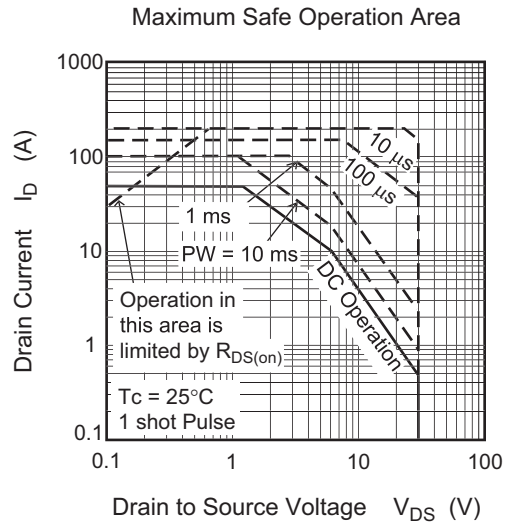
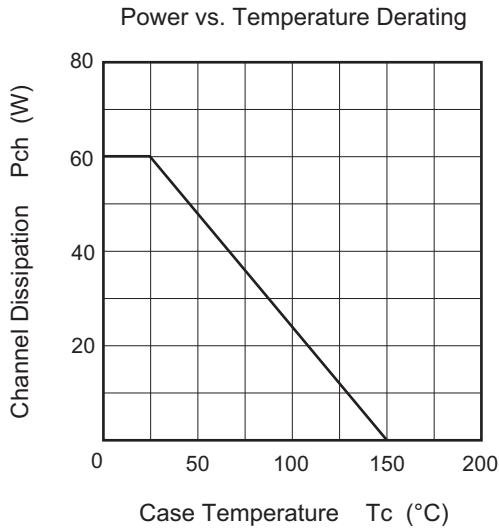
Electrical Characteristics

(Ta = 25°C)

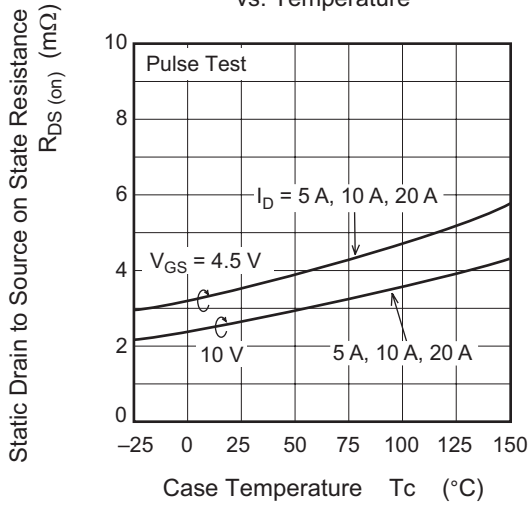
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = +16/-12 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.6	3.1	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	3.5	4.6	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	95	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4200	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	1380	—	pF	
Reverse transfer capacitance	C_{rss}	—	210	—	pF	
Gate Resistance	R_g	—	0.7	—	Ω	
Total gate charge	Q_g	—	28	—	nC	$V_{DD} = 10 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 50 \text{ A}$
Gate to source charge	Q_{gs}	—	12	—	nC	
Gate to drain charge	Q_{gd}	—	6.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$, $V_{DD} \cong 10 \text{ V}$, $R_L = 0.4 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	4.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	54	—	ns	
Fall time	t_f	—	5.5	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 50 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

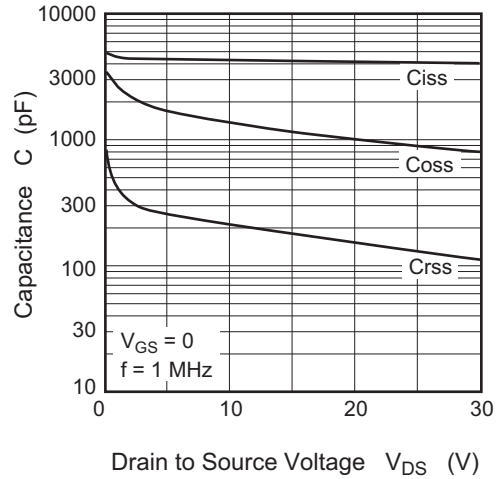
Main Characteristics



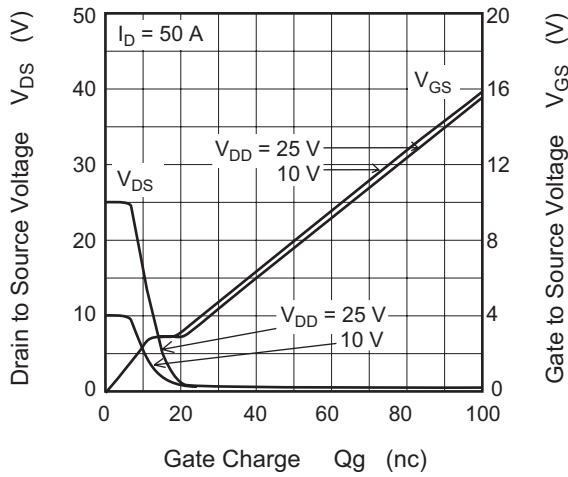
Static Drain to Source on State Resistance vs. Temperature



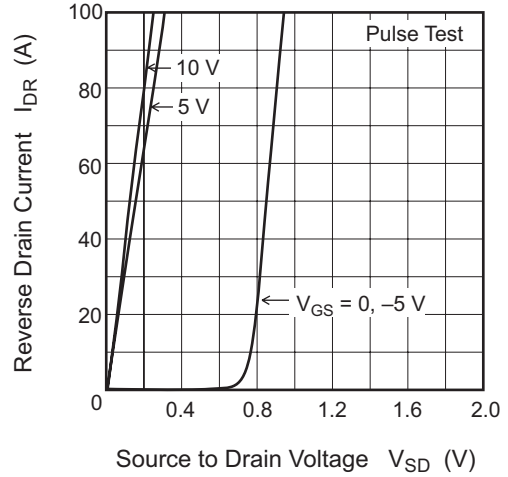
Typical Capacitance vs. Drain to Source Voltage



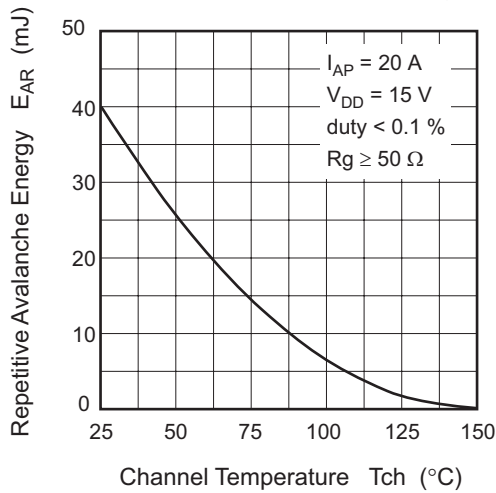
Dynamic Input Characteristics



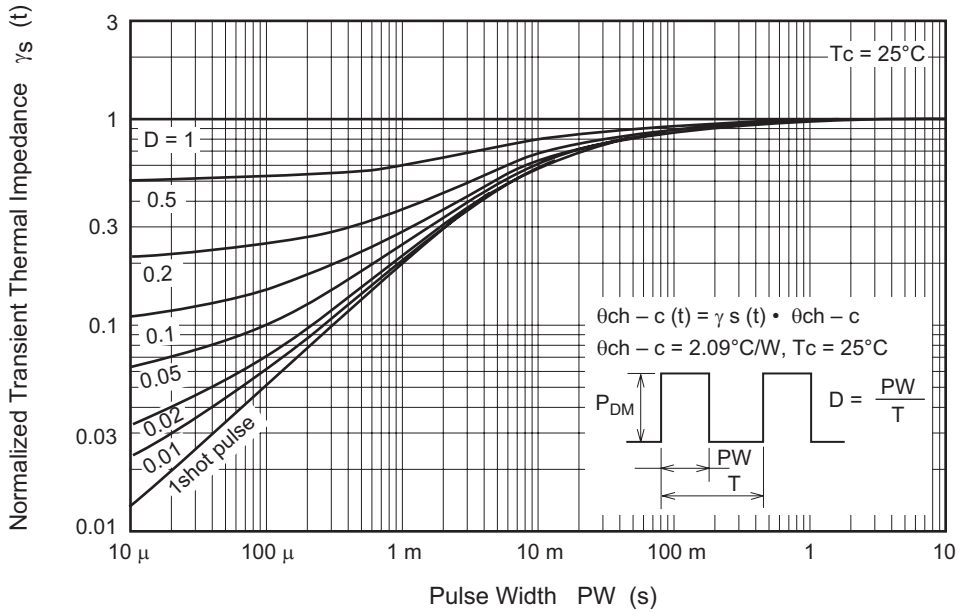
Reverse Drain Current vs. Source to Drain Voltage



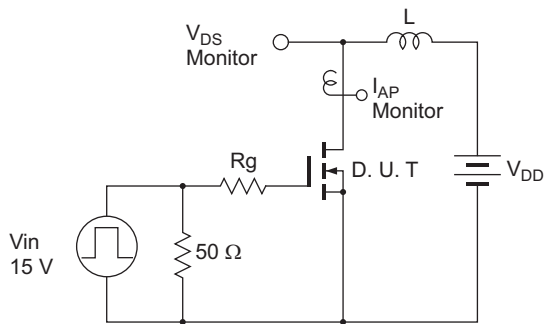
Maximum Avalanche Energy vs. Channel Temperature Derating



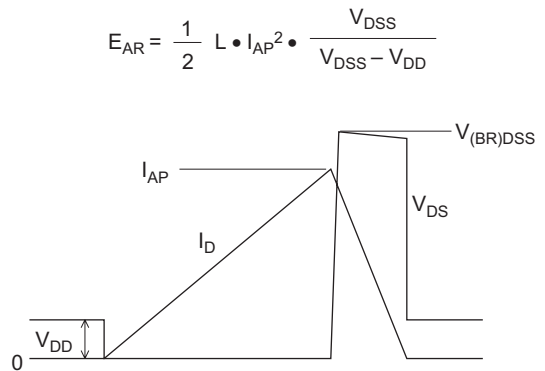
Normalized Transient Thermal Impedance vs. Pulse Width



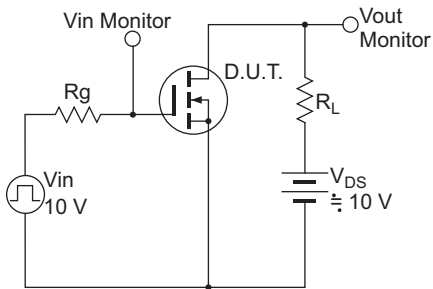
Avalanche Test Circuit



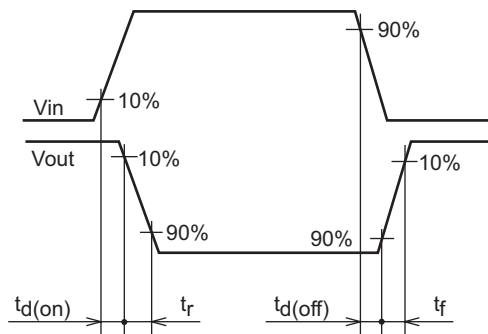
Avalanche Waveform



Switching Time Test Circuit



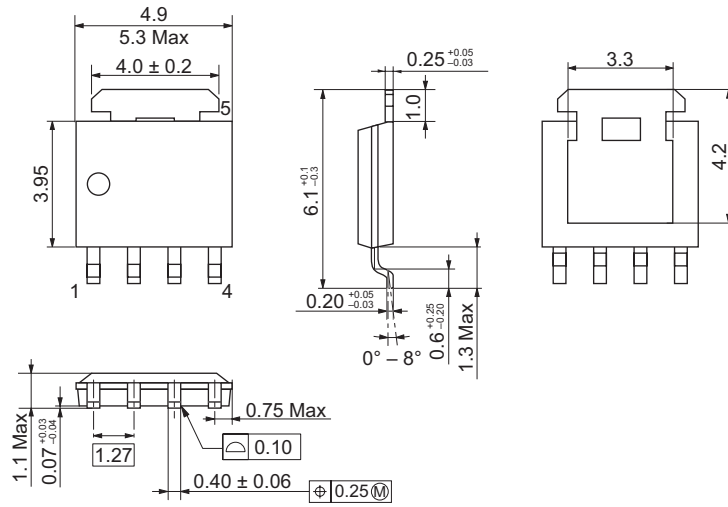
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LPAK	SC-100	PTZZ0005DA-A	LPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part Name	Quantity	Shipping Container
RJK0302DPB-00-J0	2500 pcs	Taping

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April 1st, 2010
Renesas Electronics Corporation

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