

# NTD40N03R

## Power MOSFET

45 A, 25 V, N-Channel DPAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- These are Pb-Free Devices

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	25	Vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	Vdc
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	50	W
Drain Current	$I_D$	45	A
– Continuous @ $T_C = 25^\circ\text{C}$ , Chip	$I_D$	32	A
– Continuous @ $T_A = 25^\circ\text{C}$ , Limited by Wires	$I_D$	100	A
– Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$		
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.1	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	9.2	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.5	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	7.8	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	$-55$ to $175$	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



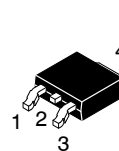
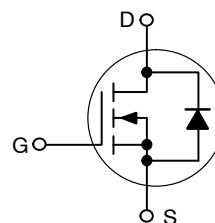
ON Semiconductor®

<http://onsemi.com>

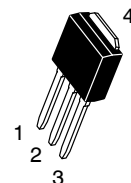
45 AMPERES, 25 VOLTS

$R_{DS(on)} = 12.6 \text{ m}\Omega$  (Typ)

### N-CHANNEL

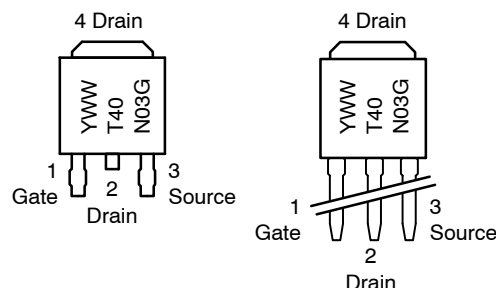


CASE 369AA  
DPAK  
(Surface Mount)  
STYLE 2



CASE 369D  
DPAK  
(Straight Lead)  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year  
WW = Work Week  
T40N03 = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD40N03R

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\text{ }\mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(br)DSS}$	25 –	28 –	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$	– –	– –	1.0 10	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	$\pm 100$	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ( $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{Adc}$ ) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.7 –	2.0 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 10\text{ Adc}$ ) ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 10\text{ Adc}$ )	$R_{DS(on)}$	– –	18.6 12.6	23 16.5	m $\Omega$
Forward Transconductance (Note 3) ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 10\text{ Adc}$ )	$g_{FS}$	–	20	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ )	$C_{iss}$	–	584	–	pF
Output Capacitance		$C_{oss}$	–	254	–	
Transfer Capacitance		$C_{rss}$	–	99	–	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ Vdc}$ , $V_{DD} = 10\text{ Vdc}$ , $I_D = 10\text{ Adc}$ , $R_G = 3\text{ }\Omega$ )	$t_{d(on)}$	–	4.5	–	ns
Rise Time		$t_r$	–	19.5	–	
Turn-Off Delay Time		$t_{d(off)}$	–	16.7	–	
Fall Time		$t_f$	–	3.5	–	
Gate Charge	$(V_{GS} = 4.5\text{ Vdc}$ , $I_D = 10\text{ Adc}$ , $V_{DS} = 10\text{ Vdc}$ ) (Note 3)	$Q_T$	–	5.78	–	nC
		$Q_1$	–	2.1	–	
		$Q_2$	–	2.5	–	

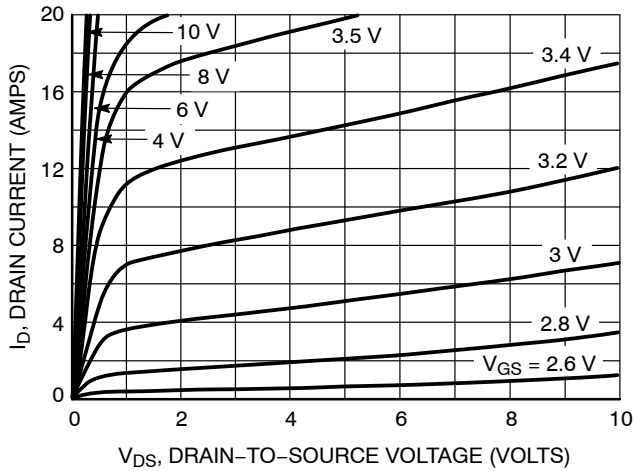
### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 10\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ ) (Note 3) $(I_S = 10\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	– –	0.85 0.71	1.2 –	Vdc
Reverse Recovery Time	$(I_S = 10\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $di_S/dt = 100\text{ A}/\mu\text{s}$ ) (Note 3)	$t_{rr}$	–	20.4	–	ns
		$t_a$	–	8.25	–	
		$t_b$	–	12.1	–	
Reverse Recovery Stored Charge		$Q_{RR}$	–	0.007	–	$\mu\text{C}$

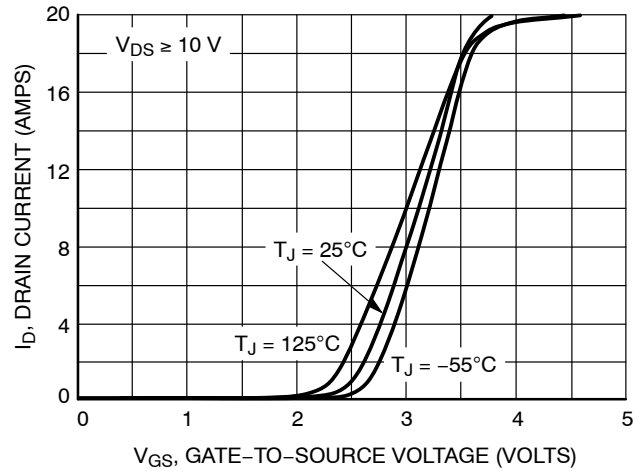
3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

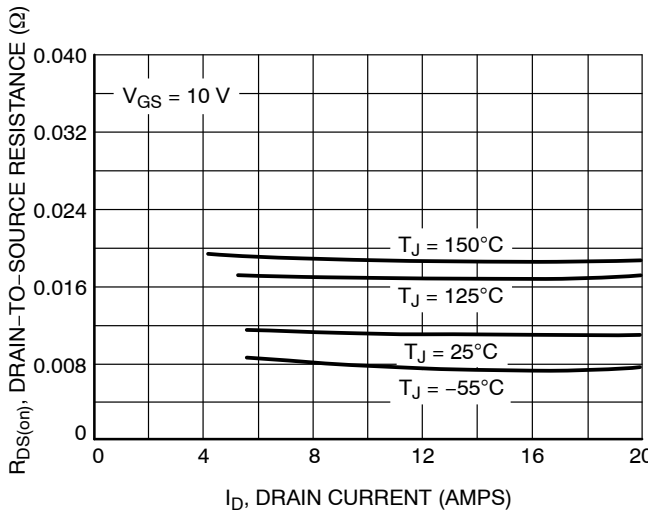
# NTD40N03R



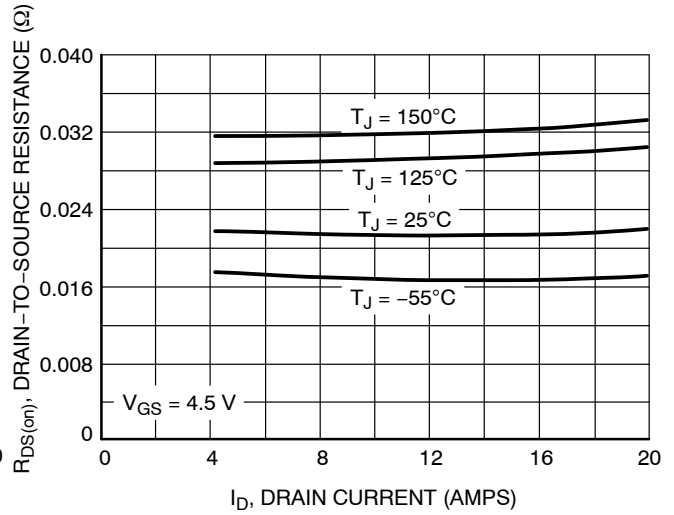
**Figure 1. On-Region Characteristics**



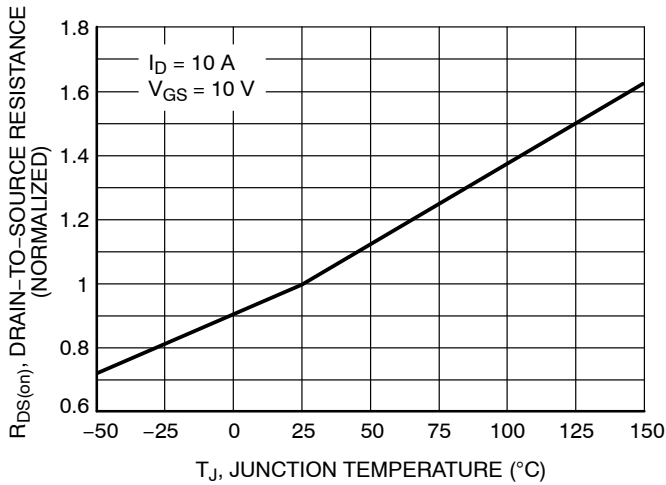
**Figure 2. Transfer Characteristics**



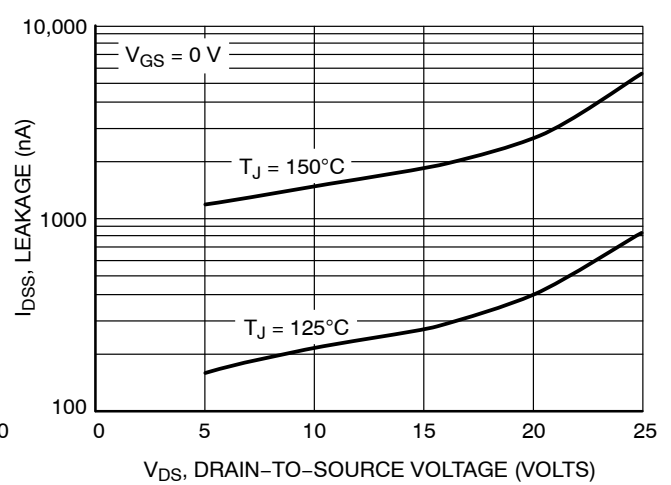
**Figure 3. On-Resistance versus Drain Current and Temperature**



**Figure 4. On-Resistance versus Drain Current and Temperature**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

# NTD40N03R

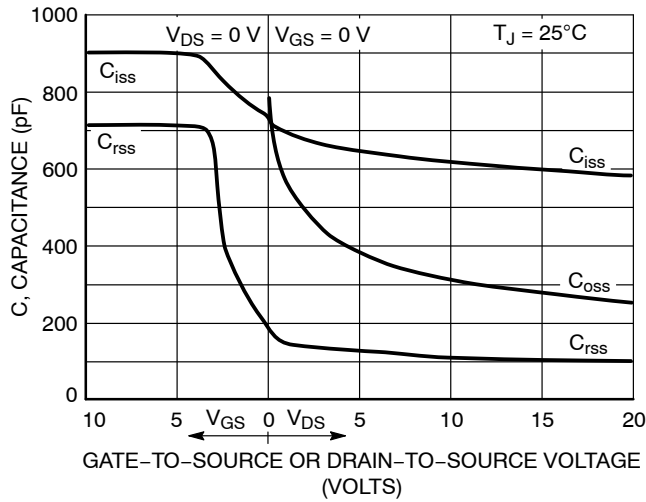


Figure 7. Capacitance Variation

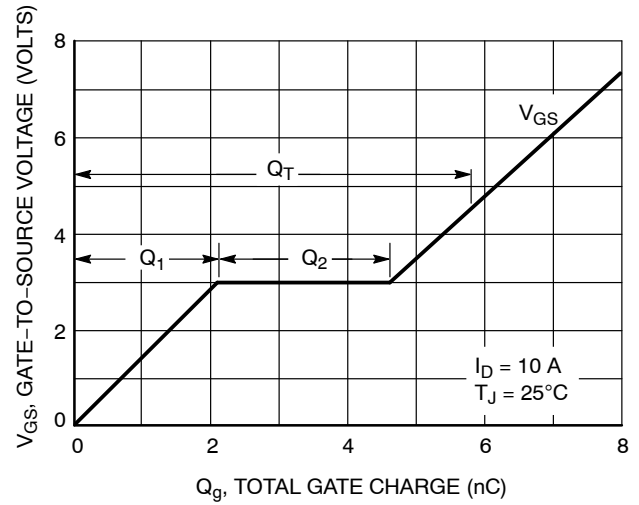


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

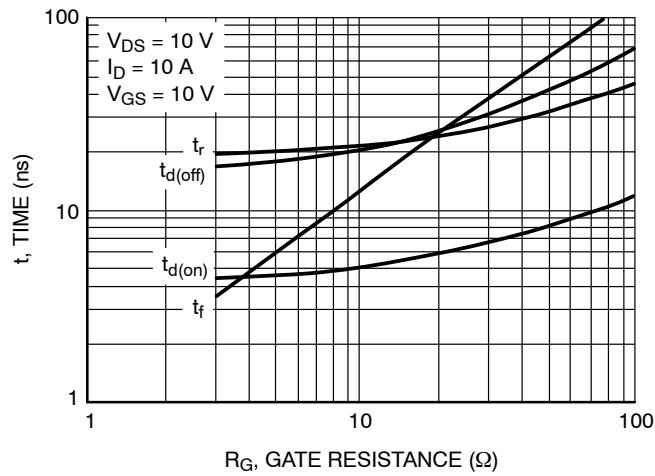


Figure 9. Resistive Switching Time Variation versus Gate Resistance

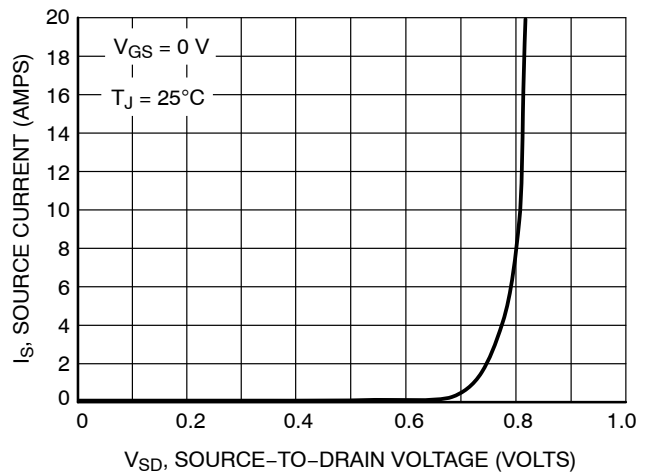


Figure 10. Diode Forward Voltage versus Current

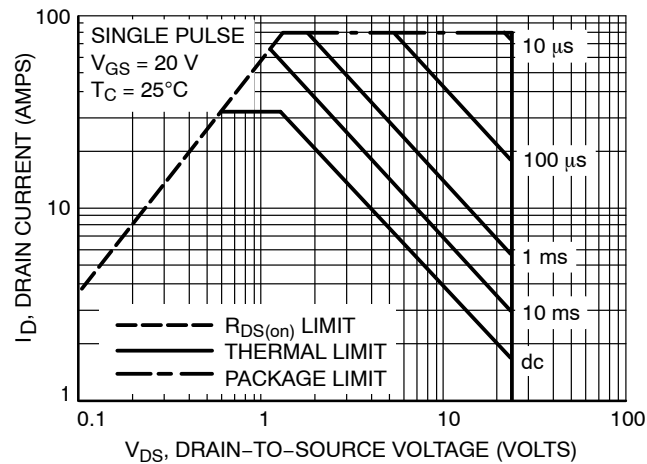


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTD40N03R

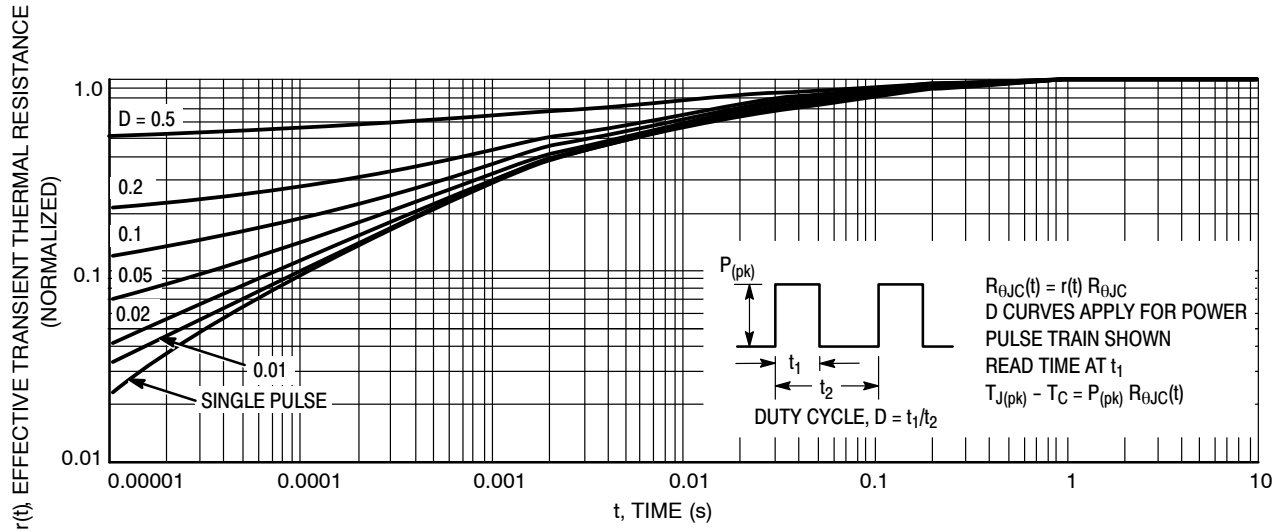


Figure 12. Thermal Response

## ORDERING INFORMATION

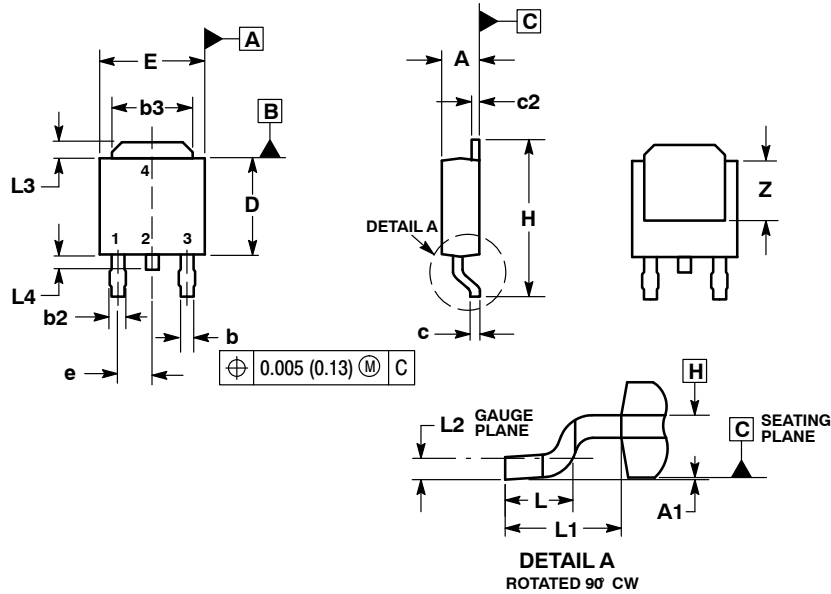
Device	Package	Shipping <sup>†</sup>
NTD40N03R-1G	DPAK (Straight Lead) (Pb-Free)	75 Units/Rail
NTD40N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD40N03R

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE B

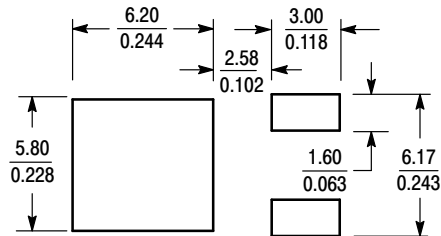


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

#### STYLE 2:

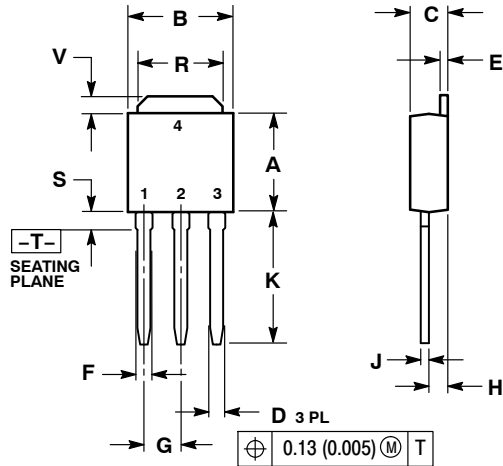
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD40N03R

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369D-01 ISSUE B




#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

#### STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5773-3850

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NTD40N03R/D