Freescale Semiconductor
Product Brief

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MPC5125 Product Brief

Designed for telematics systems and high temperature industrial applications, the MPC5125 32-bit embedded controller is a device from Freescale Semiconductor's mobileGT™ family containing the e300 Power Architecture™ technology core. This core complies with the Power Architecture embedded category, and maintains binary compatible with other processors in the mobileGT product family such as the MPC5121e and MPC5200B. It offers a robust system performance with a smaller package size, while bringing you the reliability and familiarity of the proven Power Architecture technology. An ecosystem of third-party vendors is available to help simplify and speed system design. This document provides an overview of the MPC5125 microcontroller features, including the major functional components.

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1 Applications

The MPC5125 is well suited to network-connected automotive and industrial applications that require complex real-time control and robust performance, such as the following:

- Telematics
- Industrial automation
- Avionics
- Robotics
- Motion control
- Utilities / Power Management
- Medical instrumentation

2 Features

2.1 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5125.

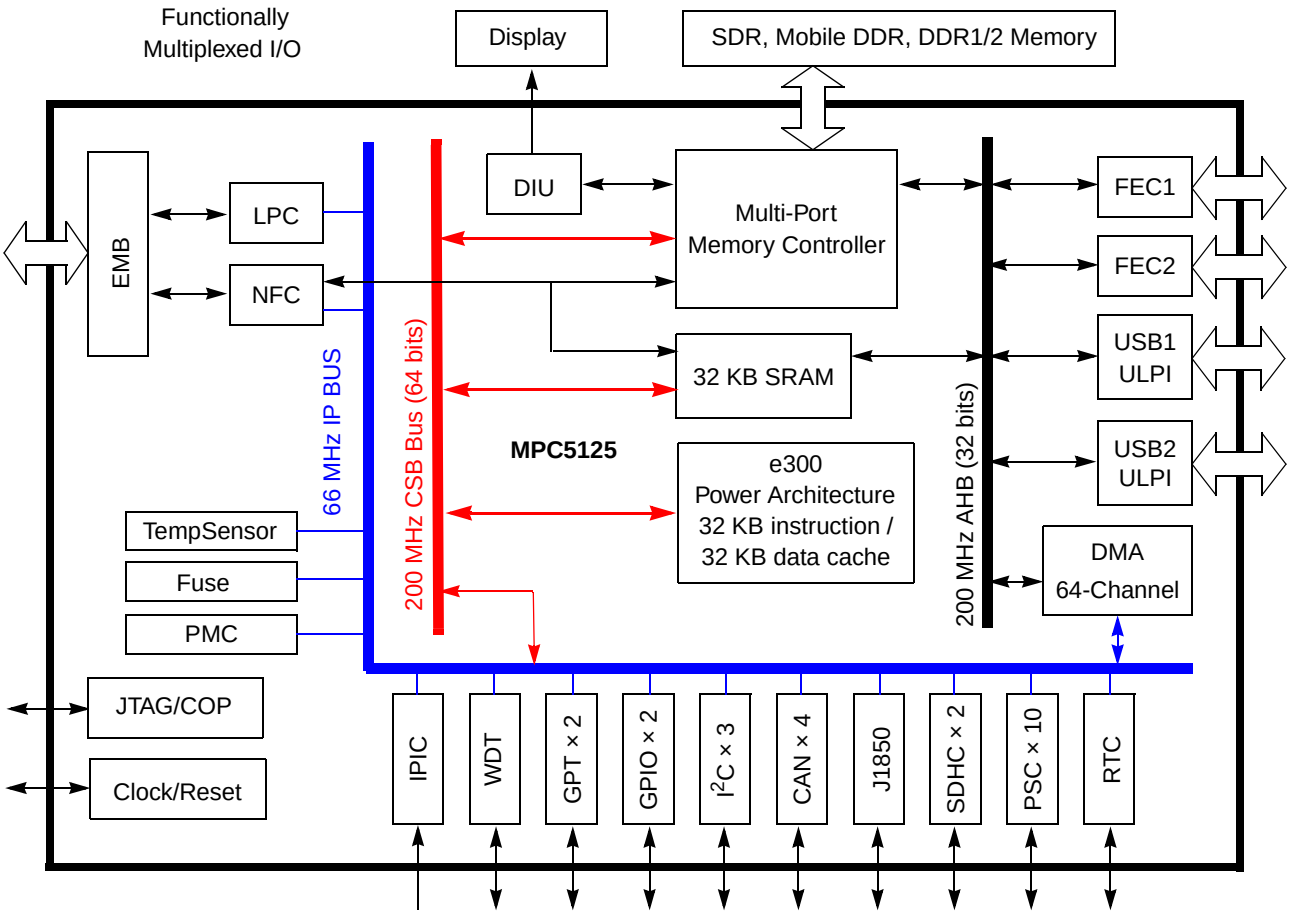

Figure 1. Simplified MPC5125 Block Diagram

2.2 Operating Parameters

- As fast as 400 MHz
- –40 to 125 °C junction temperature

2.3 Package

- 324-pin plastic ball grid array (TEPBGA)

2.4 Chip Level Features

Major features of the MPC5125 are as follows:

- e300 Power Architecture processor core (enhanced version of the MPC603e core), operates as fast as 400 MHz
- Low power design
- Display interface unit (DIU)
- DDR1, DDR2, low-power mobile DDR (LPDDR), and 1.8 V/3.3 V SDR DRAM memory controllers
- 32 KB on-chip SRAM
- USB 2.0 OTG controller with ULPI interface
- DMA subsystem
- Flexible multi-function external memory bus (EMB) interface
- NAND flash controller (NFC)
- LocalPlus interface (LPC)
- 10/100Base Ethernet
- MMC/SD/SDIO card host controller (SDHC)
- Programmable serial controller (PSC)
- Inter-integrated circuit (I^2C) communication interfaces
- Controller area network (CAN)
- J1850 byte data link controller (BDLC) interface
- On-chip real-time clock (RTC)
- On-chip temperature sensor
- IC Identification module (IIM)

2.5 Module Features

The following is a brief summary of the functional blocks in the MPC5125. For more detailed information, refer to the *MPC5125 Reference Manual* (MPC5125RM).

2.5.1 e300 Processor Core

- Power Architecture instruction set

- 32 KB instruction cache
- 32 KB data cache
- High-performance, superscalar processor core with a four-stage pipeline
- Dual-issue processor with integrated floating-point unit and dual integer units
- Dynamic power management

2.5.2 Display Interface Unit (DIU)

- Supports LCD display resolution as high as 1280 × 720
- Supports refresh rate as high as 60 Hz
- Color depth as high as 24 bits per pixel
- Hardware n-plane accelerated blending

2.5.3 USB Controller

- Two on-chip USB controllers with On-The-Go (OTG) host/device capability
- Each supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps)
- Both USB controllers can be accessed through the ULPI interface

2.5.4 Direct Memory Access (DMA) Controller

- 64-channel on-chip DMA engine with advanced capabilities
- Supports channel linking and scatter/gather processing

2.5.5 DDR SDRAM Memory Controller

- Supports 16-bit wide and 32-bit wide DDR1, DDR2, and LPDDR, 32-bit SDR SDRAM devices at speeds as fast as 200 MHz
- Supports two chip selects

2.5.6 32 KB On-chip SRAM

- Usable as e300 core scratch pad memory

2.5.7 Fast Ethernet Controller (FEC)

- Two Ethernet controllers
- Supports 100 Mbps/10 Mbps IEEE 802.3 MII
- Supports 10 Mbps 7-wire interface
- IEEE 802.3 full duplex flow control
- Supports RMII interface

2.5.8 NAND Flash Interface

- Supports NAND flashes with 8-bit or 16-bit data width
- Supports booting from page size ≥ 2 KB NAND devices
- Supports 512 byte/2 KB/4 KB/8 KB page NAND devices
- Supports four chip selects
- BCH ECC engine, 0/4/6/8/12/16/24/32-bit error correction mode

2.5.9 Local Plus Bus (LPC) Interface

- Interface to external memory-mapped or chip-selected devices
- 32-bit address bus
- 32-bit data bus
- Eight chip selects
- Supports burst mode flash
- Supports 32-bit ALE-muxed interface
- Supports as many as 42-bit non-muxed interfaces
- Supports large-packet DMA transfers

2.5.10 Secure Digital Host Controller (SDHC)

- Two SD/SDIO/MMC card interfaces
- Compliant with SD and SDIO specification version 1.x
- Compliant with MMC card specification
- 200 Mbps data rate in 4-bit mode

2.5.11 Controller Area Network (CAN)

- Four CAN interfaces
- Implementation of CAN protocol, version 2.0 A/B
- Programmable wakeup functionality
- Both support either low speed or high speed

2.5.12 Integrated Circuit Communication (I^2C)

- Three inter-integrated circuit (I^2C) communication interfaces
- Input digital noise filtering
- Master and slave modes supported

2.5.13 Programmable Serial Controller (PSC)

- Ten programmable serial controllers (PSC)

- Each PSC is a flexible serial communication engine, supporting the following protocols:
  - Universal asynchronous receiver/transmitter (UART)
  - Codec/Pulse-code modulation (PCM)
  - Inter-IC sound bus (I^2S)
  - Serial Peripheral Interface (SPI)
  - AC97
- Each PSC is serviced by a centralized FIFO to provide buffer storage

2.5.14 J1850 Byte Data Link Controller (BDLC) Interface

- SAE J1850 Class B data communications network interface compliant
- ISO-compatible for low speed (< 125 Kbps) serial data communications
- Digital noise filter

2.5.15 General Purpose I/Os (GPIO)

- 64 general-purpose I/Os (GPIOs)
- Four GPIOs in V_{BAT} power domain available for external wake up

2.5.16 On-chip Real-time Clock (RTC)

- Real-time clock runs from separate V_{BAT} power domain
- Programmable alarm
- Periodic interrupts for one second, one minute, one day
- Runs with external 32 kHz crystal or external clock source

2.5.17 IC Identification Module (IIM)

- One fuse bank user space (32 bytes)

2.5.18 On-chip Temperature Sensor

- Capable of generating an interrupt at a programmable temperature level

2.5.19 Power Modes

- Run
- Doze
- Nap
- Sleep
- Deep sleep mode
- Hibernation mode

2.5.20 System Timer

- Real-time clock
- 16 general-purpose timers

2.5.21 IEEE 1149.1 Compliant JTAG Boundary Scan

3 Developer Environment

The MPC5125 supports similar tools and third party developers as other mobileGT products, offering a widespread, established network of tools and software vendors.

The following development support is available.

- Evaluation/development boards
- IDE/tool chains
- C/C++ compilers
- Hardware and software debuggers
- Initialization/boot code generators
- Software libraries
- Device/module drivers
- JTAG interfaces
- Third party real-time operating systems (RTOS)

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