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MC56F844x/5x/7x Product Brief

Supports MC56F844x, MC56F845x, MC56F847x

Contents

1 Introduction

The 56F844x/5x/7x is the initial family of 32-bit 56800EX core–based Digital Signal Controllers (DSCs). Each device in the family combines, on a single chip, the processing power of a 32-bit DSP and the functionality of a microcontroller with a flexible set of peripherals. Due to its cost-effectiveness, configuration flexibility, and compact program code, the 56F844x/5x/7x is well-suited for many consumer and industrial applications.

The 56800EX core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications. Additionally, memory resource protection (MRP) is provided to protect supervisor programs and resources from user programs.

The 56F844x/5x/7x supports up to 100 MHz program execution from both internal flash memory and RAM. Both on-chip flash memory and RAM can also be mapped into both program and data memory spaces. Two data operands can be accessed from the on-chip data RAM per instruction cycle.

1.1 Core Overview

The 56F844x/5x/7x family is based on an 56800EX core, which updates the 56800E core. The 56800EX core has all 56800E core features and adds new enhancements, including:

- 32-bit x 32-bit MUL/MAC operations
- all registers in the Address Generation Unit (AGU) have shadowed registers that effectively reduce the context save/ restore time during exception processing, reducing latency
- bit-reverse address mode supporting Fast Fourier Transform
- new bit manipulation instruction that integrates a Test bitfield and a Set/Clear (BFSC) bitfield into a single instruction

With all existing 32-bit arithmetic operations, the 56800EX core is truly 32-bit compatible.

1.2 Memory Overview

Devices in the 56F844x/5x/7x family include multiple blocks of on-chip memory:

- Up to 256 KB (128 KW) program flash memory
- Up to 32 KB (16 KW) data flash memory
- Up to 32 KB (16 KW) RAM

Both bulk erasing and erasing in pages are supported.

1.3 Peripheral Overview

A full set of programmable peripherals—including eFlexPWMs, ADCs, QSCIs, QSPIs, I2Cs, a FlexCAN, Inter-Module Crossbars, Quad Timers, a CRC block, DACs, Analog Comparators, and on-chip/off-chip clock sources—supports various applications. Each peripheral's clock can be independently gated to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

2 Application Examples

With numerous, highly integrated peripherals and powerful processing capabilities, the 56F844x/5x/7x family is especially useful for switched-mode power supplies (SMPSs), advanced motor control (including dual motor control), smart appliances, uninterruptible power supplies (UPSs), photovoltaic systems, power distribution systems, wireless charging, and advanced lighting systems.

Table 1. Sample Applications

Application	Examples
Switched-mode power supplies (SMPSs)	• Multi-output digital SMPSs • Interleaving Power Factor Correction (PFC) • Multiple phase converters • LLC DC to DC converters

Table continues on the next page...

Table 1. Sample Applications (continued)

Application	Examples
Advanced motor control	• Universal motors • DC motors • AC Induction Motors (ACIMs) • Brushless DC (BLDC) motors • Permanent Magnet Synchronous Motors (PMSMs) • Switched Reluctance (SR) motors • Stepper motors • Linear motors • Actuators • Poly-phase motors • Dual motor control
Smart appliances	• Washing machines • Dryers • Dishwashers • Induction cookers
Uninterruptible power supplies (UPSs)	• Single phase UPS • Three phase online UPS
Photovoltaic systems	• Residential solar inverter • Grid-tied three phase solar inverter • Micro-inverter • Fuel cell generator
Power distribution systems	• Circuit breakers • Arc fault detectors • Power quality monitors
Wireless charging	
Advanced lighting systems	

3 Features

The following list summarizes the superset of features across the entire 56F844x/5x/7x family.

- 56800EX 32-bit DSC core
- Up to 100 MHz operation frequency
- Up to 128 KW program/data flash memory
- Up to 16 KW dual port program/data RAM
- FlexMemory and configuration options:
  - Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
  - Up to 1 KW FlexRAM, which can be used as additional RAM
  - When FlexNVM and FlexRAM are used in conjunction: Up to 1 KW high-endurance, enhanced EEPROM, or a combination of data flash memory and EEPROM
- Memory resource protection (MRP) unit:
  - Partitions software into two modes—supervisor software and user software—with separate system address spaces and resources, for both program and data
  - Protects supervisor programs and resources from user programs
- Four-channel DMA
- One 8-channel eFlexPWM module with NanoEdge™ placement and enhanced capture
- One 8-channel eFlexPWM module with accumulative fractional clock calculation and enhanced capture
- 2 x 8-channel 12-bit cyclic ADC with 300 ns conversion speed

- 1 x 24-channel 16-bit SAR ADC with temperature sensor
- Watchdog timer
- Cyclic Redundancy Check (CRC) Generator
- On-chip 8 MHz/400 kHz relaxation oscillator, 32 kHz Relaxation Oscillator and 4 MHz to 16 MHz Crystal Oscillator (XOSC)
- Power Supervisor
- Inter-Module Crossbar
- Programmable Interrupt Controller (INTC)
- Two Quad Timers
- One Quadrature Decoder
- Two Periodic Interval Timers
- Two Programmable Delay Blocks
- One 12-bit DAC
- Four 6-bit DACs (64-tap voltage reference)
- Four High Speed Comparators
- Three Queued SPI modules
- Three Queued SCI modules
- Two I2C/SMBus modules
- One FlexCAN module
- 5 V tolerant I/O

3.1 MC56F844x/5x/7x Product Family

The following table highlights major features, including features that differ among members of the family. Features not listed are shared in common by all members of the family.

Table 2. 56F844x/5x/7x Family

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
Core frequency (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory, including FlexNVM (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Table 2. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
12-bit Cyclic ADC channels	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x5 (600 ns)	2x8 (600 ns)	2x5 (600 ns)
16-bit SAR ADC (with Temp Sensor) channels	1x 16	1x 10	1x 16	1x 10	1x8	1x8	0	1x8	0	1x 16	1x 10	1x 16	1x 10	0	1x8	0	1x8	0
PWMA with input capture:																		
High-resolution channels	1x8	1x8	1x8	1x8	1x8	1x8	1x6	1x8	1x6	0	0	0	0	0	0	0	0	0
Standard channels	4	1	4	1	1	1	0	1	0	2x 12	1x 12, 1x9	2x 12	1x 12, 1x9	1x9	1x9	1x6	1x9	1x6
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total assumes no FlexNVM is used with FlexRAM for EEPROM.

3.2 Block Diagram

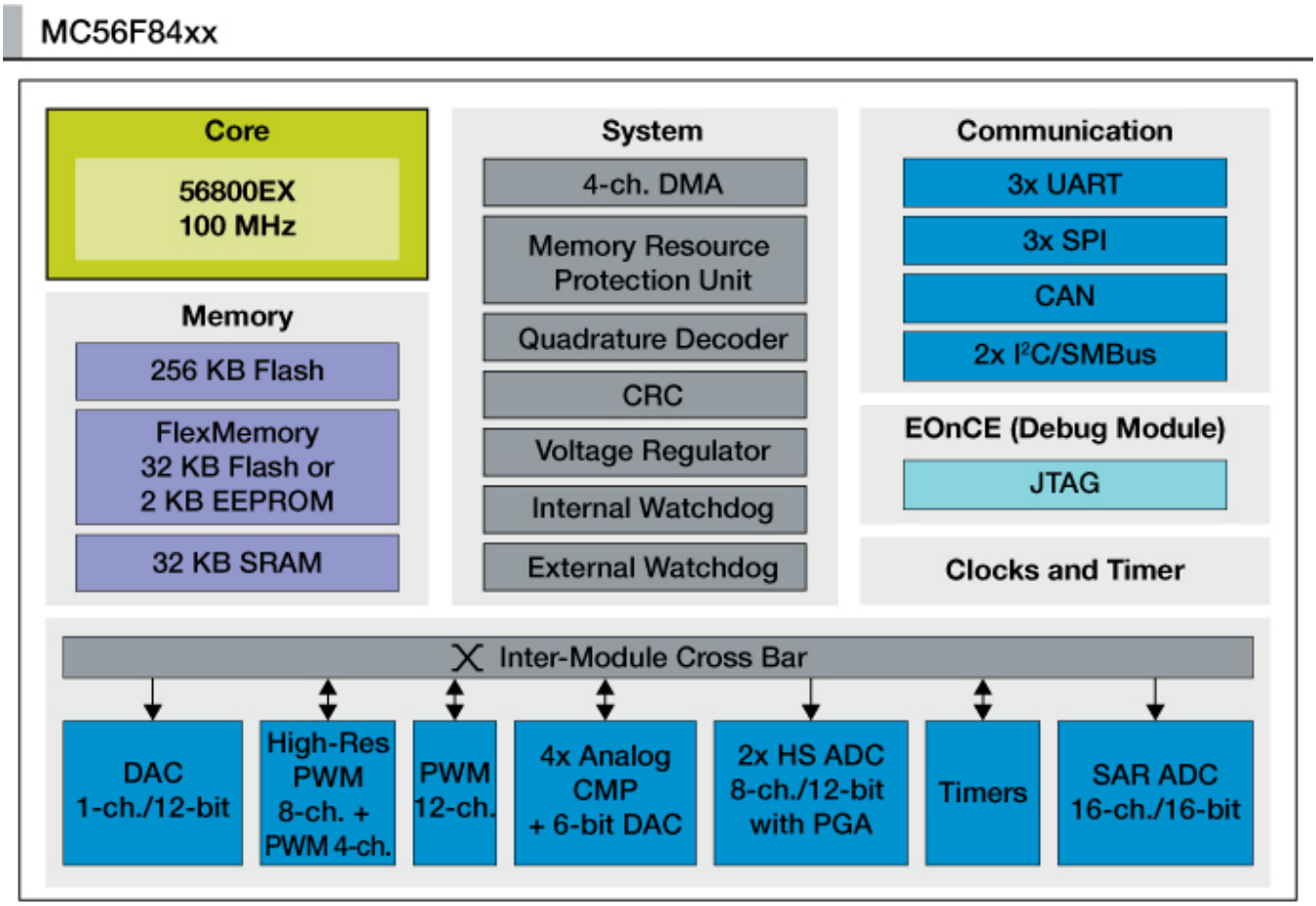

Figure 1. Block Diagram

3.3 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, effectively supporting DSP and Fast Fourier Transform algorithms

- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers corresponding to the R0, R1, R2, R3, R4, R5, N, N3, and M01 address registers
- Instruction set supporting both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

3.4 Operation Parameters

- Up to 100 MHz operation at -40 ºC to 105 ºC ambient temperature
- Single 3.3 V power supply
- Supply range: Vdd - Vss = 2.7 V to 3.6 V, Vdda - Vssa = 2.7 V to 3.6 V

3.5 Packages

- 48LQFP
- 64LQFP
- 80LQFP
- 100LQFP

3.6 On-Chip Memory and Memory Protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.
    - Concurrent accesses provide increased performance.
    - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
    - Up to 128 KW program/data flash memory
    - Up to 16 KW dual port data/program RAM
    - Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
    - Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

3.7 Peripherals

3.7.1 System Modules

3.7.1.1 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

3.7.1.2 Direct Memory Access (DMA) Controller

- Four independently programmable DMA controller channels
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-bit, 16-bit, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation
- One programmable input selected from 16 possible peripheral requests per channel
- Automatic hardware acknowledge/done indicator from each channel
- Independent source and destination address registers
- Optional modulo addressing and automatic updates of source and destination addresses
- Independent transfer sizes for source and destination
- Optional auto-alignment feature for source or destination accesses
- Optional automatic single or double channel linking
- Programming model accessed via 32-bit slave peripheral bus
- Channel arbitration on transfer boundaries using fixed priority scheme
- DMA peripherals:
  - Quad Timer
  - ADCs
  - Quadrature Decoder
  - QSPIs
  - QSCIs
  - I2Cs
  - PWMs
  - Crossbar
  - 12-bit DAC

3.7.1.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar

- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

3.7.1.4 Cyclic Redundancy Check (CRC) Generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

3.7.2 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

3.7.3 Timers and PWM modules

3.7.3.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

Most devices in the 56F847x family have PWMA and PWMB. Devices in the 56F844x/5x families have PWMA only.

- Up to 12 output channels in each module
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with NanoEdge high resolution
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - NanoEdge implementation: 312 ps PWM frequency and duty-cycle resolution
- PWMB with supporting accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average
- Each complementary pair can operate with its own PWM frequency base and deadtime values
  - 4 time base in each PWM module
  - Independent top and bottom deadtime insertion for each complementary pair
- PWM outputs can operate as complementary pairs or independent channels
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input
  - Channels not used for PWM generation can be used for buffered output compare functions

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

    - Channels not used for PWM generation can be used for input capture functions
    - Enhanced dual edge capture functionality
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers

3.7.3.2 Quad Timer

- Four 16-bit up/down counters with programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

3.7.3.3 Enhanced Quadrature Decoder

- Includes logic to decode quadrature signals
- Configurable digital filter for inputs to remove glitches and ensure only true transitions are recorded
- 32-bit position counter register
- 16-bit position difference register
- Maximum count frequency equals the IPBus clock rate
- Position counter can be initialized by software or external events
- Position counter and resolution counter can be captured by external trigger signal (new feature)
- Preloadable 16-bit revolution counter
- Inputs can be connected to a general purpose timer, aiding low speed velocity measurements
- Watchdog timer to detect a non-rotating shaft condition
- Optional use as a single phase pulse accumulator

3.7.3.4 Periodic Interrupt Timer (PIT) Modules

- 16-bit up-counter with programmable counter modulo
- Interrupt capability
- Selectable clock sources:
    - External crystal oscillator/external clock source
    - On-chip low-power 32 kHz oscillator
    - System bus (IPBus up to 100 MHz)
    - 8 MHz / 400 kHz ROSC
- Can signal the device to exit powerdown mode
- Programmable master/slave selection between PIT instances

3.7.3.5 Programmable Delay Block (PDB) Modules

- 16-bit counter with programmable counter modulo and delay time

- Counter is initiated by positive transition of internal or external trigger pulse
- Support for synchronizing PWM and ADC conversions
- Two PDB outputs can be ORed together to schedule two conversions from one input trigger event
- PDB outputs can be used to schedule precise edge placement for a pulsed output that generates the control signal for the CMP windowing comparison
- Support for continuous mode or single shot mode
- Bypass mode supported

3.7.3.6 Computer Operating Properly (COP) Watchdog

- Programmable timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

3.7.3.7 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable time-out period
- Interrupt capability prior to time-out
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM time-out occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and stop mode operation is not supported
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC

3.7.4 Clock Modules

3.7.4.1 On-Chip Oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

3.7.4.2 Crystal Oscillator

- Support for both high ESR crystal oscillator (greater than 100-ohm ESR) and ceramic resonator
- 4 MHz to 16 MHz operating frequency

3.7.4.3 Phase Locked Loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz

- Detection of loss of lock and loss of reference clock
- Ability to power down

3.7.5 Analog Modules

3.7.5.1 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency is up to 20 MHz with 50 ns period
  - Single conversion time of 8.5 ADC clock cycles (8.5 x 50 ns = 425 ns)
  - Additional conversion time of 6 ADC clock cycles (6 x 50 ns = 300 ns)
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by any module connected to internal crossbar module, such as PWM and timer modules and GPIO and comparators
- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results

3.7.5.2 16-bit Analog-to-Digital Converter (SAR type)

- Linear successive approximation algorithm with up to 16-bit resolution
- Differential and 16 single-ended external analog inputs
- Maximum ADC clock frequency up to 12.5 MHz
- Output modes: single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes
- Output formatted in 2's complement, 16-bit sign extended for differential modes
- Output in right-justified, unsigned format for single-ended modes
- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Conversion complete / hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low-power modes for lower-noise operation
- Asynchronous clock source for lower-noise operation with option to output the clock
- Automatic compare with interrupt for less-than, greater-than, or equal-to, within range or out-of-range programmable value
- Integrated temperature sensor
- Selectable voltage reference: internal, external, or alternate

3.7.5.3 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth waveforms
- Programmable period, update rate, and range
- Output can be routed to internal comparator, ADC, or optionally off chip

3.7.5.4 6-bit Digital-to-Analog Converter

- 2.7 V to 3.3 V operation range
- 64-tap resistor ladder

- Selectable supply reference source
- Powerdown mode to conserve power when not in use
- Output routed to internal comparator input
- Less than 20 µA power consumption

3.7.5.5 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

3.7.6 Communication Interfaces

3.7.6.1 Queued Serial Peripheral Interface (QSPI) Modules

- Maximum 25 Mbps baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

3.7.6.2 Queued Serial Communications Interface (QSCI) Modules

- Operating clock up to two times CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

3.7.6.3 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) Modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Dual slave addresses
- Programmable glitch input filter

3.7.6.4 Flex Controller Area Network (FlexCAN) Module

- Clock source from PLL or XOSC/CLKIN
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers, each configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

3.7.7 Power Management

3.7.7.1 On-Chip Voltage Regulator

- Input 2.7 V to 3.6 V (4.0 V absolute maximum rating)
- Provides 1.2 V ± 10% accuracy
- Separate large and small regulators
- Distributed type layout

3.7.7.2 Power Supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (VDD > 2.1 V)
- Brownout reset (VDD < 1.9 V)
- Critical warn low voltage interrupt (LVI2.0)
- Peripheral low voltage interrupt (LVI2.7)

4 Developer Environment

The following table summarizes available development tools.

Tool	Description
TWR-56F8400	Cost-effective development board that is part of the Freescale Tower System, a modular development platform that enables rapid prototyping and re-use through reconfigurable hardware
TWR-MC-LV3PH	3-Phase Low Voltage Motor Control Module for TWR-56F8400 used to develop DC, BLDC, and PMSM motor control solutions using various algorithms provided by Freescale
TWR-MC-STEPPER	Low Voltage Motor Control Module for TWR-56F8400 used to develop stepper motor control solutions using various algorithms provided by Freescale

Table continues on the next page...

Tool	Description
TWR-ELEV Elevator Module	Elevator modules are the basic building block of Freescale's Tower System. Designed to connect microcontroller and peripheral modules, Elevator modules provide the power regulation circuitry and structural integrity needed for all configurations of an assembled Tower System.
CodeWarrior for Microcontrollers 10.2[1]	This comprehensive integrated development environment (IDE), based in Eclipse,™ provides a highly visual and automated framework to accelerate the development of most complex embedded applications.
Processor Expert[1]	Rapid application design tool that combines easy-to-use component-based application creation with an expert knowledge system
FreeMASTER[1]	FreeMASTER software represents a sophisticated tool with intuitive navigation that can be used in any application development. This tool allows control of an application remotely from a user-friendly graphical environment running on a PC. It also provides the ability to view realtime application variables in both textual and graphical form.
Embedded Software Library[1]	Freescale Embedded Software Library v1.0 for MC56F84xx

1. Complimentary

5 Document Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 4. Revision History

Revision	Substantive Change(s)
2	"Introduction": Highlighted the memory resource protection (MRP) feature "Peripheral Overview": Clarified list of supported peripherals and description of power-saving option "Features": Removed Real Time Clock (RTC), and clarified details about supported peripherals "MC56F844x/5x/7x Product Family": Updated the part numbers and their associated features "56800EX 32-bit Digital Signal Controller Core": Added features as well as information about concurrent instruction fetches and dual data accesses "On-Chip Memory and Memory Protection": Added RAM controller details, and simplified description of supported memory sizes "Direct Memory Access (DMA) Controller": Added 12-bit DAC to list of DMA peripherals "Developer Environment": Updated table Provided additional feature details in these sections: • Periodic Interrupt Timer (PIT) Modules • Computer Operating Properly (COP) Watchdog • External Watchdog Monitor (EWM) • Phase Locked Loop Clarified feature details in these sections: • GPIO • Enhanced Flex Pulse Width Modulator (eFlexPWM) • Crystal Oscillator • 16-bit Analog-to-Digital Converter (SAR type) • 6-bit Digital-to-Analog Converter • Comparator • 12-bit Digital-to-Analog Converter • Quad Timer • Queued Serial Communications Interface (QSCI) Modules • Flex Controller Area Network (FlexCAN) Module • On-Chip Voltage Regulator

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