

ESD Protection Diodes Silicon Epitaxial Planar

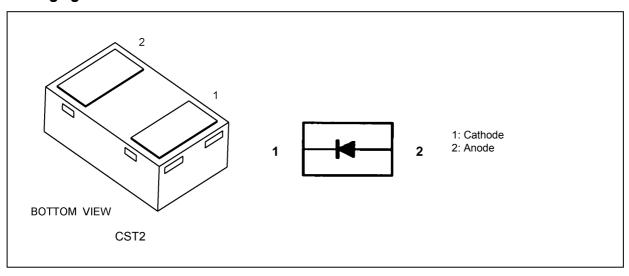
DF2S6.8UCT

1. Applications

· ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

2. Packaging and Internal Circuit



3. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V _{ESD}	±8	kV
Junction temperature	Tj	150	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



4. Electrical Characteristics (Unless otherwise specified, T_a = 25°C)

 V_{RWM} : Working peak reverse voltage

V_{BR}: Reverse breakdown voltage

I_{BR}: Reverse breakdown current

V_R: Reverse voltage I_R: Reverse current V_F: Forward voltage I_F: Forward current V_C: Clamping voltage I_{PP}: Peak pulse current R_{DYN}: Dynamic resistance

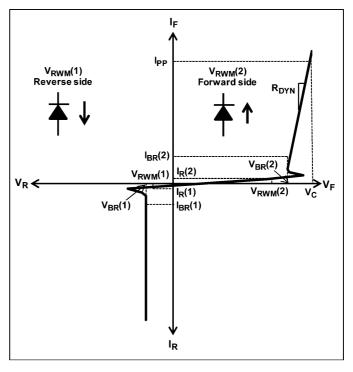


Fig. 4.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V _{RWM} (1)		_	_	_	5	V
Reverse breakdown voltage	V _{BR} (1)		I _{BR} = 1 mA	5.3	6.8	_	V
Reverse current	I _R (1)		V _{RWM} = 5 V	_	_	0.1	μА
Dynamic resistance	R _{DYN}	(Note 1)		_	0.3	_	Ω
Total capacitance	Ct		V _R = 0 V, f = 1 MHz	_	1.6	_	pF
Working peak reverse voltage	V _{RWM} (2)		_	_	_	19	V
Reverse breakdown voltage	V _{BR} (2)		I _{BR} = 1 mA	22	25	_	V
Reverse current	I _R (2)		V _{RWM} = 19 V	_	_	0.5	μА

Note 1: TLP parameter: Z0 = 50 Ω , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using a least-squares fit of TLP characteristics at I_{PP} between 3 A to 8 A.

5. Guaranteed ESD Protection (Note)

Test Condition	ESD Protection		
IEC61000-4-2 (Contact discharge)	±8 kV		

Criterion: No damage to devices.



6. Marking

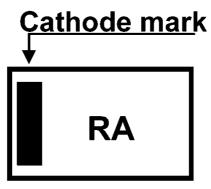


Fig. 6.1 Marking

Marking Code	Part Number		
RA	DF2S6.8UCT		

7. Land Pattern Dimensions (for reference only)

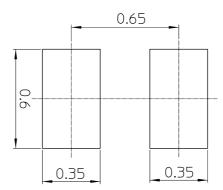


Fig. 7.1 Land Pattern Dimensions (Unit: mm)

8. Characteristics Curves (Note)

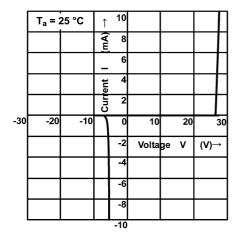


Fig. 8.1 I - V

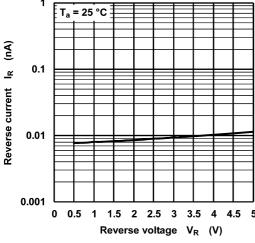


Fig. 8.2 $I_R - V_R (V_{RWM} (1) \text{ side})$

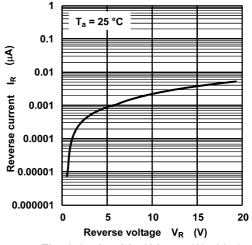
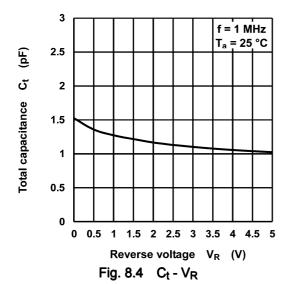


Fig. 8.3 I_R - V_R (V_{RWM} (2) side)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

9. ESD Clamp Waveform (Note)

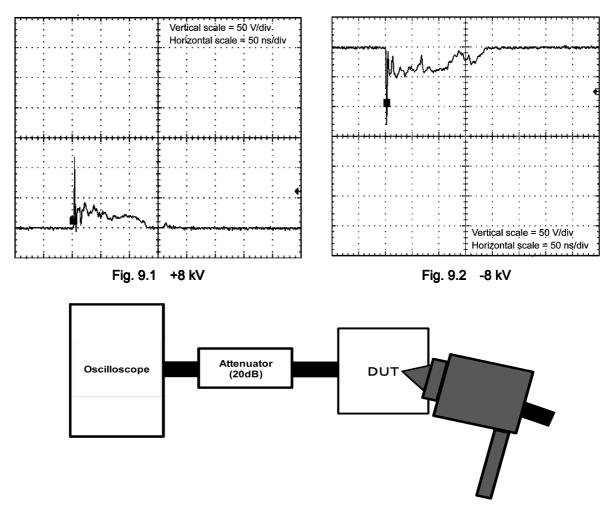


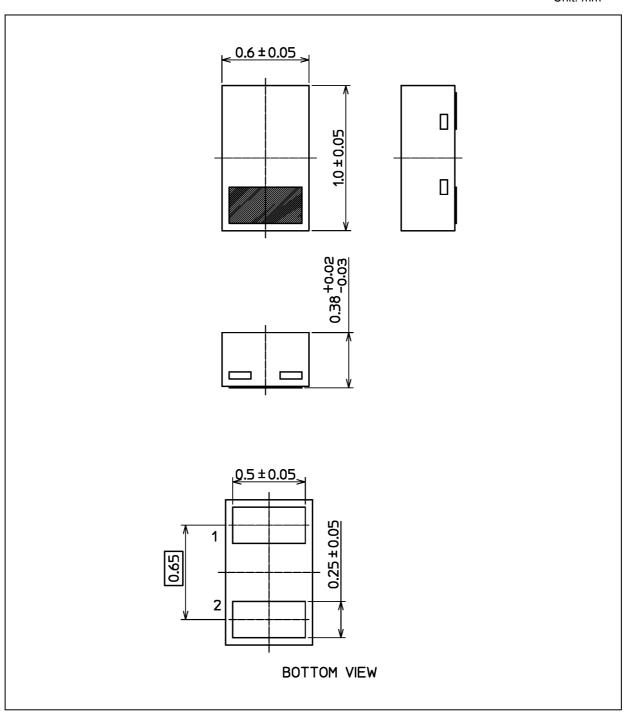
Fig. 9.3 IEC61000-4-2(Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.7 mg (typ.)

	Package Name(s)
TOSHIBA: 1-1P1S	
Nickname: CST2	

Rev.3.0



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