

1Mbps, 2.5kVRMS DIGITAL ISOLATORS

Features

- High-speed operation
 - DC to 1 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
 - 2.5–5.5 V
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- High electromagnetic immunity
- Ultra low power (typical)
 - 5 V Operation
 - 1.6 mA per channel at 1 Mbps
 - 2.5 V Operation
 - 1.5 mA per channel at 1 Mbps
- Tri-state outputs with ENABLE
- Schmitt trigger inputs
- Transient Immunity 50 kV/μs
- AEC-Q100 qualification
- Wide temperature range
 - –40 to 125 °C
- RoHS-compliant packages
 - SOIC-16 wide body
 - SOIC-16 narrow body
 - SOIC-8 narrow body

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communication systems

Safety Regulatory Approvals

- UL 1577 recognized
 - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
 - IEC 60950-1, 61010-1
- VDE certification conformity
 - IEC 60747-5-2 (VDE0884 Part 2)
- CQC certification approval
 - GB4943.1

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors.

All products support Data rates up to 1 Mbps and Enable inputs which provide a single point control for enabling and disabling output drive. All products are safety certified by UL, CSA, VDE, and CQC and support withstand ratings up to 2.5 kV_{RMS}.

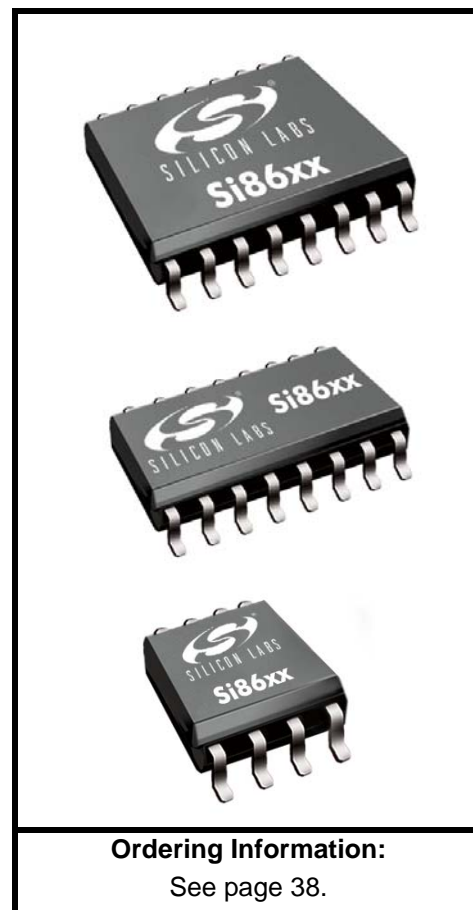


TABLE OF CONTENTS

| <u>Section</u> | <u>Page</u> |
|---|--------------------|
| 1. Electrical Specifications | 4 |
| 2. Functional Description | 29 |
| 2.1. Theory of Operation | 29 |
| 3. Device Operation | 30 |
| 3.1. Device Startup | 32 |
| 3.2. Undervoltage Lockout | 32 |
| 3.3. Layout Recommendations | 33 |
| 4. Pin Descriptions (Si861x/2x Narrow Body SOIC-8) | 34 |
| 5. Pin Descriptions (Si863x) | 35 |
| 6. Pin Descriptions (Si864x) | 36 |
| 7. Pin Descriptions (Si8650/51/52) | 37 |
| 8. Pin Descriptions (Si866x) | 38 |
| 9. Ordering Guide | 39 |
| 10. Package Outline: 16-Pin Wide Body SOIC | 40 |
| 11. Land Pattern: 16-Pin Wide-Body SOIC | 42 |
| 12. Package Outline: 16-Pin Narrow Body SOIC | 43 |
| 13. Land Pattern: 16-Pin Narrow Body SOIC | 45 |
| 14. Package Outline: 8-Pin Narrow Body SOIC | 46 |
| 15. Land Pattern: 8-Pin Narrow Body SOIC | 47 |
| 16. Top Markings | 48 |
| 16.1. Top Marking (16-Pin Wide Body SOIC) | 48 |
| 16.2. Top Marking Explanation (16-Pin Wide Body SOIC) | 48 |
| 16.3. Top Marking (16-Pin Narrow Body SOIC) | 49 |
| 16.4. Top Marking Explanation (16-Pin Narrow Body SOIC) | 49 |
| 16.5. Top Marking (8-Pin Narrow Body SOIC) | 50 |
| 16.6. Top Marking Explanation (8-Pin Narrow Body SOIC) | 50 |
| Contact Information | 52 |

1. Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------|-----------|-----|-----|-----|------|
| Ambient Operating Temperature* | T_A | -40 | 25 | 125 | °C |
| Supply Voltage | V_{DD1} | 2.5 | — | 5.5 | V |
| | V_{DD2} | 2.5 | — | 5.5 | V |

*Note: The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics

($V_{DD1} = 5 V \pm 10\%$, $V_{DD2} = 5 V \pm 10\%$, $T_A = -40$ to 125 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|-----------|----------------------------|--------------------------|------|----------|----------|
| VDD Undervoltage Threshold | VDDUV+ | V_{DD1}, V_{DD2} rising | 1.95 | 2.24 | 2.375 | V |
| VDD Undervoltage Threshold | VDDUV- | V_{DD1}, V_{DD2} falling | 1.88 | 2.16 | 2.325 | V |
| VDD Undervoltage Hysteresis | VDDHYS | | 50 | 70 | 95 | mV |
| Positive-Going Input Threshold | VT+ | All inputs rising | 1.4 | 1.67 | 1.9 | V |
| Negative-Going Input Threshold | VT- | All inputs falling | 1.0 | 1.23 | 1.4 | V |
| Input Hysteresis | V_{HYS} | | 0.38 | 0.44 | 0.50 | V |
| High Level Input Voltage | V_{IH} | | 2.0 | — | — | V |
| Low Level input voltage | V_{IL} | | — | — | 0.8 | V |
| High Level Output Voltage | V_{OH} | $I_{OH} = -4$ mA | $V_{DD1}, V_{DD2} - 0.4$ | 4.8 | — | V |
| Low Level Output Voltage | V_{OL} | $I_{OL} = 4$ mA | — | 0.2 | 0.4 | V |
| Input Leakage Current | I_L | | — | — | ± 10 | μA |
| Output Impedance ¹ | Z_O | | — | 50 | — | Ω |
| Enable Input High Current | I_{ENH} | $V_{ENx} = V_{IH}$ | — | 2.0 | — | μA |
| Enable Input Low Current | I_{ENL} | $V_{ENx} = V_{IL}$ | — | 2.0 | — | μA |

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50Ω , $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued) $(V_{DD1} = 5 V \pm 10\%, V_{DD2} = 5 V \pm 10\%, T_A = -40 \text{ to } 125 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| DC Supply Current (All inputs 0 V or at Supply) | | | | | | |
| Si8610Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 0.6 | 1.2 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 0.8 | 1.5 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 1.8 | 2.9 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 0.8 | 1.5 | |
| Si8620Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 0.8 | 1.4 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 1.4 | 2.2 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 3.3 | 5.3 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 1.4 | 2.2 | |
| Si8621Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 1.2 | 1.9 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 2.4 | 3.8 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 2.4 | 3.8 | |
| Si8630Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 0.9 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 1.9 | 3.0 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 4.6 | 7.4 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 1.9 | 3.0 | |
| Si8631Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.3 | 2.1 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 1.7 | 2.7 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 3.9 | 5.9 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 3.0 | 4.5 | |
| Si8640Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.0 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.4 | 3.8 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 6.1 | 9.2 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 2.5 | 4.0 | |
| Si8641Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.4 | 2.2 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.3 | 3.7 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 5.2 | 7.8 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 3.6 | 5.4 | |
| Si8642Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.8 | 2.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 1.8 | 2.9 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 4.4 | 6.6 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 4.4 | 6.6 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

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Table 2. Electrical Characteristics (Continued)

($V_{DD1} = 5 V \pm 10\%$, $V_{DD2} = 5 V \pm 10\%$, $T_A = -40$ to 125 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|------|------|
| Si8650Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.1 | 1.8 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.1 | 4.7 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 7.0 | 9.8 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 3.3 | 5.0 | |
| Si8651Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.5 | 2.4 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.7 | 4.1 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 6.6 | 9.2 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 4.0 | 6.0 | |
| Si8652Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 2.0 | 3.0 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.4 | 3.6 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 5.6 | 7.8 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 5.0 | 7.5 | |
| Si8660Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.5 | 5.3 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 8.8 | 12.3 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 3.7 | 5.6 | |
| Si8661Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.7 | 2.7 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.4 | 5.1 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 7.9 | 11.1 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 4.8 | 7.2 | |
| Si8662Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 2.2 | 3.3 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.0 | 4.5 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 7.5 | 10.5 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 5.6 | 8.4 | |
| Si8663Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 2.6 | 3.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.6 | 3.9 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 6.5 | 9.1 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 6.5 | 9.1 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 2. Electrical Characteristics (Continued) $(V_{DD1} = 5 V \pm 10\%, V_{DD2} = 5 V \pm 10\%, T_A = -40 \text{ to } 125 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|--------|------------|------------|------|
| 1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all Outputs) | | | | | | |
| Si8610Ax V_{DD1} V_{DD2} | | | — — | 1.2 0.9 | 2.0 1.5 | mA |
| Si8620Ax V_{DD1} V_{DD2} | | | — — | 2.1 1.6 | 3.1 2.4 | mA |
| Si8621Ax V_{DD1} V_{DD2} | | | — — | 1.9 1.9 | 2.9 2.9 | mA |
| Si8630Ax V_{DD1} V_{DD2} | | | — — | 2.8 2.2 | 3.9 3.1 | mA |
| Si8631Ax V_{DD1} V_{DD2} | | | — — | 2.7 2.6 | 3.8 3.6 | mA |
| Si8640Ax V_{DD1} V_{DD2} | | | — — | 3.6 2.9 | 5.0 4.0 | mA |
| Si8641Ax V_{DD1} V_{DD2} | | | — — | 3.4 3.3 | 4.8 4.6 | mA |
| Si8642Ax V_{DD1} V_{DD2} | | | — — | 3.3 3.3 | 4.6 4.6 | mA |
| Si8650Ax V_{DD1} V_{DD2} | | | — — | 4.1 3.7 | 5.7 5.2 | mA |
| Si8651Ax V_{DD1} V_{DD2} | | | — — | 4.2 3.8 | 5.8 5.3 | mA |
| Si8652Ax V_{DD1} V_{DD2} | | | — — | 4.0 4.0 | 5.6 5.6 | mA |
| Si8660Ax V_{DD1} V_{DD2} | | | — — | 5.0 4.2 | 7.0 5.9 | mA |
| Si8661Ax V_{DD1} V_{DD2} | | | — — | 4.9 4.6 | 6.9 6.4 | mA |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

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Table 2. Electrical Characteristics (Continued)

($V_{DD1} = 5 V \pm 10\%$, $V_{DD2} = 5 V \pm 10\%$, $T_A = -40$ to 125 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|--|-----|-----|-----|-------------|
| Si8662Ax | | | | | | |
| V_{DD1} | | | — | 5.1 | 7.1 | mA |
| V_{DD2} | | | — | 4.7 | 6.6 | |
| Si8663Ax | | | | | | |
| V_{DD1} | | | — | 4.9 | 6.8 | mA |
| V_{DD2} | | | — | 4.9 | 6.8 | |
| Timing Characteristics | | | | | | |
| All Models | | | | | | |
| Maximum Data Rate | | | 0 | — | 1 | Mbps |
| Minimum Pulse Width | | | — | — | 250 | ns |
| Propagation Delay | t_{PHL} , t_{PLH} | See Figure 2 | — | — | 35 | ns |
| Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | PWD | See Figure 2 | — | — | 25 | ns |
| Propagation Delay Skew ² | $t_{PSK(P-P)}$ | | — | — | 40 | ns |
| Channel-Channel Skew | t_{PSK} | | — | — | 35 | ns |
| Output Rise Time | t_r | $C_L = 15$ pF See Figure 2 | — | 2.5 | 4.0 | ns |
| Output Fall Time | t_f | $C_L = 15$ pF See Figure 2 | — | 2.5 | 4.0 | ns |
| Peak eye diagram jitter | $t_{JIT(PK)}$ | See Figure 8 | — | 350 | — | ps |
| Common Mode Transient Immunity | CMTI | $V_I = V_{DD}$ or 0 V $V_{CM} = 1500$ V (see Figure 3) | 35 | 50 | — | kV/ μ s |
| Enable to Data Valid | t_{en1} | See Figure 1 | — | 6.0 | 11 | ns |
| Enable to Data Tri-State | t_{en2} | See Figure 1 | — | 8.0 | 12 | ns |
| Start-up Time ³ | t_{SU} | | — | 15 | 40 | μ s |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

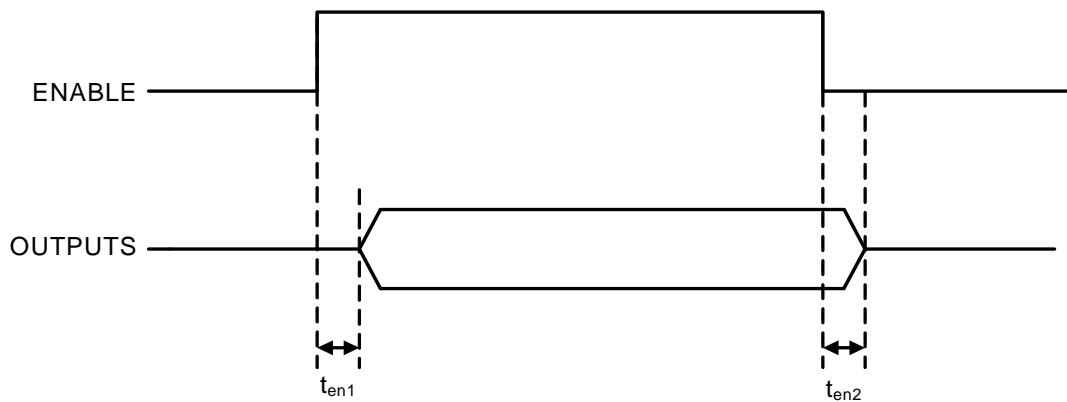


Figure 1. ENABLE Timing Diagram

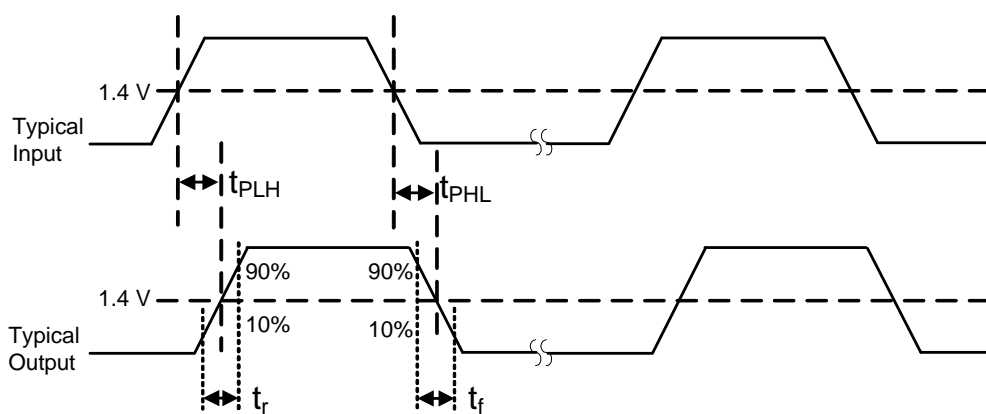


Figure 2. Propagation Delay Timing

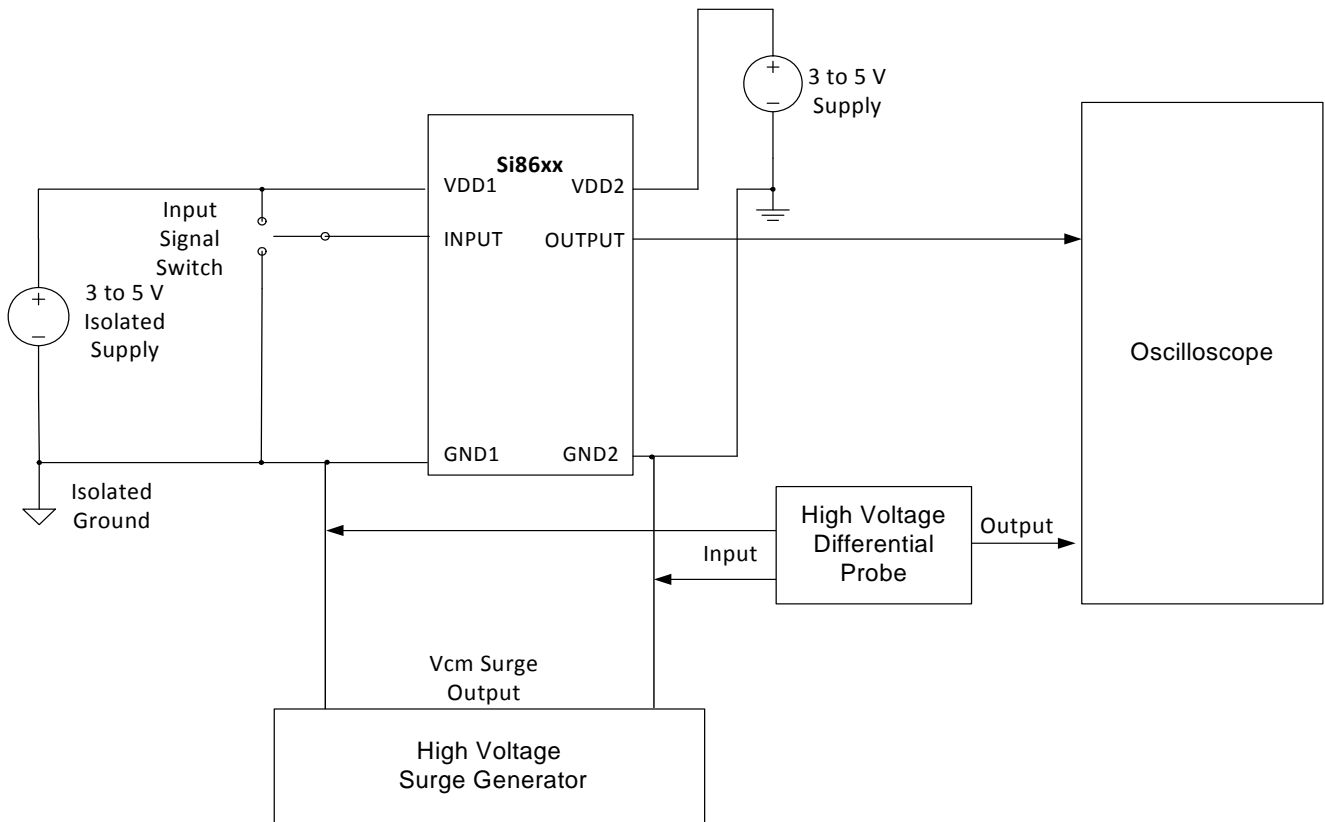


Figure 3. Common-Mode Transient Immunity Test Circuit

Table 3. Electrical Characteristics $(V_{DD1} = 3.3\text{ V} \pm 10\%, V_{DD2} = 3.3\text{ V} \pm 10\%, T_A = -40\text{ to }125\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|----------------------------|--------------------------|------|----------|---------------|
| VDD Undervoltage Threshold | VDDUV+ | V_{DD1}, V_{DD2} rising | 1.95 | 2.24 | 2.375 | V |
| VDD Undervoltage Threshold | VDDUV- | V_{DD1}, V_{DD2} falling | 1.88 | 2.16 | 2.325 | V |
| VDD Undervoltage Hysteresis | VDDHYS | | 50 | 70 | 95 | mV |
| Positive-Going Input Threshold | VT+ | All inputs rising | 1.4 | 1.67 | 1.9 | V |
| Negative-Going Input Threshold | VT- | All inputs falling | 1.0 | 1.23 | 1.4 | V |
| Input Hysteresis | V_{HYS} | | 0.38 | 0.44 | 0.50 | V |
| High Level Input Voltage | V_{IH} | | 2.0 | — | — | V |
| Low Level Input Voltage | V_{IL} | | — | — | 0.8 | V |
| High Level Output Voltage | V_{OH} | loh = -4 mA | $V_{DD1}, V_{DD2} - 0.4$ | 3.1 | — | V |
| Low Level Output Voltage | V_{OL} | lol = 4 mA | — | 0.2 | 0.4 | V |
| Input Leakage Current | I_L | | — | — | ± 10 | μA |
| Output Impedance ¹ | Z_O | | — | 50 | — | Ω |
| Enable Input High Current | I_{ENH} | $V_{ENx} = V_{IH}$ | — | 2.0 | — | μA |
| Enable Input Low Current | I_{ENL} | $V_{ENx} = V_{IL}$ | — | 2.0 | — | μA |
| DC Supply Current (All inputs 0 V or at supply) | | | | | | |
| Si8610Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.6 | 1.2 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 0.8 | 1.5 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 1.8 | 2.9 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 0.8 | 1.5 | |
| Si8620Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.8 | 1.4 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.4 | 2.2 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 3.3 | 5.3 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 1.4 | 2.2 | |
| Si8621Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.2 | 1.9 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 2.4 | 3.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 2.4 | 3.8 | |
| Si8630Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.9 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.9 | 3.0 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 4.6 | 7.4 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 1.9 | 3.0 | |
| Notes: | | | | | | |
| 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. | | | | | | |
| 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. | | | | | | |
| 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Si86xx

Table 3. Electrical Characteristics (Continued)

($V_{DD1} = 3.3\text{ V} \pm 10\%$, $V_{DD2} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------------|-----|-----|-----|------|
| Si8631Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.3 | 2.1 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.7 | 2.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 3.9 | 5.9 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.0 | 4.5 | |
| Si8640Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.0 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.4 | 3.8 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 6.1 | 9.2 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 2.5 | 4.0 | |
| Si8641Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.4 | 2.2 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.3 | 3.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 5.2 | 7.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.6 | 5.4 | |
| Si8642Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.8 | 2.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.8 | 2.9 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 4.4 | 6.6 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 4.4 | 6.6 | |
| Si8650Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.1 | 1.8 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 3.1 | 4.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 7.0 | 9.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.3 | 5.0 | |
| Si8651Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.5 | 2.4 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.7 | 4.1 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 6.6 | 9.2 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 4.0 | 6.0 | |
| Si8652Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 2.0 | 3.0 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.4 | 3.6 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 5.6 | 7.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 5.0 | 7.5 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 3. Electrical Characteristics (Continued) $(V_{DD1} = 3.3 V \pm 10\%$, $V_{DD2} = 3.3 V \pm 10\%$, $T_A = -40$ to 125 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|------|------|
| Si8660Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.5 | 5.3 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 8.8 | 12.3 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 3.7 | 5.6 | |
| Si8661Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 1.7 | 2.7 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.4 | 5.1 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 7.9 | 11.1 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 4.8 | 7.2 | |
| Si8662Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 2.2 | 3.3 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 3.0 | 4.5 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 7.5 | 10.5 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 5.6 | 8.4 | |
| Si8663Ax | | | | | | |
| V_{DD1} | | $V_I = 0(Ax)$ | — | 2.6 | 3.9 | mA |
| V_{DD2} | | $V_I = 0(Ax)$ | — | 2.6 | 3.9 | |
| V_{DD1} | | $V_I = 1(Ax)$ | — | 6.5 | 9.1 | |
| V_{DD2} | | $V_I = 1(Ax)$ | — | 6.5 | 9.1 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Si86xx

Table 3. Electrical Characteristics (Continued)

($V_{DD1} = 3.3 V \pm 10\%$, $V_{DD2} = 3.3 V \pm 10\%$, $T_A = -40$ to 125 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|--------|------------|------------|------|
| 1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs) | | | | | | |
| Si8610Ax V_{DD1} V_{DD2} | | | — — | 1.2 0.9 | 2.0 1.5 | mA |
| Si8620Ax V_{DD1} V_{DD2} | | | — — | 2.1 1.6 | 3.1 2.4 | mA |
| Si8621Ax V_{DD1} V_{DD2} | | | — — | 1.9 1.9 | 2.9 2.9 | mA |
| Si8630Ax V_{DD1} V_{DD2} | | | — — | 2.8 2.2 | 3.9 3.1 | mA |
| Si8631Ax V_{DD1} V_{DD2} | | | — — | 2.7 2.6 | 3.8 3.6 | mA |
| Si8640Ax V_{DD1} V_{DD2} | | | — — | 3.6 2.9 | 5.0 4.0 | mA |
| Si8641Ax V_{DD1} V_{DD2} | | | — — | 3.4 3.3 | 4.8 4.6 | mA |
| Si8642Ax V_{DD1} V_{DD2} | | | — — | 3.3 3.3 | 4.6 4.6 | mA |
| Si8650Ax V_{DD1} V_{DD2} | | | — — | 4.1 3.7 | 5.7 5.2 | mA |
| Si8651Ax V_{DD1} V_{DD2} | | | — — | 4.2 3.8 | 5.8 5.3 | mA |
| Si8652Ax V_{DD1} V_{DD2} | | | — — | 4.0 4.0 | 5.6 5.6 | mA |
| Si8660Ax V_{DD1} V_{DD2} | | | — — | 5.0 4.2 | 7.0 5.9 | mA |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately 50Ω, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 3. Electrical Characteristics (Continued) $(V_{DD1} = 3.3\text{ V} \pm 10\%, V_{DD2} = 3.3\text{ V} \pm 10\%, T_A = -40\text{ to }125\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Si8661Ax | | | | | | |
| V_{DD1} | | | — | 4.9 | 6.9 | mA |
| V_{DD2} | | | — | 4.6 | 6.4 | |
| Si8662Ax | | | | | | |
| V_{DD1} | | | — | 5.1 | 7.1 | mA |
| V_{DD2} | | | — | 4.7 | 6.6 | |
| Si8663Ax | | | | | | |
| V_{DD1} | | | — | 4.9 | 6.8 | mA |
| V_{DD2} | | | — | 4.9 | 6.8 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 3. Electrical Characteristics (Continued)

($V_{DD1} = 3.3\text{ V} \pm 10\%$, $V_{DD2} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------------|---|-----|-----|-----|-------------------|
| Timing Characteristics | | | | | | |
| All Models | | | | | | |
| Maximum Data Rate | | | 0 | — | 1 | Mbps |
| Minimum Pulse Width | | | — | — | 250 | ns |
| Propagation Delay | t_{PHL} , t_{PLH} | See Figure 2 | — | — | 35 | ns |
| Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | PWD | See Figure 2 | — | — | 25 | ns |
| Propagation Delay Skew ² | $t_{PSK(P-P)}$ | | — | — | 40 | ns |
| Channel-Channel Skew | t_{PSK} | | — | — | 35 | ns |
| Output Rise Time | t_r | $C_L = 15\text{ pF}$ See Figure 2 | — | 2.5 | 4.0 | ns |
| Output Fall Time | t_f | $C_L = 15\text{ pF}$ See Figure 2 | — | 2.5 | 4.0 | ns |
| Peak eye diagram jitter | $t_{JIT(PK)}$ | See Figure 8 | — | 350 | — | ps |
| Common Mode Transient Immunity | CMTI | $V_I = V_{DD}$ or 0 V $V_{CM} = 1500\text{ V}$ (see Figure 3) | 35 | 50 | — | kV/ μs |
| Enable to Data Valid | t_{en1} | See Figure 1 | — | 6.0 | 11 | ns |
| Enable to Data Tri-State | t_{en2} | See Figure 1 | — | 8.0 | 12 | ns |
| Start-Up Time ³ | t_{SU} | | — | 15 | 40 | μs |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 4. Electrical Characteristics $(V_{DD1} = 2.5\text{ V} \pm 5\%$, $V_{DD2} = 2.5\text{ V} \pm 5\%$, $T_A = -40$ to $125\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|-------------------------------|--------------------------|------|----------|---------------|
| VDD Undervoltage Threshold | VDDUV+ | V_{DD1} , V_{DD2} rising | 1.95 | 2.24 | 2.375 | V |
| VDD Undervoltage Threshold | VDDUV- | V_{DD1} , V_{DD2} falling | 1.88 | 2.16 | 2.325 | V |
| VDD Undervoltage Hysteresis | VDDHYS | | 50 | 70 | 95 | mV |
| Positive-Going Input Threshold | VT+ | All inputs rising | 1.4 | 1.67 | 1.9 | V |
| Negative-Going Input Threshold | VT- | All inputs falling | 1.0 | 1.23 | 1.4 | V |
| Input Hysteresis | V_{HYS} | | 0.38 | 0.44 | 0.50 | V |
| High Level Input Voltage | V_{IH} | | 2.0 | — | — | V |
| Low Level Input Voltage | V_{IL} | | — | — | 0.8 | V |
| High Level Output Voltage | V_{OH} | loh = -4 mA | $V_{DD1}, V_{DD2} - 0.4$ | 2.3 | — | V |
| Low Level Output Voltage | V_{OL} | lol = 4 mA | — | 0.2 | 0.4 | V |
| Input Leakage Current | I_L | | — | — | ± 10 | μA |
| Output Impedance ¹ | Z_O | | — | 50 | — | Ω |
| Enable Input High Current | I_{ENH} | $V_{ENx} = V_{IH}$ | — | 2.0 | — | μA |
| Enable Input Low Current | I_{ENL} | $V_{ENx} = V_{IL}$ | — | 2.0 | — | μA |
| DC Supply Current (All inputs 0 V or at supply) | | | | | | |
| Si8610Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.6 | 1.2 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 0.8 | 1.5 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 1.8 | 2.9 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 0.8 | 1.5 | |
| Si8620Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.8 | 1.4 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.4 | 2.2 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 3.3 | 5.3 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 1.4 | 2.2 | |
| Si8621Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.2 | 1.9 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 2.4 | 3.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 2.4 | 3.8 | |

Notes:

- The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
- $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
- Start-up time is the time period from the application of power to valid data at the output.

Si86xx

Table 4. Electrical Characteristics (Continued)

($V_{DD1} = 2.5\text{ V} \pm 5\%$, $V_{DD2} = 2.5\text{ V} \pm 5\%$, $T_A = -40\text{ to }125\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------------|-----|-----|-----|------|
| Si8630Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 0.9 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.9 | 3.0 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 4.6 | 7.4 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 1.9 | 3.0 | |
| Si8631Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.3 | 2.1 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.7 | 2.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 3.9 | 5.9 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.0 | 4.5 | |
| Si8640Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.0 | 1.6 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.4 | 3.8 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 6.1 | 9.2 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 2.5 | 4.0 | |
| Si8641Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.4 | 2.2 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.3 | 3.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 5.2 | 7.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.6 | 5.4 | |
| Si8642Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.8 | 2.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 1.8 | 2.9 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 4.4 | 6.6 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 4.4 | 6.6 | |
| Si8650Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.1 | 1.8 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 3.1 | 4.7 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 7.0 | 9.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.3 | 5.0 | |
| Si8651Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.5 | 2.4 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.7 | 4.1 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 6.6 | 9.2 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 4.0 | 6.0 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 4. Electrical Characteristics (Continued) $(V_{DD1} = 2.5\text{ V} \pm 5\%, V_{DD2} = 2.5\text{ V} \pm 5\%, T_A = -40\text{ to }125\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------------|-----|-----|------|------|
| Si8652Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 2.0 | 3.0 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.4 | 3.6 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 5.6 | 7.8 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 5.0 | 7.5 | |
| Si8660Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.2 | 1.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 3.5 | 5.3 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 8.8 | 12.3 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 3.7 | 5.6 | |
| Si8661Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 1.7 | 2.7 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 3.4 | 5.1 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 7.9 | 11.1 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 4.8 | 7.2 | |
| Si8662Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 2.2 | 3.3 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 3.0 | 4.5 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 7.5 | 10.5 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 5.6 | 8.4 | |
| Si8663Ax | | | | | | |
| V_{DD1} | | $V_I = 0(\text{Ax})$ | — | 2.6 | 3.9 | mA |
| V_{DD2} | | $V_I = 0(\text{Ax})$ | — | 2.6 | 3.9 | |
| V_{DD1} | | $V_I = 1(\text{Ax})$ | — | 6.5 | 9.1 | |
| V_{DD2} | | $V_I = 1(\text{Ax})$ | — | 6.5 | 9.1 | |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Si86xx

Table 4. Electrical Characteristics (Continued)

($V_{DD1} = 2.5\text{ V} \pm 5\%$, $V_{DD2} = 2.5\text{ V} \pm 5\%$, $T_A = -40\text{ to }125\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|--------|------------|------------|------|
| 1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs) | | | | | | |
| Si8610Ax V_{DD1} V_{DD2} | | | — — | 1.2 0.9 | 2.0 1.5 | mA |
| Si8620Ax V_{DD1} V_{DD2} | | | — — | 2.1 1.6 | 3.1 2.4 | mA |
| Si8621Ax V_{DD1} V_{DD2} | | | — — | 1.9 1.9 | 2.9 2.9 | mA |
| Si8630Ax V_{DD1} V_{DD2} | | | — — | 2.8 2.2 | 3.9 3.1 | mA |
| Si8631Ax V_{DD1} V_{DD2} | | | — — | 2.7 2.6 | 3.8 3.6 | mA |
| Si8640Ax V_{DD1} V_{DD2} | | | — — | 3.6 2.9 | 5.0 4.0 | mA |
| Si8641Ax V_{DD1} V_{DD2} | | | — — | 3.4 3.3 | 4.8 4.6 | mA |
| Si8642Ax V_{DD1} V_{DD2} | | | — — | 3.3 3.3 | 4.6 4.6 | mA |
| Si8650Ax V_{DD1} V_{DD2} | | | — — | 4.1 3.7 | 5.7 5.2 | mA |
| Si8651Ax V_{DD1} V_{DD2} | | | — — | 4.2 3.8 | 5.8 5.3 | mA |
| Si8652Ax V_{DD1} V_{DD2} | | | — — | 4.0 4.0 | 5.6 5.6 | mA |
| Si8660Ax V_{DD1} V_{DD2} | | | — — | 5.0 4.2 | 7.0 5.9 | mA |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 4. Electrical Characteristics (Continued) $(V_{DD1} = 2.5\text{ V} \pm 5\%, V_{DD2} = 2.5\text{ V} \pm 5\%, T_A = -40\text{ to }125\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|--------|------------|------------|------|
| Si8661Ax V_{DD1} V_{DD2} | | | — — | 4.9 4.6 | 6.9 6.4 | mA |
| Si8662Ax V_{DD1} V_{DD2} | | | — — | 5.1 4.7 | 7.1 6.6 | mA |
| Si8663Ax V_{DD1} V_{DD2} | | | — — | 4.9 4.9 | 6.8 6.8 | mA |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 4. Electrical Characteristics (Continued)

($V_{DD1} = 2.5\text{ V} \pm 5\%$, $V_{DD2} = 2.5\text{ V} \pm 5\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------------|---|-----|-----|-----|-------------------|
| Timing Characteristics | | | | | | |
| All Models | | | | | | |
| Maximum Data Rate | | | 0 | — | 1 | Mbps |
| Minimum Pulse Width | | | — | — | 250 | ns |
| Propagation Delay | t_{PHL} , t_{PLH} | See Figure 2 | — | — | 35 | ns |
| Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | PWD | See Figure 2 | — | — | 25 | ns |
| Propagation Delay Skew ² | $t_{PSK(P-P)}$ | | — | — | 40 | ns |
| Channel-Channel Skew | t_{PSK} | | — | — | 35 | ns |
| Output Rise Time | t_r | $C_L = 15\text{ pF}$ See Figure 2 | — | 2.5 | 4.0 | ns |
| Output Fall Time | t_f | $C_L = 15\text{ pF}$ See Figure 2 | — | 2.5 | 4.0 | ns |
| Peak Eye Diagram Jitter | $t_{JIT(PK)}$ | See Figure 8 | — | 350 | — | ps |
| Common Mode Transient Immunity | CMTI | $V_I = V_{DD}$ or 0 V $V_{CM} = 1500\text{ V}$ (see Figure 3) | 35 | 50 | — | kV/ μs |
| Enable to Data Valid | t_{en1} | See Figure 1 | — | 6.0 | 11 | ns |
| Enable to Data Tri-State | t_{en2} | See Figure 1 | — | 8.0 | 12 | ns |
| Startup Time ³ | t_{SU} | | — | 15 | 40 | μs |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. The nominal output impedance of an isolator driver channel is approximately $50\ \Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. Start-up time is the time period from the application of power to valid data at the output. | | | | | | |

Table 5. Regulatory Information*

| |
|---|
| CSA |
| The Si86xx is certified under CSA Component Acceptance Notice 5A, IEC61010-1 and IEC60950-1. For more details, see File 232873. |
| VDE |
| The Si86xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001. |
| UL |
| The Si86xx is certified under UL1577 component recognition program. For more details, see File E257455. |
| CQC |
| The Si86xx is certified under GB4943.1-2011. For more details, see File V2012CQC001041. |
| *Note: Regulatory Certifications apply to 2.5 kV _{RMS} rated devices which are production tested to 3.0 kV _{RMS} for 1 sec. For more information, see "8. Pin Descriptions (Si866x)" on page 38. |

Table 6. Insulation and Safety-Related Specifications

| Parameter | Symbol | Test Condition | Value | | | Unit |
|---|-----------------|----------------|------------------|------------------|------------------|------------------|
| | | | WB SOIC-16 | NB SOIC-16 | NB SOIC-8 | |
| Nominal Air Gap (Clearance) ¹ | L(IO1) | | 8.0 | 4.9 | 4.9 | mm |
| Nominal External Tracking (Creepage) ¹ | L(IO2) | | 8.0 | 4.01 | 4.01 | mm |
| Minimum Internal Gap (Internal Clearance) | | | 0.014 | 0.014 | 0.014 | mm |
| Tracking Resistance (Proof Tracking Index) | PTI | IEC60112 | 600 | 600 | 600 | V _{RMS} |
| Erosion Depth | ED | | 0.019 | 0.019 | 0.040 | mm |
| Resistance (Input-Output) ² | R _{IO} | | 10 ¹² | 10 ¹² | 10 ¹² | Ω |
| Capacitance (Input-Output) ² | C _{IO} | f = 1 MHz | 2.0 | 2.0 | 2.0 | pF |
| Input Capacitance ³ | C _I | | 4.0 | 4.0 | 4.0 | pF |

Notes:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and SOIC-8 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 and SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 (Pins 1-4 for the NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (Pins 5-8 for the NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 7. IEC 60664-1 (VDE 0844 Part 2) Ratings

| Parameter | Test Conditions | Specification | |
|-----------------------------|---|-------------------------|------------|
| | | NB SOIC-16 NB SOIC-8 | WB SOIC-16 |
| Basic Isolation Group | Material Group | I | I |
| Installation Classification | Rated Mains Voltages ≤ 150 V _{RMS} | I-IV | I-IV |
| | Rated Mains Voltages ≤ 300 V _{RMS} | I-III | I-IV |
| | Rated Mains Voltages ≤ 400 V _{RMS} | I-II | I-III |
| | Rated Mains Voltages ≤ 600 V _{RMS} | I-II | I-III |

Table 8. IEC 60747-5-2 Insulation Characteristics for Si86xxxx*

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|--|------------|--|----------------|-------------------|----------|
| | | | WB SOIC-16 | NB SOIC-16 SOIC-8 | |
| Maximum Working Insulation Voltage | V_{IORM} | | 1200 | 630 | Vpeak |
| Input to Output Test Voltage | V_{PR} | Method b1 ($V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC) | 2250 | 1182 | |
| Transient Overvoltage | V_{IOTM} | t = 60 sec | 6000 | 6000 | Vpeak |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | 2 | |
| Insulation Resistance at T_S , $V_{IO} = 500$ V | R_S | | $>10^9$ | $>10^9$ | Ω |

*Note: Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 9. IEC Safety Limiting Values¹

| Parameter | Symbol | Test Condition | Max | | | Unit |
|--|--------|--|------------|------------|-----------|------|
| | | | WB SOIC-16 | NB SOIC-16 | NB SOIC-8 | |
| Case Temperature | T_S | | 150 | 150 | 150 | °C |
| Safety Input, Output, or Supply Current | I_S | $\theta_{JA} = 100$ °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), 140 °C/W (NB SOIC-8), $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C | 220 | 215 | 160 | mA |
| Device Power Dissipation ² | P_D | | 415 | 415 | 150 | mW |

Notes:

1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 4, 5 and 6.
2. The Si86xx is tested with $VDD1 = VDD2 = 5.5$ V, $T_J = 150$ °C, $C_L = 15$ pF, input a 150 Mbps 50% duty cycle square wave.

Table 10. Thermal Characteristics

| Parameter | Symbol | WB SOIC-16 | NB SOIC-16 | NB SOIC-8 | Unit |
|---------------------------------------|---------------|------------|------------|-----------|-----------------------------|
| IC Junction-to-Air Thermal Resistance | θ_{JA} | 100 | 105 | 140 | $^{\circ}\text{C}/\text{W}$ |

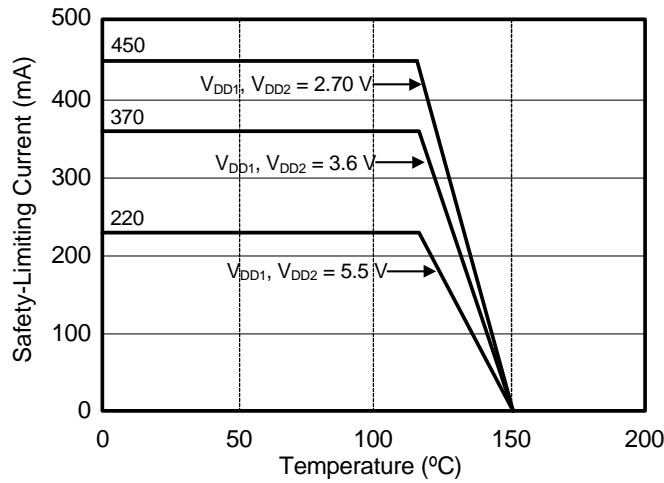


Figure 4. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

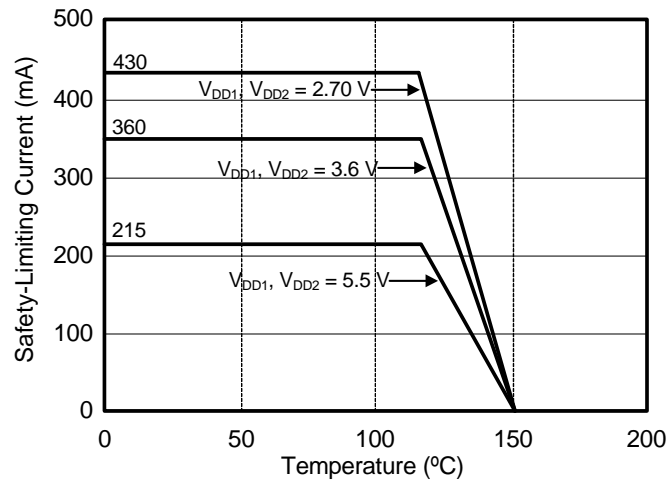


Figure 5. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

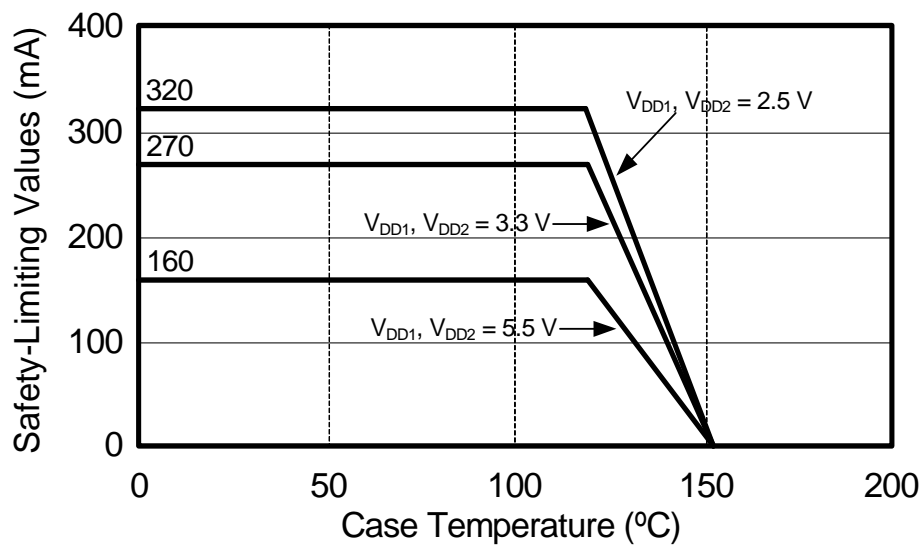


Figure 6. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 11. Absolute Maximum Ratings¹

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------------------|------|-----|----------------|-----------|
| Storage Temperature ² | T_{STG} | -65 | — | 150 | °C |
| Ambient Temperature Under Bias | T_A | -40 | — | 125 | °C |
| Junction Temperature | T_J | — | — | 150 | °C |
| Supply Voltage | V_{DD1}, V_{DD2} | -0.5 | — | 7.0 | V |
| Input Voltage | V_I | -0.5 | — | $V_{DD} + 0.5$ | V |
| Output Voltage | V_O | -0.5 | — | $V_{DD} + 0.5$ | V |
| Output Current Drive Channel (All devices unless otherwise stated) | I_O | — | — | 10 | mA |
| Output Current Drive Channel (All Si86xxxA-x-xx devices) | I_O | — | — | 22 | mA |
| Latchup Immunity ³ | | — | — | 100 | V/ns |
| Lead Solder Temperature (10 s) | | — | — | 260 | °C |
| Maximum Isolation (Input to Output) (1 sec) NB SOIC-16, SOIC-8 | | — | — | 4500 | V_{RMS} |
| Maximum Isolation (Input to Output) (1 sec) WB SOIC-16 | | — | — | 6500 | V_{RMS} |
| Notes: | | | | | |
| 1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. | | | | | |
| 2. VDE certifies storage temperature from -40 to 150 °C. | | | | | |
| 3. Latchup immunity specification is for slew rate applied across GND1 and GND2. | | | | | |

2. Functional Description

2.1. Theory of Operation

The operation of an Si86xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86xx channel is shown in Figure 7.

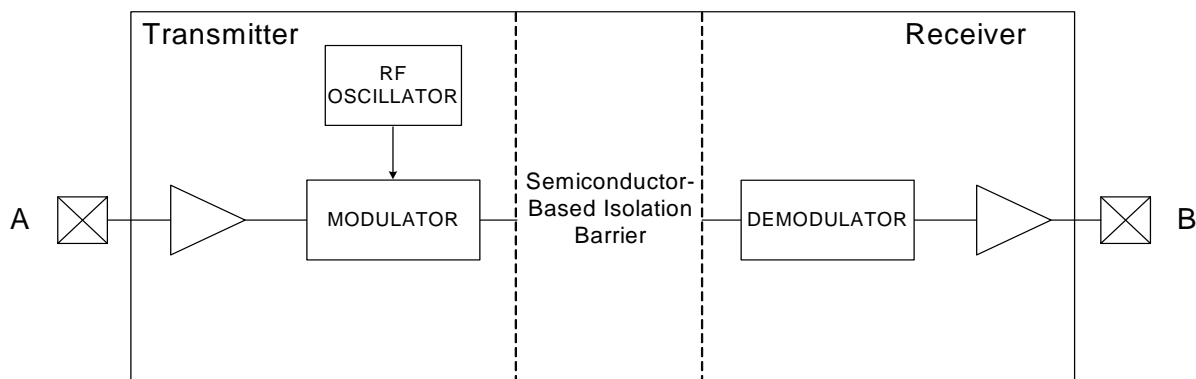


Figure 7. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 8 for more details.

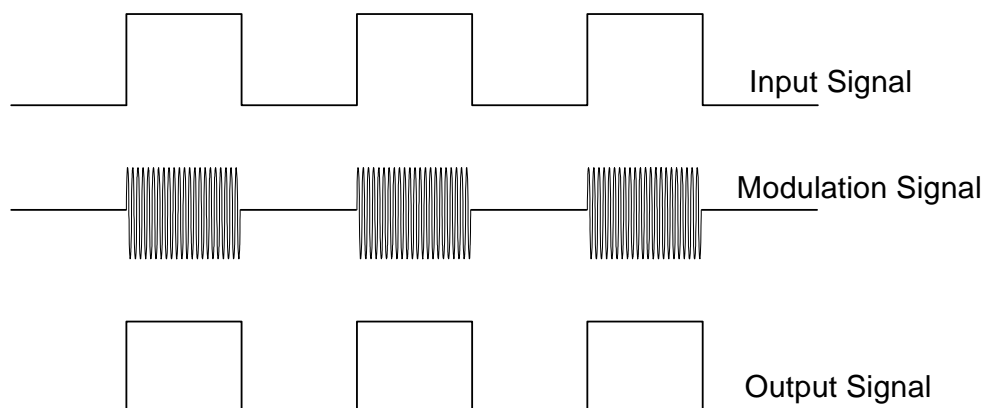


Figure 8. Modulation Scheme

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 9, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 12 to determine outputs when power supply (VDD) is not present. Additionally, refer to Table 13 for logic conditions when enable pins are used.

Table 12. Si86xx Logic Operation

| V _I Input ^{1,2} | EN Input ^{1,2,3,4} | VDDI State ^{1,5,6} | VDDO State ^{1,5,6} | V _O Output ^{1,2} | Comments |
|--|--------------------------------|--------------------------------|--------------------------------|--------------------------------------|--|
| H | H or NC | P | P | H | Enabled, normal operation. |
| L | H or NC | P | P | L | |
| X ⁷ | L | P | P | Hi-Z ⁸ | Disabled. |
| X ⁷ | H or NC | UP | P | L | Upon transition of VDDI from unpowered to powered, V _O returns to the same state as V _I in less than 1 μs. |
| X ⁷ | L | UP | P | Hi-Z ⁸ | Disabled. |
| X ⁷ | X ⁷ | P | UP | Undetermined | Upon transition of VDDO from unpowered to powered, V _O returns to the same state as V _I within 1 μs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V _O returns to Hi-Z within 1 μs if EN is L. |

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si86xx is operating in noisy environments.
4. No Connect (NC) replaces EN1 on some devices. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 2.5 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

Table 13. Enable Input Truth¹

| P/N | EN1 ^{1,2} | EN2 ^{1,2} | Operation |
|-----------|--------------------|--------------------|--|
| Si861x/2x | — | — | Outputs are enabled and follow input state. |
| Si8630 | — | H | Outputs B1, B2, B3 are enabled and follow input state. |
| | — | L | Outputs B1, B2, B3 are disabled and in high impedance state. ³ |
| Si8631 | H | X | Output A3 enabled and follows input state. |
| | L | X | Output A3 disabled and in high impedance state. ³ |
| | X | H | Outputs B1, B2 are enabled and follow input state. |
| | X | L | Outputs B1, B2 are disabled and in high impedance state. ³ |
| Si8640 | — | H | Outputs B1, B2, B3, B4 are enabled and follow the input state. |
| | — | L | Outputs B1, B2, B3, B4 are disabled and in high impedance state. ³ |
| Si8641 | H | X | Output A4 enabled and follows the input state. |
| | L | X | Output A4 disabled and in high impedance state. ³ |
| | X | H | Outputs B1, B2, B3 are enabled and follow the input state. |
| | X | L | Outputs B1, B2, B3 are disabled and in high impedance state. ³ |
| Si8642 | H | X | Outputs A3 and A4 are enabled and follow the input state. |
| | L | X | Outputs A3 and A4 are disabled and in high impedance state. ³ |
| | X | H | Outputs B1 and B2 are enabled and follow the input state. |
| | X | L | Outputs B1 and B2 are disabled and in high impedance state. ³ |
| Si8650 | — | H | Outputs B1, B2, B3, B4, B5 are enabled and follow input state. |
| | — | L | Outputs B1, B2, B3, B4, B5 are disabled and Logic Low or in high impedance state. ³ |
| Si8651 | H | X | Output A5 enabled and follow input state. |
| | L | X | Output A5 disabled and in high impedance state. ³ |
| | X | H | Outputs B1, B2, B3, B4 are enabled and follow input state. |
| | X | L | Outputs B1, B2, B3, B4 are disabled and in high impedance state. ³ |
| Si8652 | H | X | Outputs A4 and A5 are enabled and follow input state. |
| | L | X | Outputs A4 and A5 are disabled and in high impedance state. ³ |
| | X | H | Outputs B1, B2, B3 are enabled and follow input state. |
| | X | L | Outputs B1, B2, B3 are disabled and in high impedance state. ³ |
| Si866x | — | — | Outputs are enabled and follow input state. |

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 2 μ A current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si86xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO-)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

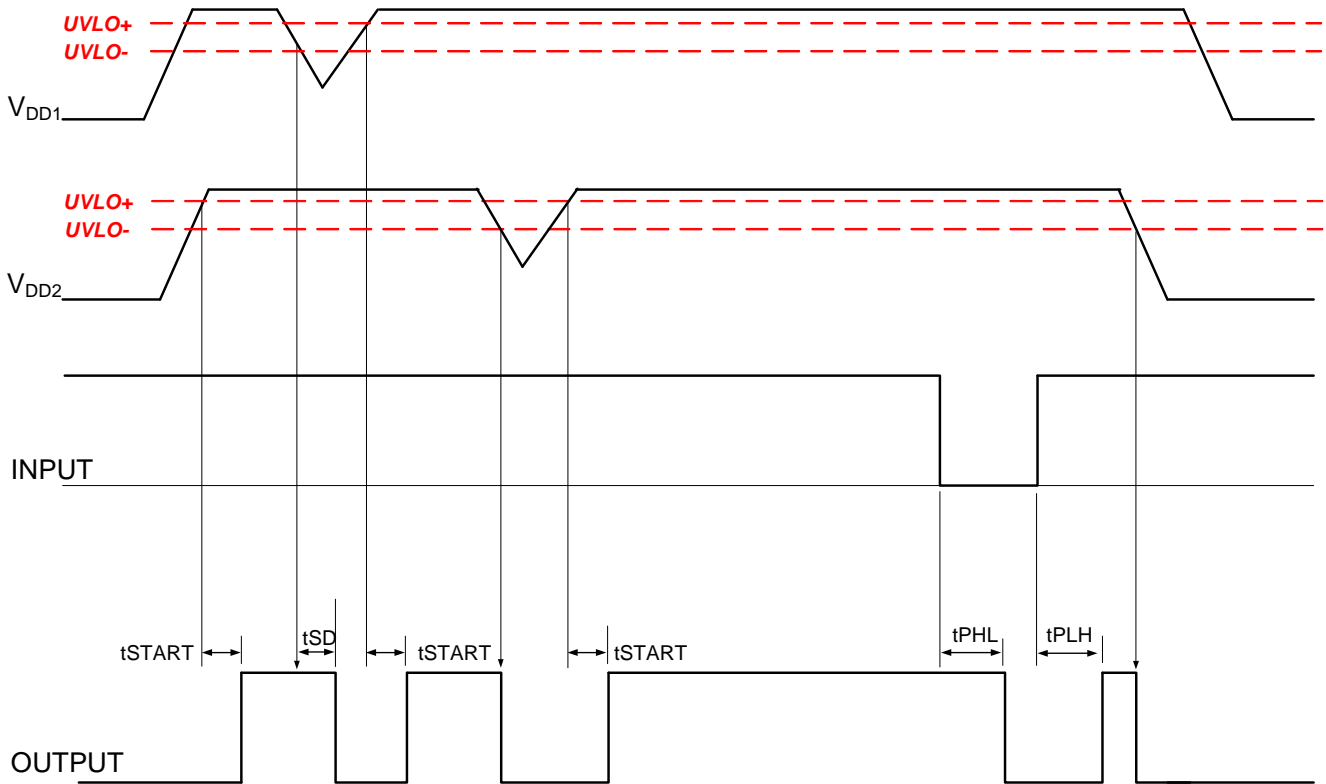


Figure 9. Device Behavior during Normal Operation

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with $>30 V_{AC}$) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with $<30 V_{AC}$) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5 on page 23 and Table 6 on page 24 detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

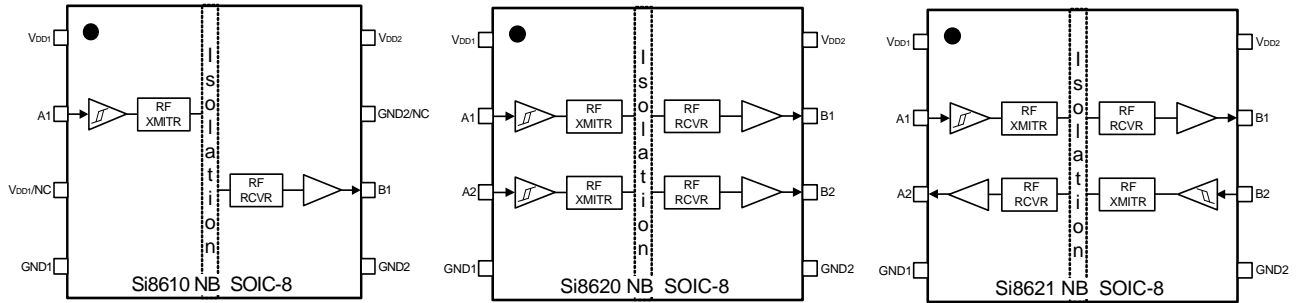
The Si86xx family requires a $0.1 \mu\text{F}$ bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors ($50\text{--}300 \Omega$) in series with the inputs and outputs if the system is excessively noisy.

3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50Ω , $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

Si86xx

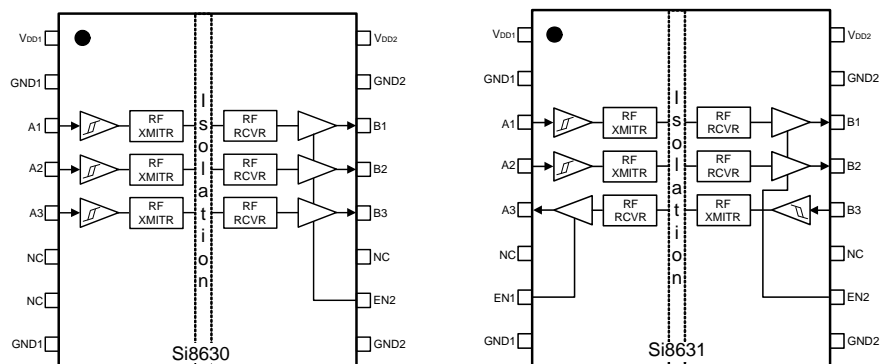
4. Pin Descriptions (Si861x/2x Narrow Body SOIC-8)



| Name | SOIC-8 Pin# Si861x | SOIC-8 Pin# Si862x | Type | Description |
|-----------------------|-----------------------|-----------------------|-------------|---------------------------------|
| V _{DD1} /NC* | 1,3 | 1 | Supply | Side 1 power supply. |
| GND1 | 4 | 4 | Ground | Side 1 ground. |
| A1 | 2 | 2 | Digital I/O | Side 1 digital input or output. |
| A2 | NA | 3 | Digital I/O | Side 1 digital input or output. |
| B1 | 6 | 7 | Digital I/O | Side 2 digital input or output. |
| B2 | NA | 6 | Digital I/O | Side 2 digital input or output. |
| V _{DD2} | 8 | 8 | Supply | Side 2 power supply. |
| GND2/NC* | 5,7 | 5 | Ground | Side 2 ground. |

***Note:** No connect. These pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

5. Pin Descriptions (Si863x)

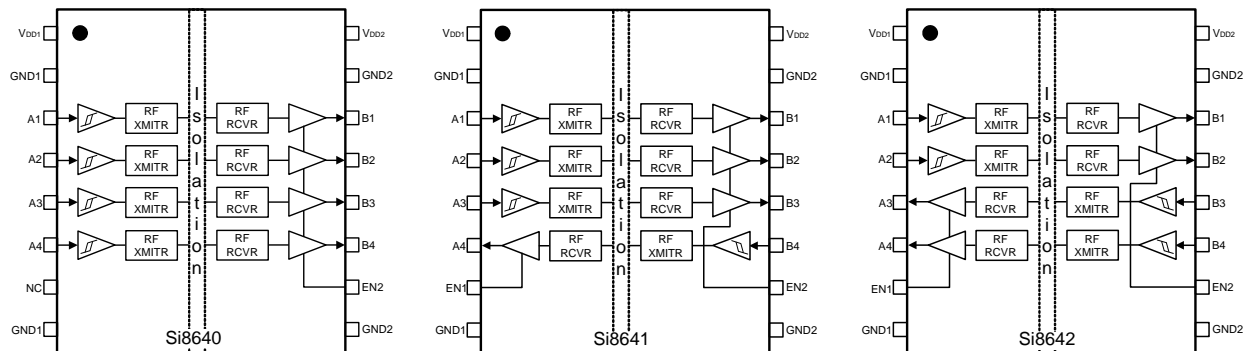


| Name | SOIC-16 Pin# | Type | Description |
|---------------------|-----------------|----------------|---|
| V _{DD1} | 1 | Supply | Side 1 power supply. |
| GND1 | 2 ¹ | Ground | Side 1 ground. |
| A1 | 3 | Digital Input | Side 1 digital input. |
| A2 | 4 | Digital Input | Side 1 digital input. |
| A3 | 5 | Digital I/O | Side 1 digital input or output. |
| NC | 6 | NA | No Connect. |
| EN1/NC ² | 7 | Digital Input | Side 1 active high enable. NC on Si8630 |
| GND1 | 8 ¹ | Ground | Side 1 ground. |
| GND2 | 9 ¹ | Ground | Side 2 ground. |
| EN2 | 10 | Digital Input | Side 2 active high enable. |
| NC | 11 | NA | No Connect. |
| B3 | 12 | Digital I/O | Side 2 digital input or output. |
| B2 | 13 | Digital Output | Side 2 digital output. |
| B1 | 14 | Digital Output | Side 2 digital output. |
| GND2 | 15 ¹ | Ground | Side 2 ground. |
| V _{DD2} | 16 | Supply | Side 2 power supply. |

Notes:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

6. Pin Descriptions (Si864x)

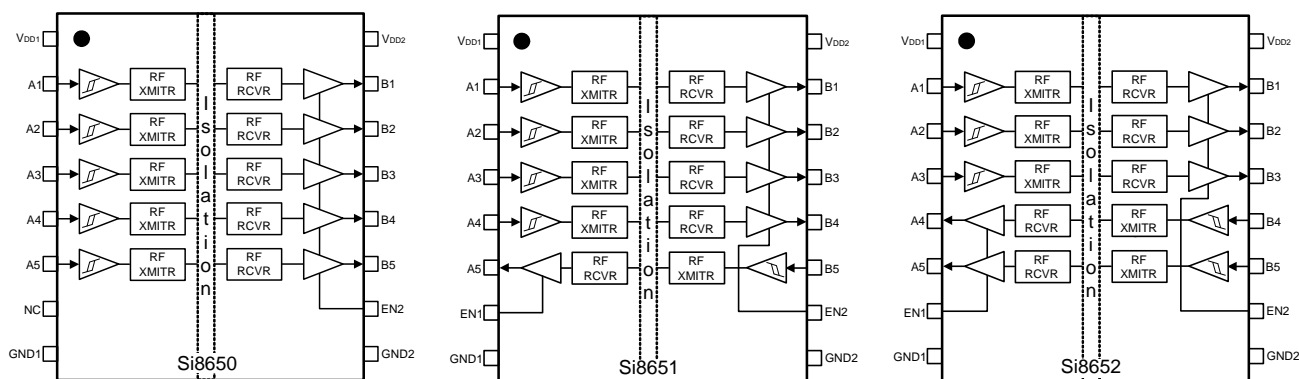


| Name | SOIC-16 Pin# | Type | Description |
|---------------------|-----------------|----------------|--|
| V _{DD1} | 1 | Supply | Side 1 power supply. |
| GND1 | 2 ¹ | Ground | Side 1 ground. |
| A1 | 3 | Digital Input | Side 1 digital input. |
| A2 | 4 | Digital Input | Side 1 digital input. |
| A3 | 5 | Digital I/O | Side 1 digital input or output. |
| A4 | 6 | Digital I/O | Side 1 digital input or output. |
| EN1/NC ² | 7 | Digital Input | Side 1 active high enable. NC on Si8640. |
| GND1 | 8 ¹ | Ground | Side 1 ground. |
| GND2 | 9 ¹ | Ground | Side 2 ground. |
| EN2 | 10 | Digital Input | Side 2 active high enable. |
| B4 | 11 | Digital I/O | Side 2 digital input or output. |
| B3 | 12 | Digital I/O | Side 2 digital input or output. |
| B2 | 13 | Digital Output | Side 2 digital output. |
| B1 | 14 | Digital Output | Side 2 digital output. |
| GND2 | 15 ¹ | Ground | Side 2 ground. |
| V _{DD2} | 16 | Supply | Side 2 power supply. |

Notes:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

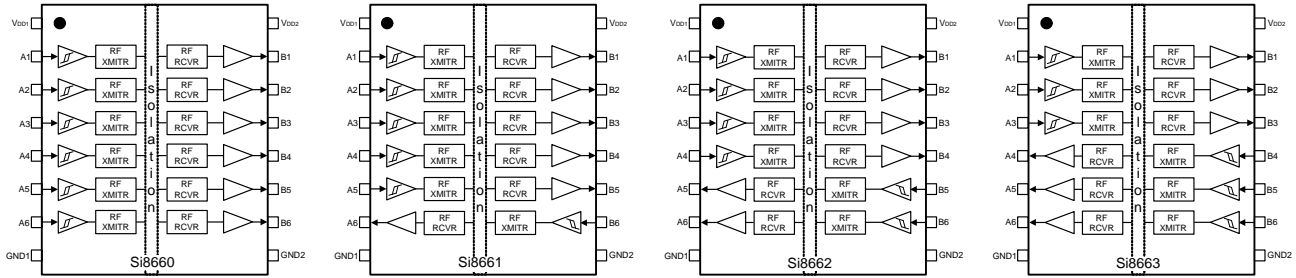
7. Pin Descriptions (Si8650/51/52)



| Name | SOIC-16 Pin# | Type | Description |
|------------------|--------------|----------------|--|
| V _{DD1} | 1 | Supply | Side 1 power supply. |
| A1 | 2 | Digital Input | Side 1 digital input. |
| A2 | 3 | Digital Input | Side 1 digital input. |
| A3 | 4 | Digital Input | Side 1 digital input. |
| A4 | 5 | Digital I/O | Side 1 digital input or output. |
| A5 | 6 | Digital I/O | Side 1 digital input or output. |
| EN1/NC* | 7 | Digital Input | Side 1 active high enable. NC on Si8650. |
| GND1 | 8 | Ground | Side 1 ground. |
| GND2 | 9 | Ground | Side 2 ground. |
| EN2 | 10 | Digital Input | Side 2 active high enable. |
| B5 | 11 | Digital I/O | Side 2 digital input or output. |
| B4 | 12 | Digital I/O | Side 2 digital input or output. |
| B3 | 13 | Digital Output | Side 2 digital output. |
| B2 | 14 | Digital Output | Side 2 digital output. |
| B1 | 15 | Digital Output | Side 2 digital output. |
| V _{DD2} | 16 | Supply | Side 2 power supply. |

***Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

8. Pin Descriptions (Si866x)



| Name | SOIC-16 Pin# | Type | Description |
|------------------|--------------|----------------|---------------------------------|
| V _{DD1} | 1 | Supply | Side 1 power supply. |
| A1 | 2 | Digital Input | Side 1 digital input. |
| A2 | 3 | Digital Input | Side 1 digital input. |
| A3 | 4 | Digital Input | Side 1 digital input. |
| A4 | 5 | Digital I/O | Side 1 digital input or output. |
| A5 | 6 | Digital I/O | Side 1 digital input or output. |
| A6 | 7 | Digital I/O | Side 1 digital input or output. |
| GND1 | 8 | Ground | Side 1 ground. |
| GND2 | 9 | Ground | Side 2 ground. |
| B6 | 10 | Digital I/O | Side 2 digital input or output. |
| B5 | 11 | Digital I/O | Side 2 digital input or output. |
| B4 | 12 | Digital I/O | Side 2 digital input or output. |
| B3 | 13 | Digital Output | Side 2 digital output. |
| B2 | 14 | Digital Output | Side 2 digital output. |
| B1 | 15 | Digital Output | Side 2 digital output. |
| V _{DD2} | 16 | Supply | Side 2 power supply. |

9. Ordering Guide

Table 14. Ordering Guide for Valid OPNs^{1,2,3}

| Ordering Part Number (OPN) | Number of Inputs VDD1 Side | Number of Inputs VDD2 Side | Max Data Rate (Mbps) | Default Output State | Isolation Rating (kV) | Temp (°C) | Package |
|----------------------------|----------------------------|----------------------------|----------------------|----------------------|-----------------------|---------------|------------|
| Si8610AB-B-IS | 1 | 0 | 1 | Low | 2.5 | -40 to 125 °C | SOIC-8 |
| Si8620AB-B-IS | 2 | 0 | 1 | Low | 2.5 | -40 to 125 °C | SOIC-8 |
| Si8621AB-B-IS | 1 | 1 | 1 | Low | 2.5 | -40 to 125 °C | SOIC-8 |
| Si8630AB-B-IS | 3 | 0 | 1 | Low | 2.5 | -40 to 125 °C | WB SOIC-16 |
| Si8630AB-B-IS1 | 3 | 0 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8631AB-B-IS | 2 | 1 | 1 | Low | 2.5 | -40 to 125 °C | WB SOIC-16 |
| Si8631AB-B-IS1 | 2 | 1 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8640AB-B-IS1 | 4 | 0 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8640AB-B-IS | 4 | 0 | 1 | Low | 2.5 | -40 to 125 °C | WB SOIC-16 |
| Si8641AB-B-IS1 | 3 | 1 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8641AB-B-IS | 3 | 1 | 1 | Low | 2.5 | -40 to 125 °C | WB SOIC-16 |
| Si8642AB-B-IS1 | 2 | 2 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8642AB-B-IS | 2 | 2 | 1 | Low | 2.5 | -40 to 125 °C | WB SOIC-16 |
| Si8650AB-B-IS1 | 5 | 0 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8651AB-B-IS1 | 4 | 1 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8652AB-B-IS1 | 3 | 2 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8660AB-B-IS1 | 6 | 0 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8661AB-B-IS1 | 5 | 1 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8662AB-B-IS1 | 4 | 2 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |
| Si8663AB-B-IS1 | 3 | 3 | 1 | Low | 2.5 | -40 to 125 °C | NB SOIC-16 |

Notes:

- All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages.
Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.
Moisture sensitivity level is MSL2A for narrow-body SOIC-8 packages.
- All devices >1 kV_{RMS} are AEC-Q100 qualified.
- "Si" and "SI" are used interchangeably.

10. Package Outline: 16-Pin Wide Body SOIC

Figure 10 illustrates the package details for the Si86xx Digital Isolator. Table 15 lists the values for the dimensions shown in the illustration.

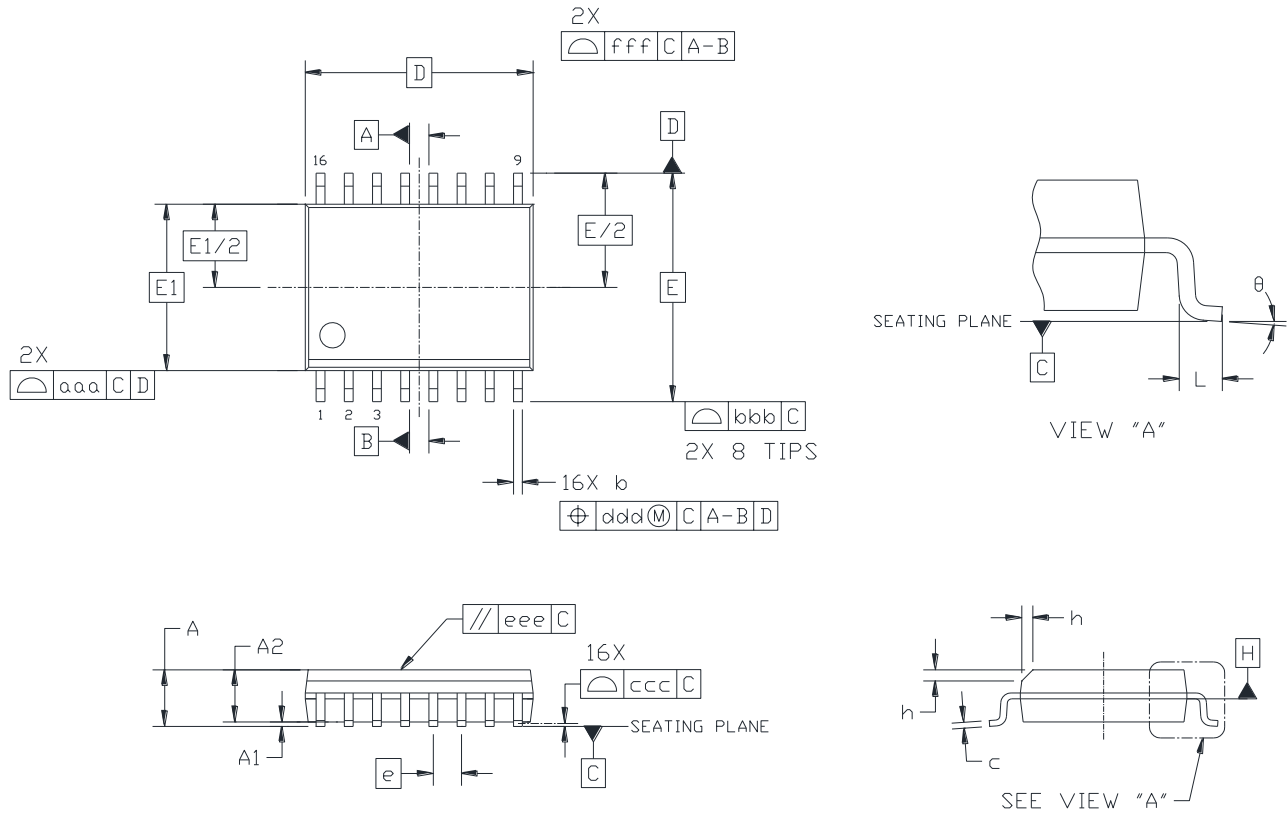


Figure 10. 16-Pin Wide Body SOIC

Table 15. Package Diagram Dimensions

| Dimension | Min | Max |
|-----------|-----------|------|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 10.30 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

11. Land Pattern: 16-Pin Wide-Body SOIC

Figure 11 illustrates the recommended land pattern details for the Si86xx in a 16-pin wide-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.

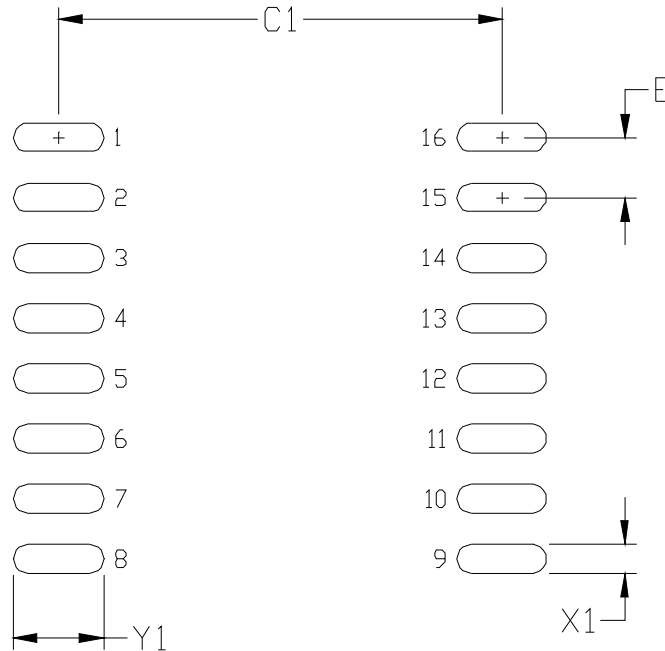


Figure 11. 16-Pin SOIC Land Pattern

Table 16. 16-Pin Wide Body SOIC Land Pattern Dimensions

| Dimension | Feature | (mm) |
|--|--------------------|------|
| C1 | Pad Column Spacing | 9.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.90 |
| Notes: | | |
| <ol style="list-style-type: none"> 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed. | | |

12. Package Outline: 16-Pin Narrow Body SOIC

Figure 12 illustrates the package details for the Si86xx in a 16-pin narrow-body SOIC (SO-16). Table 17 lists the values for the dimensions shown in the illustration.

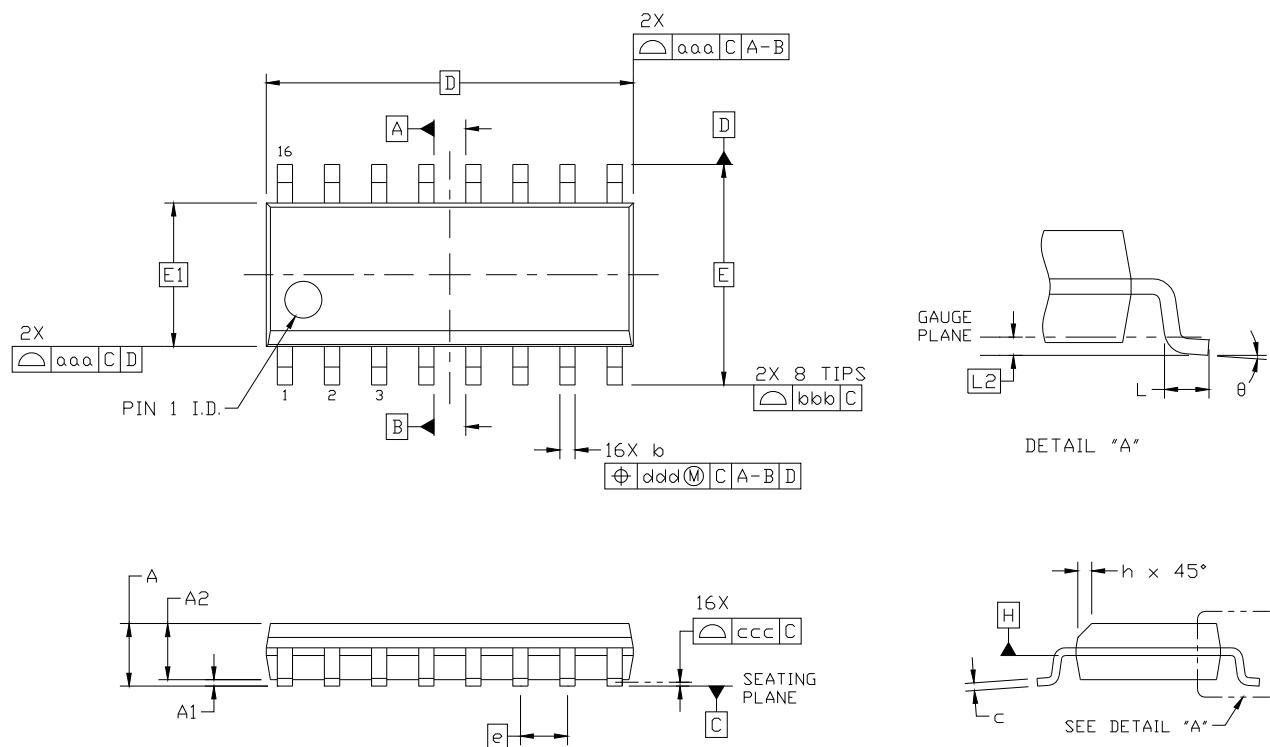


Figure 12. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 17. Package Diagram Dimensions

| Dimension | Min | Max |
|---|----------|------|
| A | — | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | — |
| b | 0.31 | 0.51 |
| c | 0.17 | 0.25 |
| D | 9.90 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |
| h | 0.25 | 0.50 |
| θ | 0° | 8° |
| aaa | 0.10 | |
| bbb | 0.20 | |
| ccc | 0.10 | |
| ddd | 0.25 | |
| Notes: | | |
| <ol style="list-style-type: none"> All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and Tolerancing per ANSI Y14.5M-1994. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | |

13. Land Pattern: 16-Pin Narrow Body SOIC

Figure 13 illustrates the recommended land pattern details for the Si86xx in a 16-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

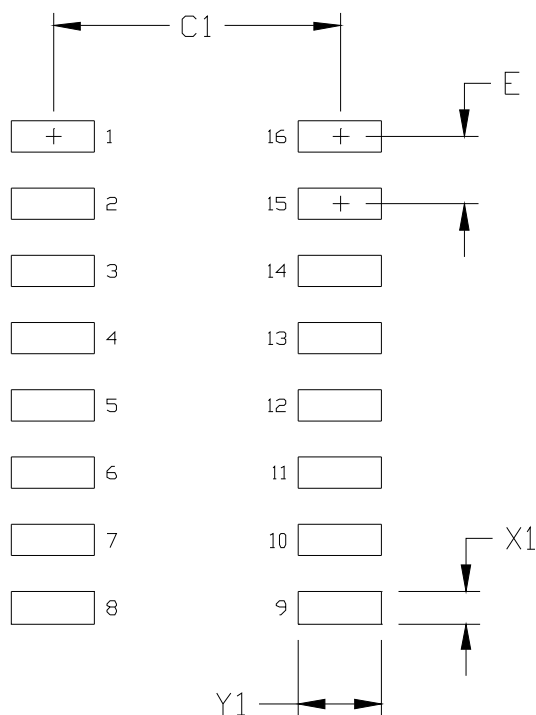


Figure 13. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 18. 16-Pin Narrow Body SOIC Land Pattern Dimensions

| Dimension | Feature | (mm) |
|-----------|--------------------|------|
| C1 | Pad Column Spacing | 5.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.55 |

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

14. Package Outline: 8-Pin Narrow Body SOIC

Figure 14 illustrates the package details for the Si86xx. Table 19 lists the values for the dimensions shown in the illustration.

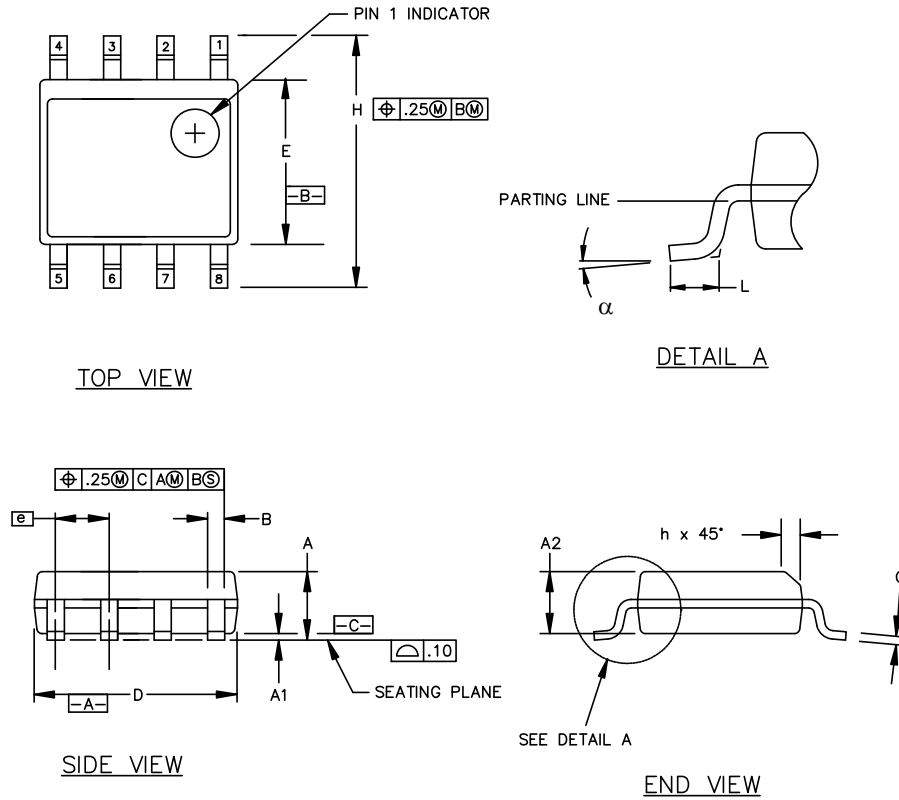


Figure 14. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 19. Package Diagram Dimensions

| Symbol | Millimeters | |
|----------|-------------|----------|
| | Min | Max |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

15. Land Pattern: 8-Pin Narrow Body SOIC

Figure 15 illustrates the recommended land pattern details for the Si86xx in an 8-pin narrow-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

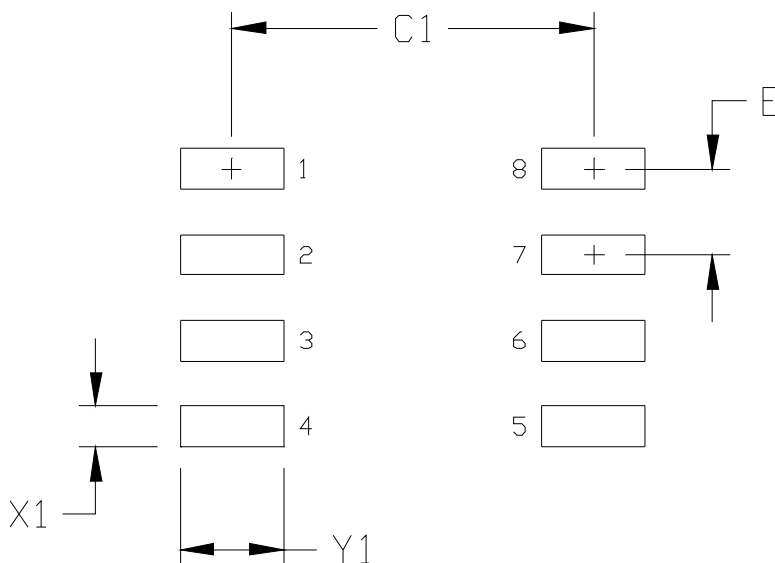


Figure 15. PCB Land Pattern: 8-Pin Narrow Body SOIC

Table 20. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

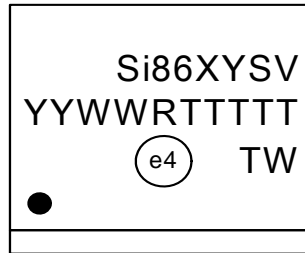
| Dimension | Feature | (mm) |
|-----------|--------------------|------|
| C1 | Pad Column Spacing | 5.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.55 |

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

16. Top Markings

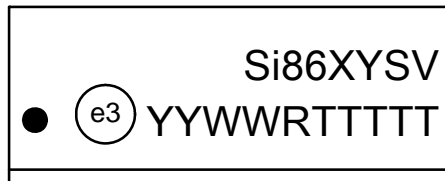
16.1. Top Marking (16-Pin Wide Body SOIC)



16.2. Top Marking Explanation (16-Pin Wide Body SOIC)

| | | |
|------------------------|--|--|
| Line 1 Marking: | Base Part Number Ordering Options (See Ordering Guide for more information). | Si86 = Isolator product series XY = Channel Configuration X = # of data channels (5, 4, 3, 2, 1) Y = # of reverse channels (2, 1, 0) S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV |
| | Line 2 Marking: YY = Year WW = Workweek RTTTTT = Mfg Code | Assigned by assembly subcontractor. Corresponds to the year and work week of the mold date. Manufacturing code from assembly house "R" indicates revision |
| Line 3 Marking: | Circle = 1.7 mm Diameter (Center-Justified) | "e4" Pb-free symbol |
| | Country of Origin ISO Code Abbreviation | TW = Taiwan |

16.3. Top Marking (16-Pin Narrow Body SOIC)

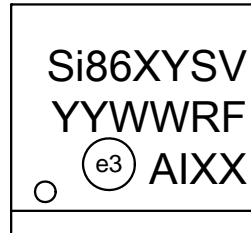


16.4. Top Marking Explanation (16-Pin Narrow Body SOIC)

| | | |
|------------------------|--|--|
| Line 1 Marking: | Base Part Number Ordering Options (See Ordering Guide for more information). | Si86 = Isolator product series XY = Channel Configuration X = # of data channels (5, 4, 3, 2, 1) Y = # of reverse channels (2, 1, 0) S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV |
| Line 2 Marking: | Circle = 1.2 mm Diameter | "e3" Pb-Free Symbol |
| | YY = Year WW = Work Week | Assigned by the assembly subcontractor. Corresponds to the year and work week of the mold date. |
| | RTTTTT = Mfg Code | Manufacturing code from assembly house "R" indicates revision |

Si86xx

16.5. Top Marking (8-Pin Narrow Body SOIC)



16.6. Top Marking Explanation (8-Pin Narrow Body SOIC)

| | | |
|------------------------|--|--|
| Line 1 Marking: | Base Part Number Ordering Options (See Ordering Guide for more information). | Si86 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0) S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV |
| Line 2 Marking: | YY = Year WW = Workweek R = Product (OPN) Revision F = Wafer Fab | Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date. |
| Line 3 Marking: | Circle = 1.1 mm Diameter Left-Justified A = Assembly Site I = Internal Code XX = Serial Lot Number | "e3" Pb-Free Symbol. First two characters of the manufacturing code. Last four characters of the manufacturing code. |

NOTES:

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