Low Voltage 2.5V/3.3V Differential ECL/ PECL/HSTL Fanout Buffer

MC100ES6210

NRND

DATA SHEET

NRND – Not Recommend for New Designs

Product Discontinuance Notice – Last Time Buy Expires on (12/23/2013)

The MC100ES6210 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6210 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low clock skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

LOW VOLTAGE DUAL 1:5 DIFFERENTIAL PECL/ECL/HSTL CLOCK FANOUT BUFFER

Features

- Dual 1:5 differential clock distribution
- 30 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, –3.3V, 2.5V or –2.5V supply
- Standard 32 lead LQFP and VFQFN packages
- Industrial temperature range
- Pin and function compatible to the MC100EP210
- 32-lead Pb-free Package

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

K SUFFIX
32-LEAD VFQFN PACKAGE
Pb-FREE PACKAGE

Functional Description

The MC100ES6210 is designed for low skew clock distribution systems and supports clock frequencies up to 3GHz. The device consists of two independent 1:5 clock fanout buffers. The input signal of each fanout buffer is distributed to five identical, differential ECL/ PECL outputs. Both CLKA and CLKB inputs can be driven by ECL/PECL compatible signals.

If V_{BB} is connected to the CLKA or CLKB input and bypassed to GND by a 10nF capacitor, the MC100ES6210 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6210 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6210 supports positive (PECL) and negative (ECL) supplies. The is function and pin compatible to the MC100EP210.

ORDERING INFORMATION

Device	Package
MC100ES6210AC	LQFP-32 (Pb-Free)
MC100ES6210ACR2	LQFP-32 (Pb-Free)
MC100ES6210KLF	VFQFN-32 (Pb-Free)

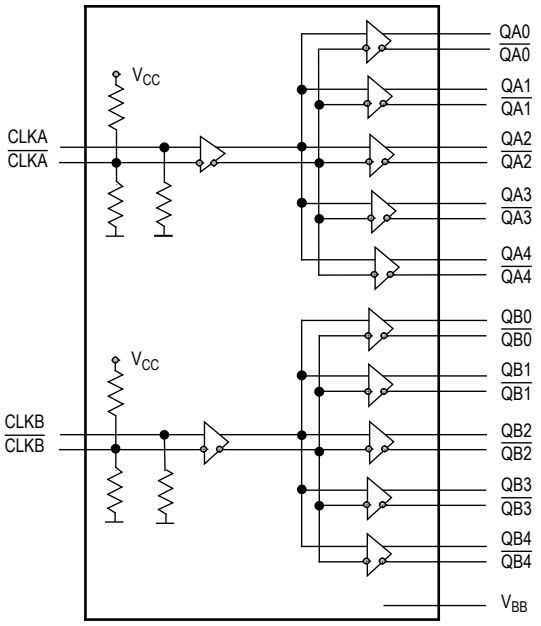


Figure 1. MC100ES6210 Logic Diagram

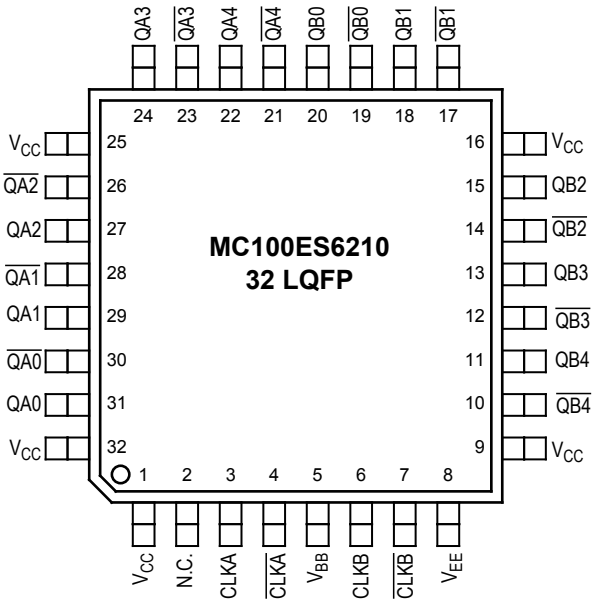


Figure 2. 32-Lead LQFP Package Pinout (Top View)

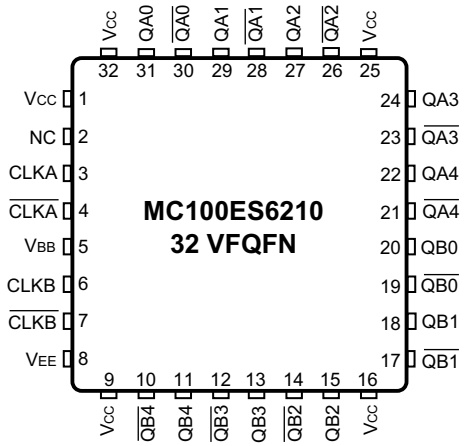


Figure 3. 32-Lead VFQFN Package Pinout (Top View)

Figure 3. 32-Lead VFQFN Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input (fanout buffer A)
CLKB, $\overline{\text{CLKB}}$	Input	ECL/PECL	Differential reference clock signal input (fanout buffer B)
QA[0-4], $\overline{\text{QA[0-4]}}$	Output	ECL/PECL	Differential clock outputs (fanout buffer A)
QB[0-4], $\overline{\text{QB[0-4]}}$	Output	ECL/PECL	Differential clock outputs (fanout buffer B)
V_{EE}(1)	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC})

Table 2. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} - 2$[1]		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)				V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient 32 LQFP					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
	Thermal Resistance Junction to Ambient 32 VFQFN		53.3		°C/W	0 meters per second
			46.6		°C/W	1 meters per second
			41.8		°C/W	2.5 meters per second
θ_{JC}	Thermal Resistance Junction to Case 32 LQFP		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years			110	°C	

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6210 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6210 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics (V_{CC} = 2.5V ± 5% or V_{CC} = 3.3V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	1.0		$V_{CC} - 0.3$	V	Differential operation
I_{IN}	Input Current[1]			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL Clock Outputs (QA0-4, $\overline{\text{QA0-4}}$, QB0-4, $\overline{\text{QB0-4}}$)						
V_{OH}	Output High Voltage	$V_{CC} - 1.2$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	I_{OH} = –30 mA[3]
V_{OL}	Output Low Voltage V_{CC} = 3.3V±5%	$V_{CC} - 1.9$	$V_{CC} - 1.705$	$V_{CC} - 1.5$	V	I_{OL} = –5 mA[3]
	V_{CC} = 2.5V±5%	$V_{CC} - 1.9$	$V_{CC} - 1.705$	$V_{CC} - 1.3$		
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current		60	100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.14$	V	I_{BB} = 0.2 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Equivalent to a termination of 50 Ω to V_{TT}.

Table 5. ECL DC Characteristics (V_{EE} = –2.5V ± 5% or V_{EE} = –3.3V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL Clock Outputs (QA0–4, $\overline{\text{QA0–4}}$, QB0–4, $\overline{\text{QB0–4}}$)						
V_{OH}	Output High Voltage	–1.2	–1.005	–0.7	V	I_{OH} = –30 mA[3]
V_{OL}	Output Low Voltage V_{CC} = 3.3V ±5% V_{CC} = 2.5V ±5%	–1.9 –1.9	–1.705 –1.705	–1.5 –1.3	V	I_{OL} = –5 mA[3]
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current		60	100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	–1.38	–1.26	–1.14	V	I_{BB} = 0.2 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Equivalent to a termination of 50 Ω to V_{TT}.

Table 6. AC Characteristics (ECL: V_{EE} = –3.3V ± 5% or V_{EE} = –2.5V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1] [2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[3] (peak-to-peak)	0.3	0.3	1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[4] PECL ECL	 1.2 V_{EE} + 1.2		 V_{CC} – 0.3 –0.3V	 V V	
ECL Clock Outputs (Qx0–4, $\overline{Qx0–4}$)						
f_{CLK}	Input Frequency	0		3000	MHz	Differential
t_{PD}	Propagation Delay CLKA to QAx or CLKB to QBx	175	260	350	ps	Differential
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 1.1GHz f_O < 2.5GHz f_O < 3.0GHz	 0.45 0.35 0.20	 0.70 0.55 0.35		 V V V	
$t_{sk(O)}$	Output-to-Output Skew (per bank)		13	30	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			175	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1	ps	
t_{jit}	Buffer Additive Phase Jitter, RMS 3.3V±5% 2.5V±5%			0.45 0.96	ps ps	
$t_{SK(P)}$	Output Pulse Skew[5]			50	ps	
DC_Q	Output Duty Cycle f_{REF} < 0.1GHz f_{REF} < 1.0GHz	49.5 45.0	50 50	50.5 55.0	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	30		250	ps	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
3. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
5. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

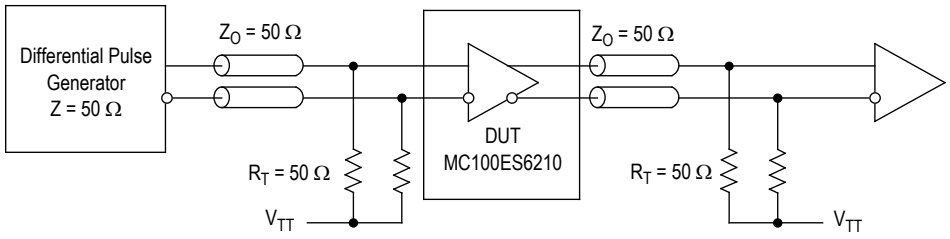
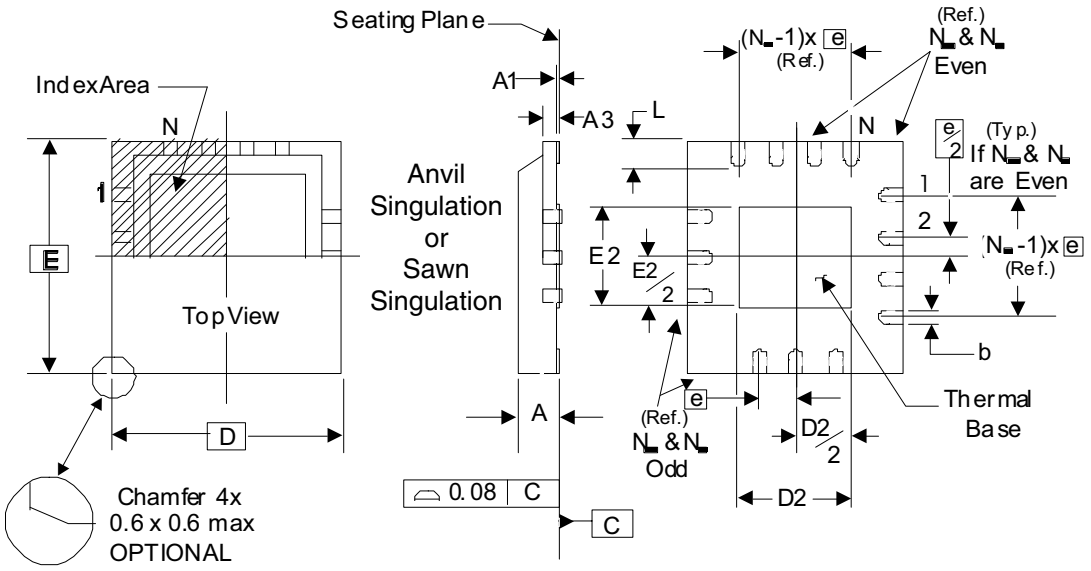


Figure 4. MC100ES6210 AC Test Reference

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN



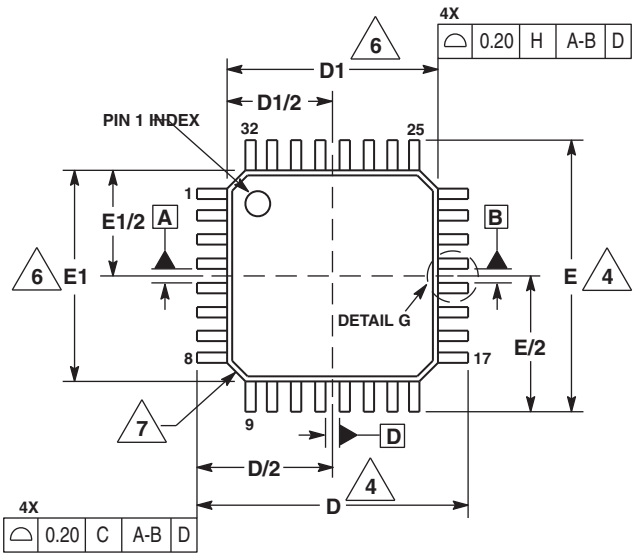
NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 7 below.

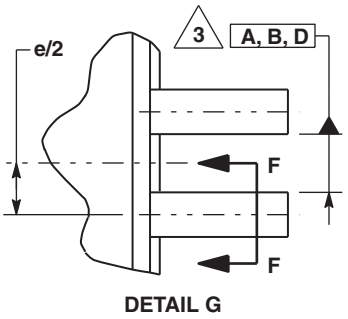
Table 7. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

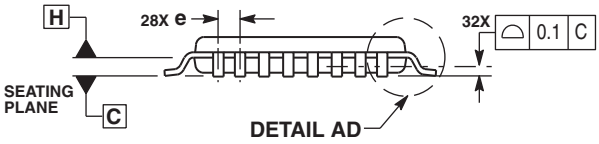
PACKAGE DIMENSIONS



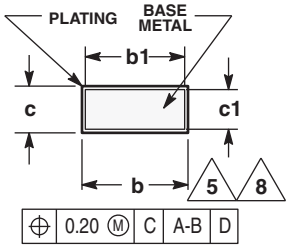


DETAIL G

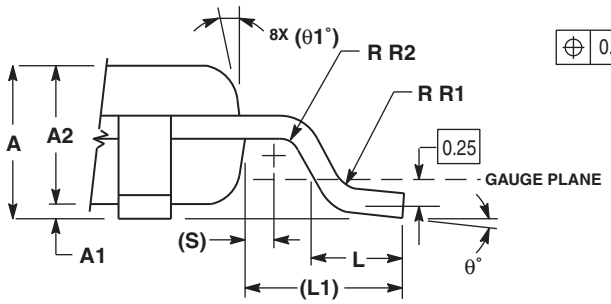
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.



DETAIL AD



SECTION F-F



DETAIL AD

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
7		1	NRND – Not Recommend for New Designs	12/19/2012
6		1	Product Discontinuance Notice – Last Time Buy Expires on (12/23/2013)	2/5/2013

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