

## Quick Start Guide for Testing the **AD9250/AD6673** Analog-to-Digital Converters (ADCs) Evaluation Boards Using the **HSC-ADC-EVALDZ** FPGA-Based Capture Board

### FEATURES

Evaluation boards for the **AD9250/AD6673** high speed analog-to-digital converters (ADCs) using the **HSC-ADC-EVALDZ** capture board

### EQUIPMENT NEEDED

An analog signal source and antialiasing filter

An analog clock source

A PC with a USB 2.0 port, recommended (USB 1.1-compatible)

The **AD9250** or the **AD6673** ADC evaluation board

The **HSC-ADC-EVALDZ** FPGA-based data capture board

### DOCUMENTS NEEDED

**AD9250** data sheet

**AD6673** data sheet

**AN-905** Application Note, *VisualAnalog Converter Evaluation Tool User Manual* (Analog Devices, Inc., 2007)

High Speed Converter Division, **AN-878** Application Note, *High Speed ADC SPI Control Software User Manual* (Analog Devices, 2006–2007)

High Speed Converter Division, **AN-877** Application Note, *Interfacing to High Speed ADCs via SPI* (Analog Devices, 2005–2007)

### SOFTWARE NEEDED

VisualAnalog

SPIController

### GENERAL DESCRIPTION

This user guide describes the **AD9250/AD6673** evaluation boards that can be used to evaluate Analog Devices, Inc., high speed **AD9250**-250, **AD9250**-170, or the **AD6673**-250 ADCs.

Full performance details are provided in the **AD9250/AD6673** data sheets and should be consulted in conjunction with this user guide. All documents and software are available at [www.analog.com/fifo](http://www.analog.com/fifo). For more information, email [highspeed.converters@analog.com](mailto:highspeed.converters@analog.com).

### EVALUATION BOARD CONNECTION DIAGRAM

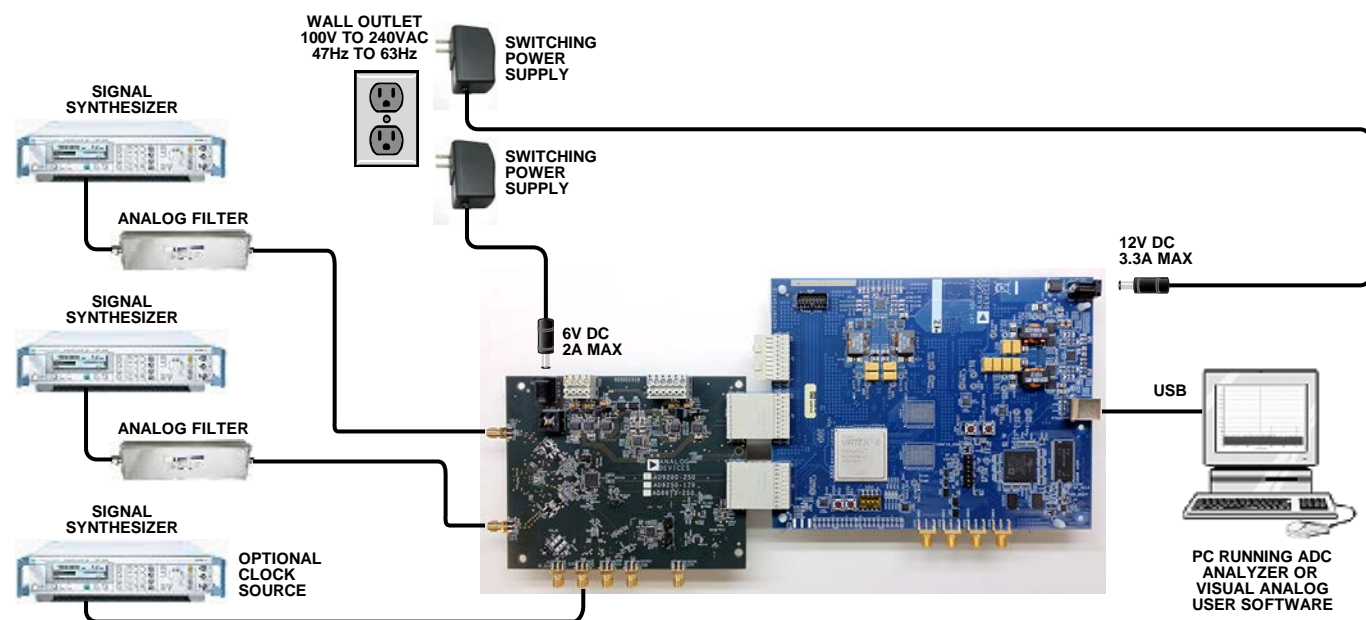


Figure 1.

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REVISION HISTORY

11/12—Revision 0: Initial Version

## EVALUATION BOARD SOFTWARE/HARDWARE QUICK START PROCEDURES

### INSTALLING THE SOFTWARE

To install the software, go to [www.analog.com/fifo](http://www.analog.com/fifo), and download and install the following:

- VisualAnalog, Rev 1.9.20.21 or later.
- SPI Control Software, Rev 1.0.91.3 or later.

### SETTING UP THE HARDWARE AND THE SOFTWARE

1. Connect the [AD9250](#) or the [AD6673](#) evaluation board and the [HSC-ADC-EVALDZ](#) board together, as shown in Figure 1.
2. Connect one 6 V, 2 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the [AD9250](#) or the [AD6673](#) board. Ensure that the 6 V power supply is used.
3. Connect one 12 V, 3.3 A switching power supply (such as the V-Infinity ETSA120330UDC-P5P-SZ supplied) to the [HSC-ADC-EVALDZ](#) board. Ensure that a 12 V power supply is used.
4. Connect the [HSC-ADC-EVALDZ](#) board to the PC with a USB cable. (Connect to P702.)
5. On the [AD9250](#) or the [AD6673](#) evaluation board, ensure that the jumpers are installed on the P205, P206, and P204 headers for default setup.
6. On the [AD9250](#) or the [AD6673](#) evaluation board, provide a clean, low jitter clock source to Connector J505 at the desired ADC conversion rate. If the [AD9250](#) or the [AD6673](#) input clock divider is used, provide a clock into the J505 connector at the appropriate rate. The input clock level must be between 10 dBm and 14 dBm.
7. On the [AD9250](#) or the [AD6673](#) evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at Connector J301 (Channel A) and/or Connector J303 (Channel B). Use a 1 m, shielded, RG-58, 50  $\Omega$  coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50  $\Omega$  terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.) For the input level to be near the full-scale of the ADC, the generator level must be set to 8 dBm to 12 dBm, and this level depends on the input frequency and any losses in band-pass filters.

8. Open the **VisualAnalog** software on the PC. The [AD9250](#) or the [AD6673](#) should be listed in the status bar of the **New Canvas** window (see Figure 2).

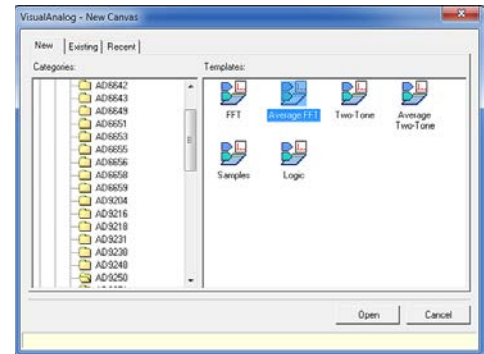


Figure 2. New Canvas Window

9. Select the template that corresponds to the type of testing that needs to be performed.
10. Select the **ADC Data Capture Settings** window and click the **Capture Board** tab (see the red box in Figure 3).
11. In the FPGA box, select the [AD9250\\_12\\_04\\_11\\_1225.mcs](#) program or the [AD6673\\_12\\_04\\_11\\_1225.mcs](#) program to configure the FPGA.
12. Click **Program** to download the file to the FPGA. The **CONFIG\_DONE** LED should illuminate on the [HSC-ADC-EVALDZ](#) board indicating that the FPGA has been correctly programmed.

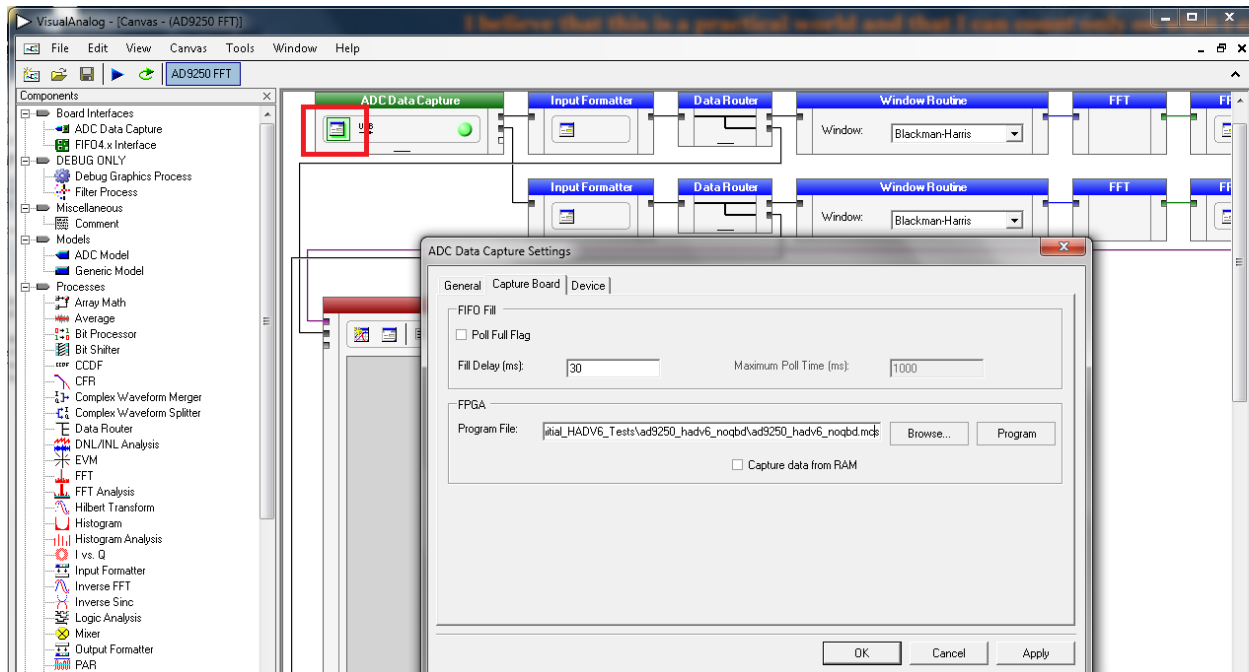


Figure 3. VisualAnalog, ADC Data Capture Settings Window

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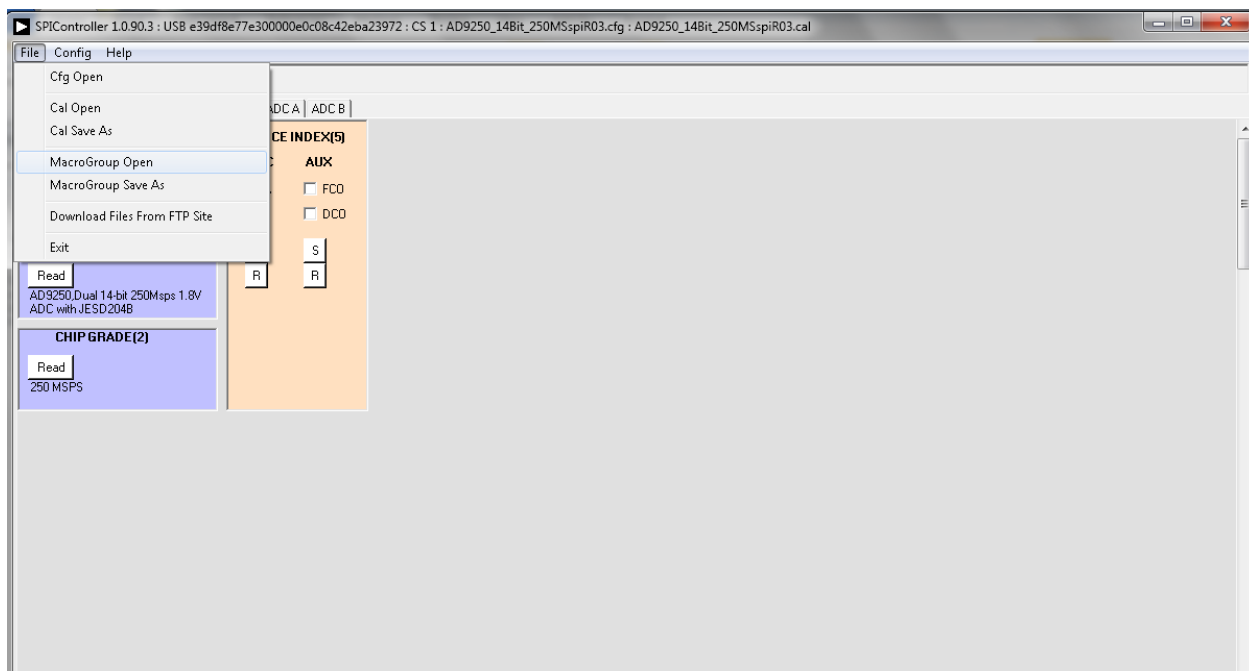


Figure 4. SPIController Software, MacroGroup Open

11140-004

13. Open the **SPIController** software. If prompted for a configuration file, select the **AD9250\_14Bit\_250MSPiR03.cfg** or **AD6673\_14Bit\_250MSPiR03.cfg**. If not, check the title bar of the window to see which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the correct configuration file. Note that the **CHIP ID(1)** field may be filled whether the correct SPIController configuration file is loaded or not.
14. In the **SPIController** software, click **File > MacroGroup Open** (see Figure 4).
15. Select the **AD9250\_M2L2\_SPI.mgp** or the **AD6673\_M2L2\_SPI.mgp** file and click **Open**.
16. Select **Config > Launch Macro Editor** (see Figure 5). The **MarcoEditor** window opens (see Figure 6).

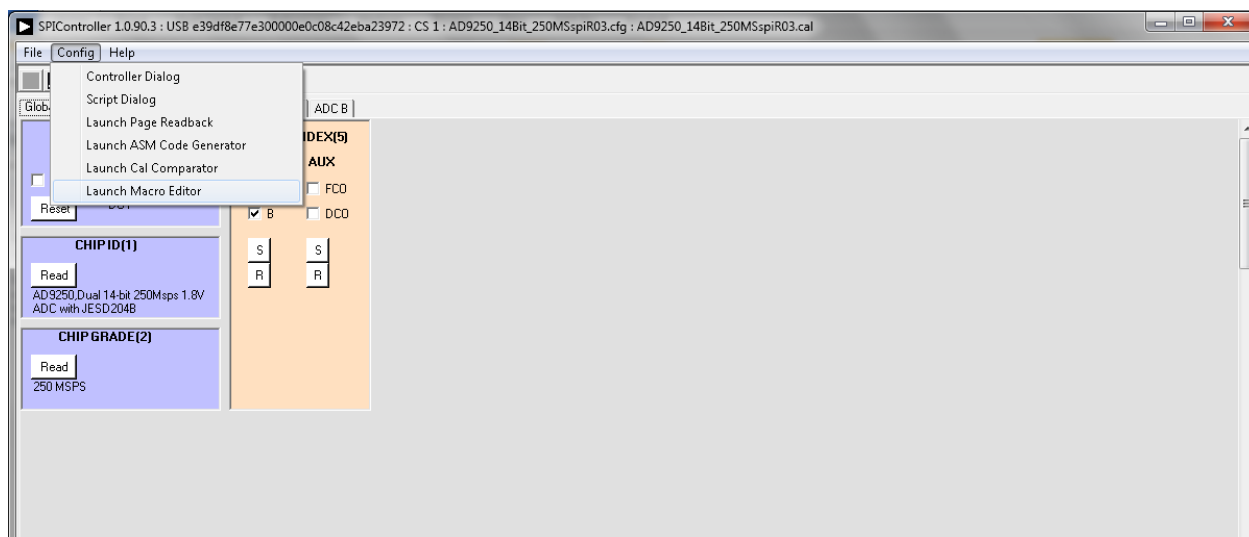


Figure 5. SPIController Software, Launch Macro Editor

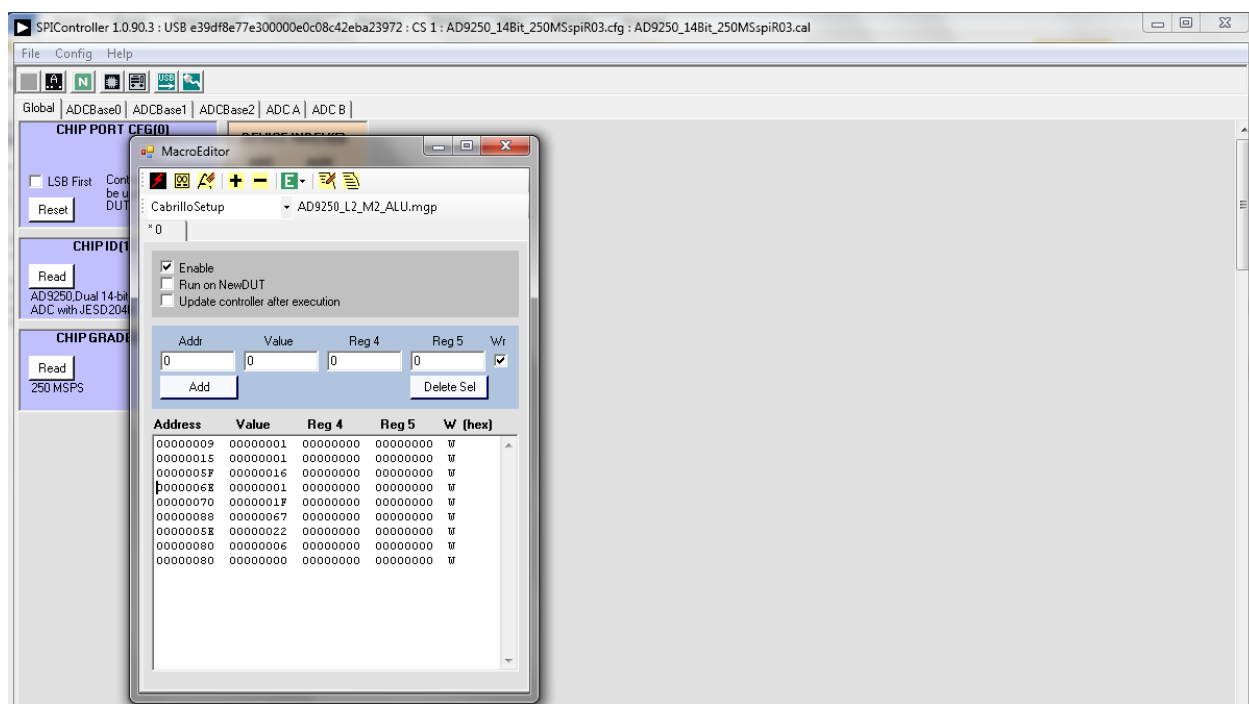


Figure 6. SPIController Software, MacroEditor

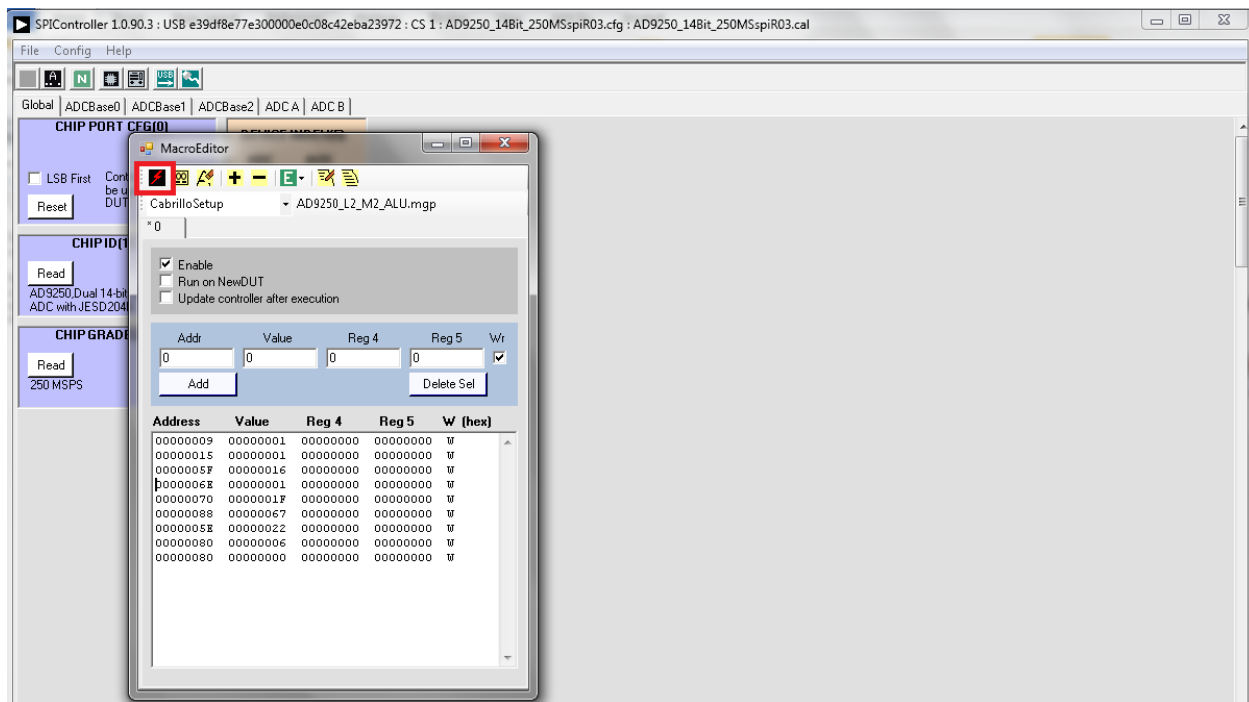


Figure 7. SPIController Software, Run Macro

17. Before running the macro, unplug the power connector to the [AD9250](#) or the [AD6673](#) evaluation board and reconnect it.
18. Click **Run Macro** to configure the [AD9250](#) or the [AD6673](#) (see highlighted red in Figure 7).
19. Click **Run** (🔴) in the **VisualAnalog** software.
20. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund**

**Power** reading in the left panel of the **VisualAnalog FFT** window.)

21. If desired, click **File > Save Form as** in the FFT window to save the FFT plot

## TROUBLESHOOTING

Four troubleshooting issues include the following:

- FFT plot appears abnormal
- FFT plot appears normal, but the performance is poor
- FFT window remains blank after clicking **Run**
- VisualAnalog indicates **FIFO capture timed out**

### ***FFT Plot Appears Abnormal***

Take the following steps if the FFT plot appears abnormal:

- If a normal noise floor is seen when the signal generator is disconnected from the analog input, ensure that the ADC is not being overdriven. Reduce input level, if necessary.
- In **VisualAnalog**, click **Settings** in the **Input Formatter** block. Ensure that **Number Format** is set to the correct encoding (twos complement by default).

### ***FFT Plot Appears Normal, but the Performance Is Poor***

Take the following steps if the FFT plot appears normal but the performance is poor:

- Ensure that the appropriate filter is being used on the analog input.
- Ensure that the signal generators for the clock and the analog input are clean (low phase noise).
- If noncoherent sampling is being used, change the analog input frequency slightly.
- Ensure that the SPI configuration file matches the product being evaluated.

### ***FFT Window Remains Blank After Run Is Clicked***

Take the following steps if the FFT window remains blank after **Run** is clicked:

- Ensure that the [AD9250](#) or the [AD6673](#) evaluation board is securely connected to the [HSC-ADC-EVALDZ](#) board.
- Disconnect power from both the [AD9250](#) or the [AD6673](#) evaluation board and the [HSC-ADC-EVALDZ](#) board, disconnect the USB cable from the [HSC-ADC-EVALDZ](#) board, and begin again at Step 1.
- Ensure that the FPGA has been programmed by verifying that the **CONFIG\_DONE** LED is illuminated on the [HSC-ADC-EVALDZ](#) board.
- Ensure that the correct FPGA program was installed.

### ***VisualAnalog Indicates FIFO Capture Timed Out***

Take the following steps if the VisualAnalog indicates that the **FIFO Capture Timed Out**:

- Ensure that all power and USB connections are secure.
- Confirm that the encode clock source is present at Connector J505.

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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