ON Semiconductor®

7-Bit, Programmable, Dual-Phase, Mobile, CPU, Synchronous Buck Controller

ADP3208

FEATURES

Single-chip solution
- **Fully compatible with the Intel® IMVP-6+™ specifications**
- **Integrated MOSFET drivers**

Selectable 1- or 2-phase operation with up to 1 MHz per phase switching frequency
Guaranteed ±8 mV worst-case differentially sensed core voltage error over temperature
Automatic power-saving mode maximizes efficiency with light load during deeper sleep operation
Soft transient control reduces inrush current and audio noise
Active current balancing between output phases
Independent current limit and load line setting inputs for additional design flexibility
Built-in power-good blanking supports voltage identification (VID) on-the-fly transients
7-bit, digitally programmable DAC with 0.3 V to 1.5 V output
Short-circuit protection with programmable latch-off delay
Clock enable output delays the CPU clock until the core voltage is stable
Output power or current monitor options
48-lead LFCSP

APPLICATIONS

Notebook power supplies for next-generation Intel processors

GENERAL DESCRIPTION

The ADP3208 is a highly efficient, multiphase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3208 is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7-bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The phase relationship of the output signals ensures interleaved 2-phase operation.

The ADP3208 uses a multimode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The ADP3208 switches between single- and dual-phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3208 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power-good output. The IC supports on-the-fly output voltage changes requested by the CPU.

The ADP3208 is specified over the extended commercial temperature range of 0°C to 100°C and is available in a 48-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

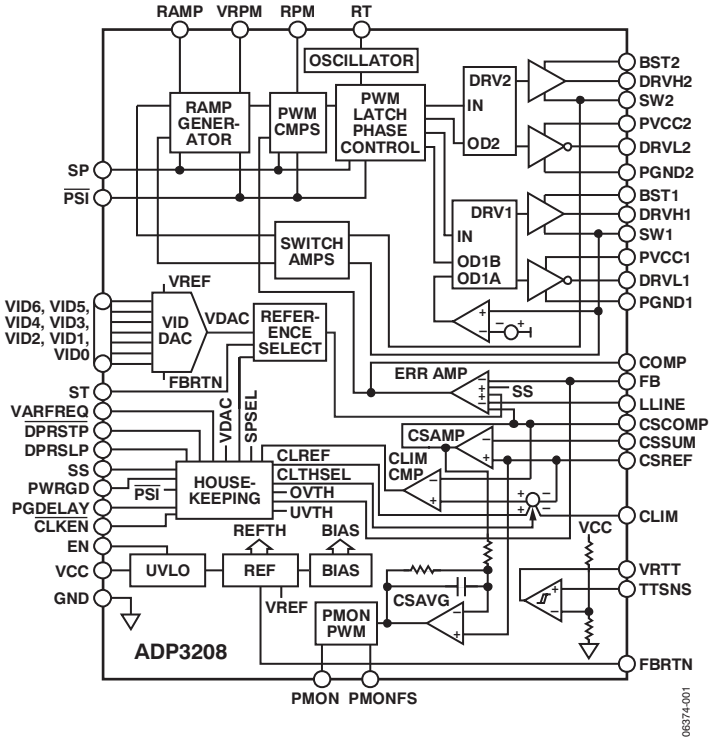

Figure 1.

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REVISION HISTORY

12/07- Rev 1: Conversion to ON Semiconductor

9/07—Rev. Sp0 to Rev. SpA

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10/06—Revision Sp0: Initial Version

SPECIFICATIONS

VCC = PVCC1 = PVCC2 = BST1 = BST2 = high = 5 V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = low = 0 V, EN = VARFREQ = high, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, $\overline{DPRSTP}$ = 0 V, V_{VID} = 1.2000 V, T_A = 0°C to 100°C, unless otherwise noted.[1] Current entering a pin (sunk by the device) has a positive sign.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE ERROR AMPLIFIER						
Output Voltage Range	V_{COMP}		0.8		3.6	V
DC Accuracy	V_{FB}	Relative to nominal V_{VID}, LLINE = CSREF				
		V_{VID} = 0.5000 V to 1.5000 V	−8		+8	mV
		V_{VID} = 0.3000 V to 0.4875 V	−10		+10	mV
Boot Voltage	$V_{BOOT(FB)}$	Startup	1.192	1.200	1.208	V
LLINE Positioning Accuracy	ΔV_{FB}	LLINE − CSREF = −80 mV	78	80	82	mV
		LLINE − CSREF = −200 mV	180	200	220	mV
LLINE Input Bias Current	I_{LLINE}		−80		+80	nA
Differential Nonlinearity[2]			−1		+1	LSB
Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.005		%
Input Bias Current	I_{FB}		−1		+1	µA
FBRTN Current	I_{FBRTN}			60	400	µA
Output Current	I_{COMP}	FB forced to V_{VID} − 3%		−4		mA
		FB forced to V_{VID} + 3%		900		µA
Gain Bandwidth Product[2]	GBW	COMP = FB		20		MHz
Slew Rate[2]		C_{COMP} = 10 pF		25		V/µs
VID DAC INPUTS						
Input Low Voltage	V_{IL}	VID(x)		0.52	0.3	V
Input High Voltage	V_{IH}	VID(x)	0.7	0.52		V
Input Current	$I_{IN(VID)}$	Sink current		1		µA
VID Transition Delay Time[2]		VID code change to FB change	400			ns
PWM OSCILLATOR						
Frequency Range[2]		$\overline{PSI}$ = $\overline{DPRSTP}$ = 1.05 V, DPRSLP = 0 V	0.3		3	MHz
Frequency	f_{OSC}	T_A = 25°C, RT = 250 kΩ, PWM mode, VARFREQ = high, V_{VID} = 1.5000 V		400		kHz
		T_A = 25°C, RT = 125 kΩ, PWM mode, VARFREQ = high, V_{VID} = 1.5000 V		750		kHz
RT Voltage	V_{RT}	RT = 250 kΩ to GND, V_{VID} = 1.5000 V, VARFREQ = low	1.08	1.25	1.32	V
VRPM Reference Voltage	V_{VRPM}	I_{VRPM} = 0 µA	0.95	1	1.05	V
		I_{VRPM} = 120 µA	0.95	1	1.16	V
RPM Output Current	I_{RPM}	V_{VID} = 1.5000 V, RT = 250 kΩ		−5		µA
RPM Comparator Offset	$V_{OS(RPM)}$	$\lvert V_{COMP} - V_{RPM} \rvert$, $\overline{PSI}$ = 0 V	−20	−1	+15	mV
RAMP Input Voltage	V_{RAMP}		0.9	1.0	1.1	V
RAMP Input Current Range	I_{RAMP}	EN = high	1		50	µA
RAMP Input Current in Shutdown		EN = low or UVLO, RAMP = 19 V		1		µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF	−2.0		+2.0	mV
Input Bias Current	I_{CSSUM}		−65		+65	nA
Input Common-Mode Range[2]		CSSUM and CSREF	0		3.5	V
Output Voltage Range	V_{CSCOMP}		0.05		2.7	V
Output Current	I_{CSCOMP}	Sink current		1		mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Source current		−15		mA
Gain Bandwidth Product[2]	GBW_{CSA}			10		MHz
Slew Rate[2]		C_{CSCOMP} = 10 pF		10		V/µs
CURRENT BALANCE AMPLIFIER						
Common-Mode Voltage Range[2]	$V_{SW(x)}$		−600		+200	mV
Input Resistance	$R_{SW(x)}$		30	50	60	kΩ
Input Current	$I_{SW(x)}$	SW(x) = 0 V		−3.5		µA
Input Current Matching	$\Delta I_{SW(x)}$	SW(x) = 0 V	−5		+5	%
Zero Current Switching Threshold Voltage	$V_{ZCS(SW1)}$	DPRSLP = 3.3 V, DCM		−6		mV
DCM Minimum Off Time Masking	$t_{OFFMASK}$	DPRSLP = 3.3 V, SW1 falling		450		ns
CURRENT LIMIT COMPARATOR						
Output Current	I_{CLIM}	R_{CLIM} = 125 kΩ		10		µA
Current Limit Threshold Voltage	V_{CLTH}	$V_{CSREF} - V_{CSCOMP}$, R_{CLIM} = 125 kΩ, SP = low (2-phase), $\overline{PSI}$ = 1.05 V	111	125	139	mV
		$V_{CSREF} - V_{CSCOMP}$, R_{CLIM} = 125 kΩ, SP = low (2-phase), $\overline{PSI}$ = 0 V or DPRSLP = low	54	62.5	74	mV
		$V_{CSREF} - V_{CSCOMP}$, R_{CLIM} = 125 kΩ, SP = high (1-phase)	111	125	139	mV
Current Limit Setting Ratio		V_{CL}/V_{ILIM}, $\overline{PSI}$ = 1.05 V		0.1		
		V_{CL}/V_{ILIM}, $\overline{PSI}$ = low, SP = low		0.05		
SOFT START/LATCH-OFF TIMER						
Output Current	I_{SS}	V_{SS} < 1.7 V, startup	−10	−8	−6	µA
		V_{SS} > 1.7 V, normal mode		−48		µA
		V_{SS} > 1.7 V, current limit	−2.5	−2	−1.5	µA
Termination Threshold Voltage	$V_{TH(SS)}$	Startup, SS rising	1.6	1.7	1.8	V
Normal Mode Operating Voltage		$\overline{CLKEN}$ = low		2.9		V
Current Limit Latch-Off Voltage	$V_{LOFF(SS)}$	Current limit or PWRGD failure, SS falling	1.55	1.65	1.8	V
SOFT TRANSIENT CONTROL						
ST Sourcing Current	$I_{SOURCE(ST)}$	Fast exit from deeper sleep mode, DPRSLP = 0 V, ST = V_{DAC} − 0.3 V		−9		µA
		Slow exit from deeper sleep mode, DPRSLP = 3.3 V, $\overline{DPRSTP}$ = 0, ST = V_{DAC} − 0.3 V		−2.5		µA
ST Sinking Current	$I_{SINK(ST)}$	Slow entry to deeper sleep, DPRSLP = 3.3 V, ST = V_{DAC} + 0.3 V		2.5		µA
ST Offset Voltage	$V_{OS(ST)}$	|ST − V_{VID}| at the end of PWRGD masking	−25		+25	mV
Minimum Capacitance[2]	C_{ST}		100			pF
Extended PWRGD Masking Comparator Voltage Threshold	$V_{TH(ST)}$	|ST − V_{VID}|, DPRSLP = 3.3 V, ST falling		170		mV
DIGITAL CONTROL INPUTS						
Input Low Voltage	V_{IL}	$\overline{PSI}$, $\overline{DPRSTP}$			0.3	V
		VARFREQ, SP			0.7	V
		DPRSLP, EN			1.0	V
Input High Voltage	V_{IH}	$\overline{PSI}$, $\overline{DPRSTP}$	0.7			V
		VARFREQ, SP	4			V
		DPRSLP, EN	2.3			V
Input Current	I_{IN}	$\overline{DPRSTP}$, VARFREQ, DPRSLP, SP		20		nA
		EN = low or EN = high		20		nA
		EN = $V_{TH(EN)}$, high-to-low or low-to-high		60		µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		transition				
		$\overline{DPRSTP}$ = high, $\overline{PSI}$ = high		1		µA
		$\overline{PSI}$ = low		−100		nA
THERMAL THROTTLING/CROWBAR DISABLE CONTROL						
TTSNS Voltage Range[2]		Temperature sensing	0.4		5	V
		Crowbar disable threshold disable	0		50	mV
TTSNS VRTT Threshold Voltage	$V_{VRTT(TTSNS)}$	VCC = 5 V, TTSNS falling	2.45	2.5	2.55	V
TTSNS VRTT Threshold Hysteresis			50	95		mV
TTSNS Crowbar Disable Threshold Voltage	$V_{CBDIS(TTSNS)}$				50	mV
TTSNS Input Current		TTSNS > 1.0 V, temperature sensing	−1		+1	µA
		TTSNS = 0 V, disabling overvoltage protection		−3		µA
VRTT Output Low Voltage	$V_{OL(VRTT)}$	$I_{SINK(VRTT)}$ = 400 µA		50	100	mV
VRTT Output High Voltage	$V_{OH(VRTT)}$	$I_{SOURCE(VRTT)}$ = −400 µA	4	5		V
POWER GOOD						
CSREF Undervoltage Threshold	$V_{UV(CSREF)}$	Relative to V_{VID} = 0.5 V to 1.5 V		−300		mV
		Relative to V_{VID} = 0.3125 V to 0.4875 V	−160			mV
CSREF Overvoltage Threshold	$V_{OV(CSREF)}$	Relative to V_{VID} = 0.5 V to 1.5 V	150	200	250	mV
CSREF Crowbar (Overvoltage Protection) Threshold	$V_{CB(CSREF)}$	Relative to FBRTN	1.65	1.7	1.75	V
CSREF Reverse Voltage Detection Threshold	$V_{RVP(CSREF)}$	Relative to FBRTN				
		CSREF falling	−400	−300		mV
		CSREF rising		−60	−5	mV
PWRGD Output Low Voltage	$V_{OL(PWRGD)}$	$I_{SINK(PWRGD)}$ = 4 mA		70	200	mV
PWRGD Output Leakage Current		V_{PWRDG} = 5 V		0.03	3	µA
Power-Good Delay Timer						
PGDELAY Voltage Detection Threshold	$V_{TH(PGDELAY)}$			2.9		V
PGDELAY Charge Current	$I_{PGDELAY}$	$V_{PGDELAY}$ = 2.0 V		−3		µA
PGDELAY Discharge Resistance	$R_{PGDELAY}$	$V_{PGDELAY}$ = 0.2 V		600		Ω
PWRGD Masking Time				130		µs
CLOCK ENABLE						
Output Low Voltage		I_{SINK} = 4 mA		100	400	mV
Output Leakage Current		$\overline{CLKEN}$ = 5 V, V_{SS} = GND			1	µA
POWER MONITOR						
PMON Output Resistance		I_{SINK} = 2 mA		16		Ω
PMON Leakage Current		PMON = 5 V			1	µA
PMON Oscillator Frequency		PMONFS = 2 V		320		kHz
PMONFS Voltage Range[2]			1.5		4	V
PMONFS Output Current		PMONFS = 2.5 V		−10		µA
HIGH-SIDE MOSFET DRIVERS						
DRVH Output Resistance, Sourcing Current		BST − SW = 4.6 V		1.9	3.3	Ω
DRVH Output Resistance, Sinking Current		BST − SW = 4.6 V		1.5	3	Ω
Transition Times	$tr_{DRVH,}$	BST − SW = 4.6 V, C_L = 3 nF, see Figure 2		10	30	ns
	tf_{DRVH}	BST − SW = 4.6 V, C_L = 3 nF, see Figure 2		8	25	ns
Propagation Delay Time	$tpdh_{DRVH}$	BST − SW = 4.6 V, see Figure 2		16	70	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BST Quiescent Current		EN = low, shutdown		5		µA
		EN = high, no switching		120		µA
LOW-SIDE MOSFET DRIVERS						
Output Resistance, Sourcing Current				1.8	3.3	Ω
Output Resistance, Sinking Current				1.4	2.5	Ω
Transition Times	tr_{DRVL}	C_L = 3 nF, see Figure 2		11	30	ns
	tf_{DRVL}	C_L = 3 nF, see Figure 2		9	25	ns
Propagation Delay Time	$tpdl_{DRVL}$	C_L = 3 nF, see Figure 2		13	30	ns
SW Transition Timeout	$t_{TO(SW)}$	BST − SW = 4.6 V	80	130	300	ns
Zero Voltage Switching Detection Threshold	$V_{ZVS(SW)}$			2.2		V
PVCC Quiescent Current		EN = low, shutdown		13		µA
		EN = high, no switching		180		µA
SUPPLY						
Supply Voltage Range[2]	V_{CC}		4.5		5.5	V
Supply Current		EN = high, normal mode		5.5	10	mA
		EN = low, shutdown		32	150	µA
VCC OK Threshold Voltage	V_{CCOK}	VCC rising		4.4	4.5	V
VCC UVLO Threshold Voltage	V_{CCUVLO}	VCC falling	4.0	4.2		V
UVLO Hysteresis[2]			150			mV

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or characterization, not production tested.

TIMING DIAGRAM

Timing is referenced to the 90% and 10% points, unless otherwise noted.

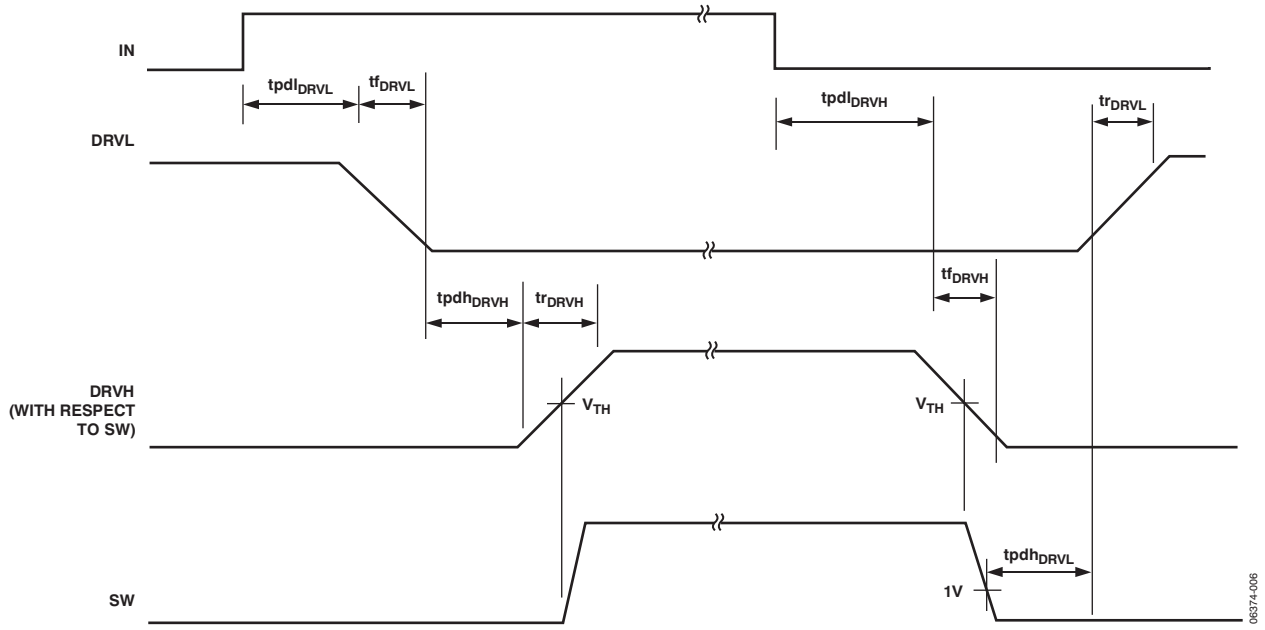


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC, PVCC1, PVCC2	−0.3 V to +6 V
FBRTN, PGND1, PGND2	−0.3 V to +0.3 V
BST1, BST2	
DC	−0.3 V to +25 V
t < 200 ns	−0.3 V to +30 V
BST1 to SW1, BST2 to SW2	−0.3 V to +6 V
DRVH1, DRVH2, SW1, SW2	
DC	−5 V to +20 V
t < 200 ns	−10 V to +25 V
DRVH1 to SW1, DRVH2 to SW2, DRVL1 to PGND1, DRVL2 to PGND2	−0.3 V to +6 V
DC	−0.3 V to +6 V
t < 200 ns	−5 V to +6 V
RAMP (in Shutdown)	
DC	−0.3 V to +20 V
t < 200 ns	−0.3 V to +25 V
All Other Inputs and Outputs	−0.3 V to +6 V
Storage Temperature	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 100°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA}) 2-Layer Board	40°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

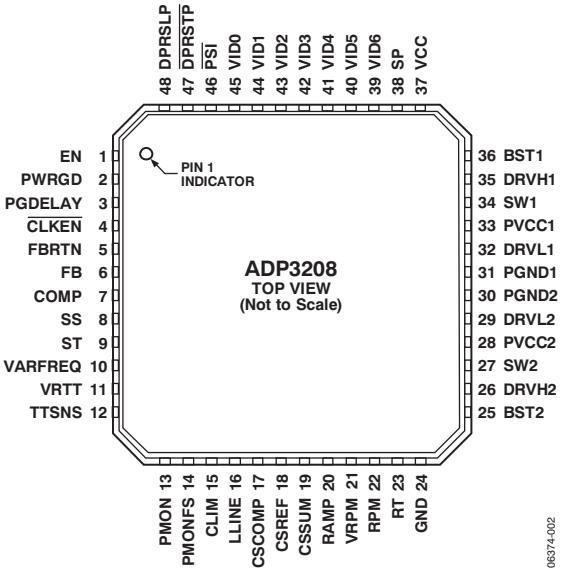


Figure 3. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls $\overline{\text{CLKEN}}$ high.
2	PWRGD	Power-Good Output. Open-drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
3	PGDELAY	Power-Good Delay Setting Input/Output. A capacitor connected from this pin to GND sets the power-good delay time.
4	$\overline{\text{CLKEN}}$	Clock Enable Output. Open-drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock.
5	FBRTN	Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
6	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
7	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
8	SS	Soft Start and Latch-Off Delay Setting Input/Output. An external capacitor from this pin to GND sets the soft start ramp-up time and the current limit latch-off delay ramp-down time.
9	ST	Soft Transient Slew Rate Timing Input/Output. A capacitor from this pin to GND sets the slew rate of the output voltage when it transitions from one VID setting to another, including boot-to-active VID, VID on the fly, and deeper sleep entry and exit transients.
10	VARFREQ	Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code.
11	VRTT	Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level.
12	TTSNS	Thermal Throttling Sense and Crowbar Disable Input. A resistor divider where the upper resistor is connected to VCC, the lower resistor (NTC thermistor) is connected to GND, and the center point is connected to this pin and acts as a temperature sensor half bridge. Connecting TTSNS to GND disables the thermal throttling function and disables the crowbar, or overvoltage protection (OVP), feature of the chip.
13	PMON	Power Monitor Output. Open-drain output. A pull-up resistor from PMON to CSREF provides a duty cycle–modulated power output signal. An external RC network can be used to convert the digital signal stream to an averaged power analog output voltage.
14	PMONFS	Power Monitor Full-Scale Setting Input/Output. A resistor from this pin to GND sets the full-scale value of the PMON output signal.

Pin No.	Mnemonic	Description
15	CLIM	Current Limit Setting Input/Output. An external resistor from this pin to GND sets the current limit threshold of the converter.
16	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP can be tied to this pin to set the load line slope.
17	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
18	CSREF	Current Sense Reference Input. This pin must be connected to the common point of the output inductors. The node is shorted to GND through an internal switch when the chip is disabled to provide soft stop transient control of the converter output voltage.
19	CSSUM	Current Sense Summing Input. External resistors from each switch node to this pin sum the inductor currents to provide total current information.
20	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp used for phase-current balancing.
21	VRPM	RPM Mode Reference Voltage Output.
22	RPM	Ramp Pulse Modulation Current Source Output. A resistor between this pin and VRPM sets the RPM comparator upper threshold.
23	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
24	GND	Analog and Digital Signal Ground.
25	BST2	High-Side Bootstrap Supply for Phase 2. A capacitor from this pin to SW2 holds the bootstrapped voltage while the high-side MOSFET is on.
26	DRVH2	High-Side Gate Drive Output for Phase 2.
27	SW2	Current Balance Input for Phase 2 and Current Return for High-Side Gate Drive.
28	PVCC2	Power Supply Input/Output of Low-Side Gate Driver for Phase 2.
29	DRVL2	Low-Side Gate Drive Output for Phase 2.
30	PGND2	Low-Side Driver Power Ground for Phase 2.
31	PGND1	Low-Side Driver Power Ground for Phase 1.
32	DRVL1	Low-Side Gate Drive Output for Phase 1.
33	PVCC1	Power Supply Input/Output of Low-Side Gate Driver for Phase 1.
34	SW1	Current Balance Input for Phase 1 and Current Return For High-Side Gate Drive.
35	DRVH1	High-Side Gate Drive Output for Phase 1.
36	BST1	High-Side Bootstrap Supply for Phase 1. A capacitor from this pin to SW1 holds the bootstrapped voltage while the high-side MOSFET is on.
37	VCC	Power Supply Input/Output of the Controller.
38	SP	Single-Phase Select Input. Logic high state sets single-phase configuration.
39 to 45	VID6 to VID0	Voltage Identification DAC Inputs. A 7-bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code table, Table 6).
46	$\overline{\text{PSI}}$	Power State Indicator Input. Driving this pin low forces the controller to operate in single-phase mode.
47	$\overline{\text{DPRSTP}}$	Deeper Stop Control Input. The logic state of this pin is usually complementary to the state of the DPRSLP pin; however, during slow deeper sleep exit, both pins are logic low.
48	DPRSLP	Deeper Sleep Control Input.

TEST CIRCUITS

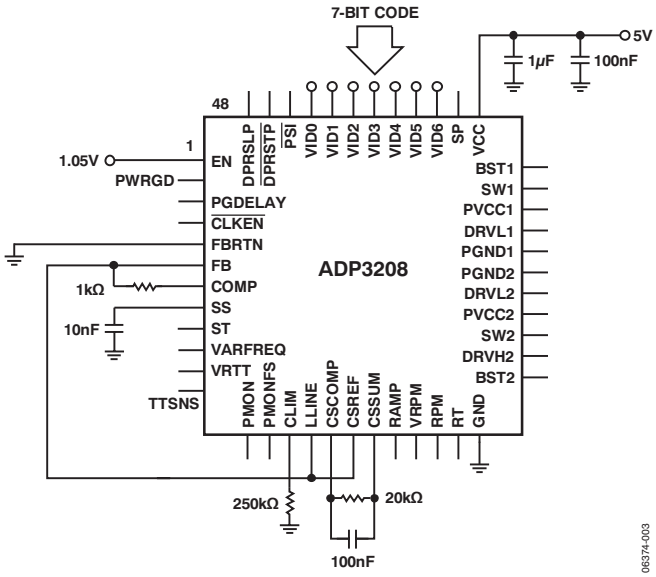


Figure 4. Closed-Loop Output Voltage Accuracy

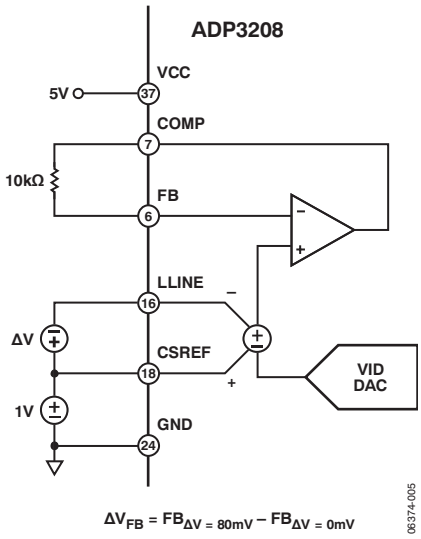


Figure 6. Positioning Accuracy

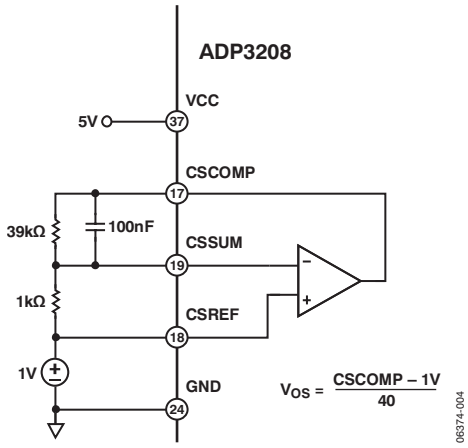


Figure 5. Current Sense Amplifier, V_{OS}

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

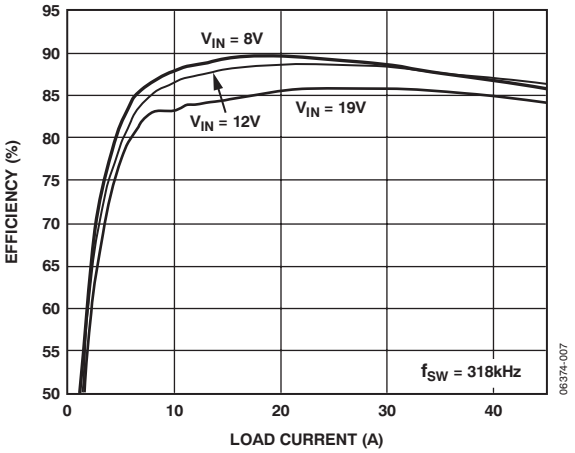


Figure 7. PWM Mode Efficiency vs. Load Current

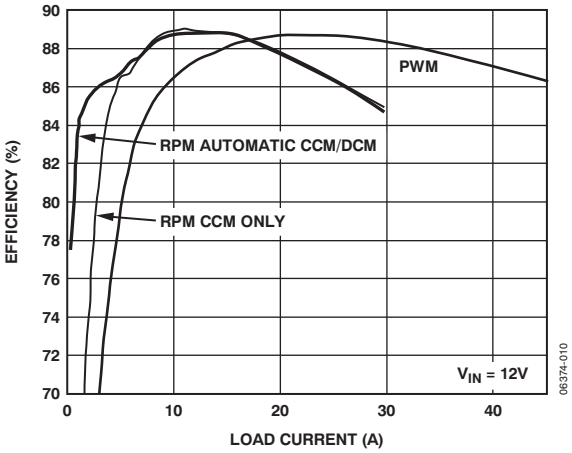


Figure 10. Efficiency vs. Load Current in All Modes

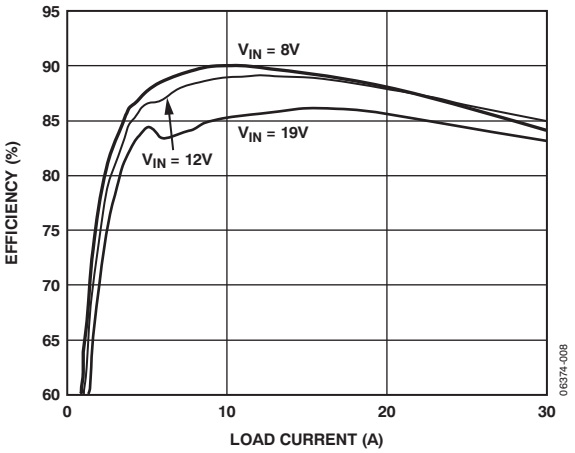


Figure 8. RPM Mode Efficiency vs. Load Current in CCM Only

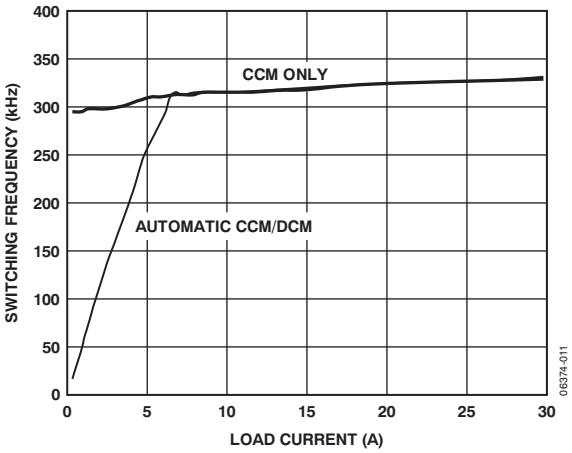


Figure 11. Switching Frequency vs. Load Current in RPM Mode

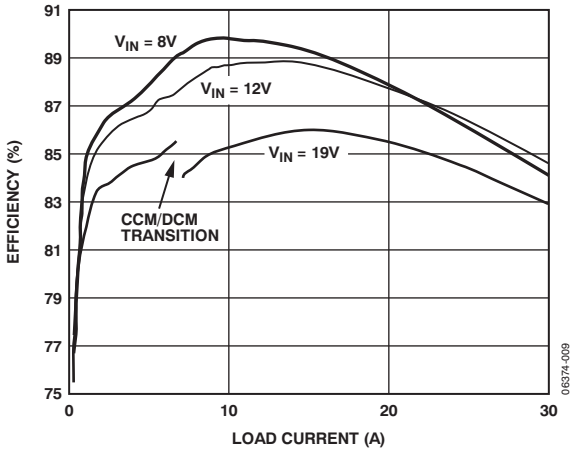


Figure 9. RPM Mode Efficiency vs. Load Current Automatic in CCM/DCM

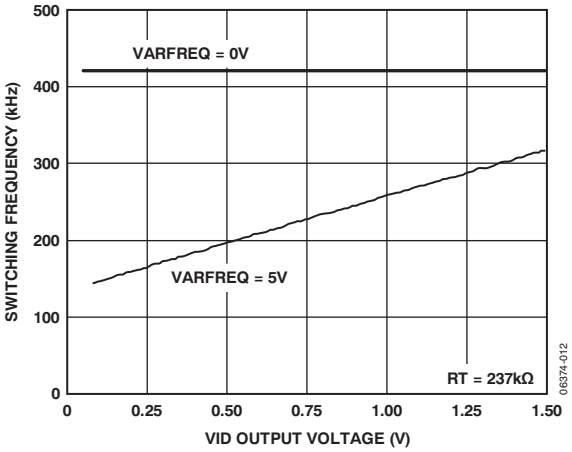


Figure 12. Switching Frequency vs. VID Output Voltage in PWM Mode

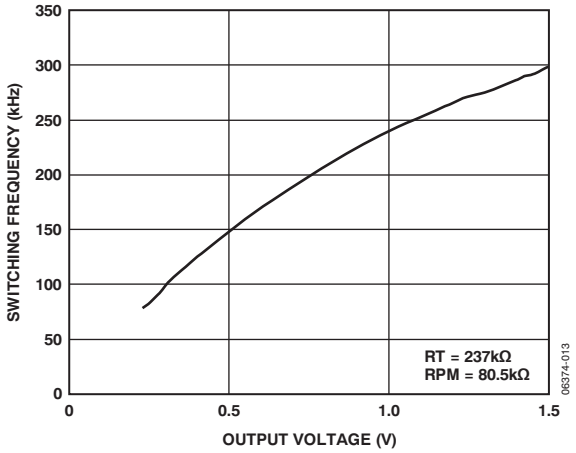


Figure 13. Switching Frequency vs. Output Voltage in RPM Mode

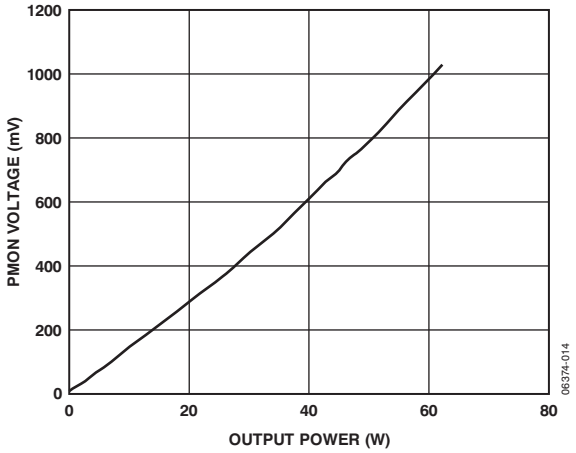


Figure 14. PMON Voltage vs. Output Power

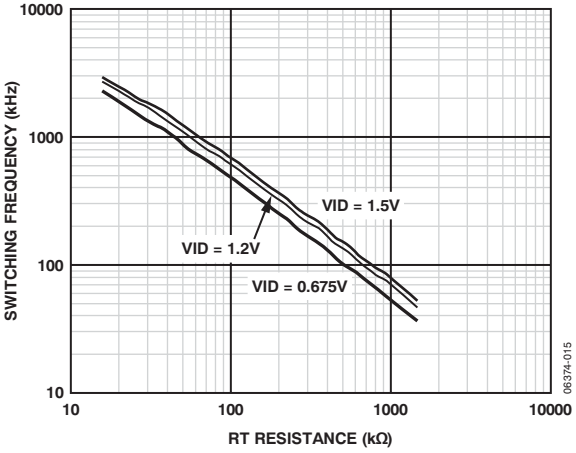


Figure 15. Per Phase Switching Frequency vs. RT Resistance

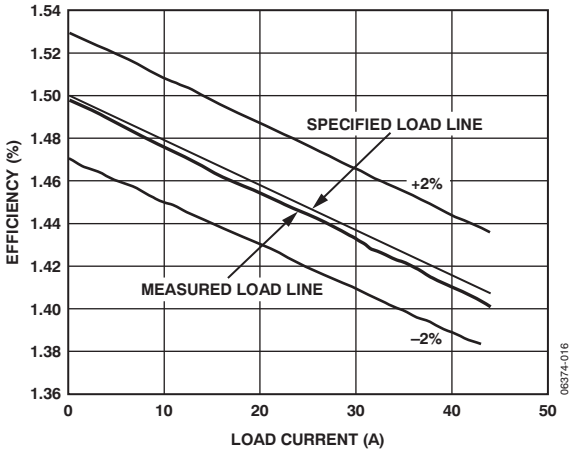


Figure 16. Load Line Accuracy

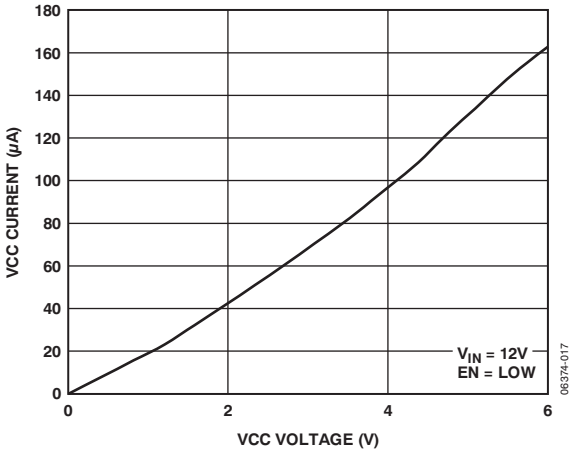


Figure 17. VCC Current vs. VCC Voltage with Enable Low

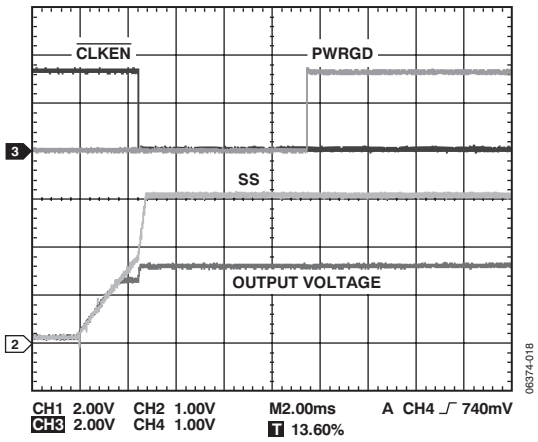


Figure 18. Start-Up Waveforms

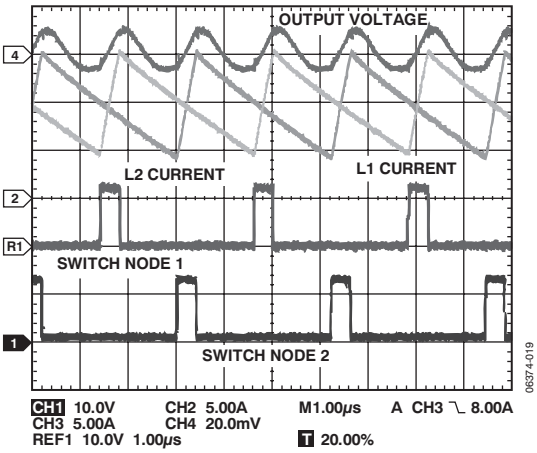


Figure 19. Dual-Phase, Interleaved PWM Waveform, 20 A Load

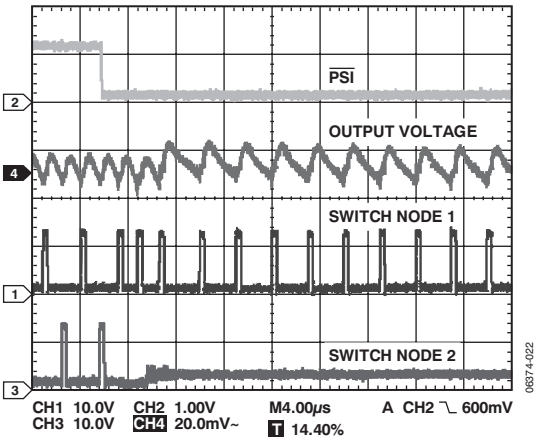


Figure 22. $\overline{PSI}$ Transition

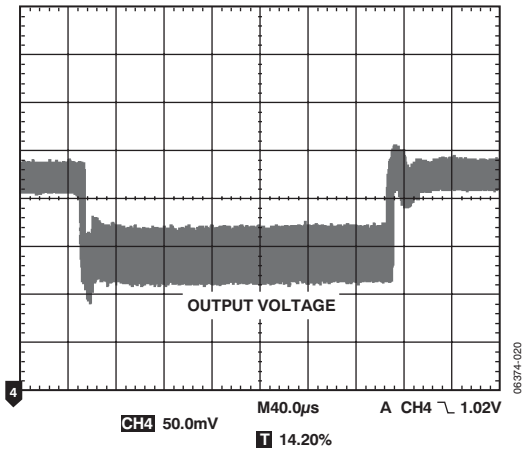


Figure 20. Load Transient, 9 A to 44 A

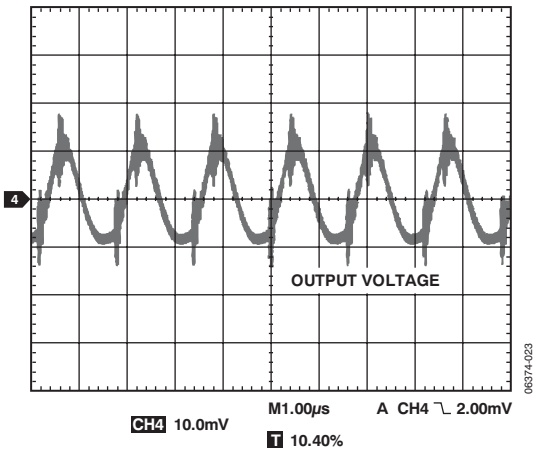


Figure 23. PWM Mode Output Ripple, 40 A Load, V_{IN} = 12 V

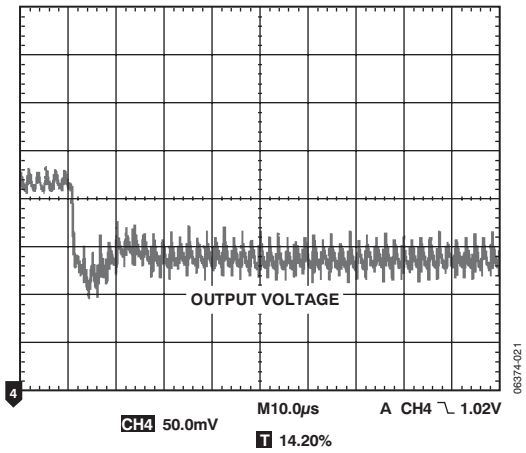


Figure 21. Load Transient, 9 A to 44 A

THEORY OF OPERATION

The ADP3208 combines multimode pulse-width-modulated (PWM) control and ramp-pulse-modulated (RPM) control with multiphase logic outputs for use in single- and dual-phase synchronous buck CPU core supply power converters. The internal 7-bit VID DAC conforms to the Intel IMVP-6+ specifications.

Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single-phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multimode control of the ADP3208 is a stable, high performance architecture that includes

- Current and thermal balance between phases
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High current output by supporting 2-phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency with heavy and light loads
- Increased immunity from noise introduced by PC board layout constraints
- Ease of use due to independent component selection
- Flexibility in design by allowing optimization for either low cost or high performance

NUMBER OF PHASES

The number of operational phases can be set by the user. Tying the SP pin to the VCC pin forces the chip into single-phase operation. Otherwise, dual-phase operation is automatically selected, and the chip switches between single- and dual-phase modes as the load changes to optimize power conversion efficiency.

In dual-phase configuration, SP is low and the timing relationship between the two phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

OPERATION MODES

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If SP is set low (user-selected dual-phase mode) during a VID transient or with a heavy load condition (indicated by DPRSLP being low and $\overline{PSI}$ being high), the ADP3208 runs in 2-phase, interleaved PWM mode to achieve minimal V_{CORE} output voltage ripple and the best transient performance possible. If the load becomes light (indicated by $\overline{PSI}$ being low or DPRSLP being high), ADP3208 switches to single-phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the ADP3208 is also capable of dynamically changing the control method. In dual-phase operation, the ADP3208 runs in PWM mode, where the switching frequency is controlled by the master clock. In single-phase operation (commanded by the $\overline{PSI}$ low state), the ADP3208 runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected between the VRPM and RPM pins. If the device is in single-phase mode and the system signal DPRSLP is asserted high during the deeper sleep mode of CPU operation, the ADP3208 continues running in RPM mode but offers the option of turning off the low-side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low-side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high- and low-side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 4 summarizes how the ADP3208 dynamically changes the number of active phases and transitions the operation mode based on system signals and operating conditions.

Table 4. Phase Number and Operation Modes[1]

$\overline{\text{PSI}}$ No.	DPRSLP	VID Transition[2]	Current Limit	No. of Phases Selected by the User	No. of Phases in Operation	Operation Modes[3]
*	*	Yes	*	N [2 or 1]	N	PWM, CCM only
1	0	No	*	N [2 or 1]	N	PWM, CCM only
0	0	No	No	*	1	RPM, CCM only
0	0	No	Yes	*	1	PWM, CCM only
*	1	No	No	*	1	RPM, automatic CCM/DCM
*	1	No	Yes	*	1	PWM, CCM only

[1] * = don't care.
[2] VID transient period is the time following any VID change, including entry into and exit from deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
[3] CCM stands for continuous current mode, and DCM stands for discontinuous current mode.

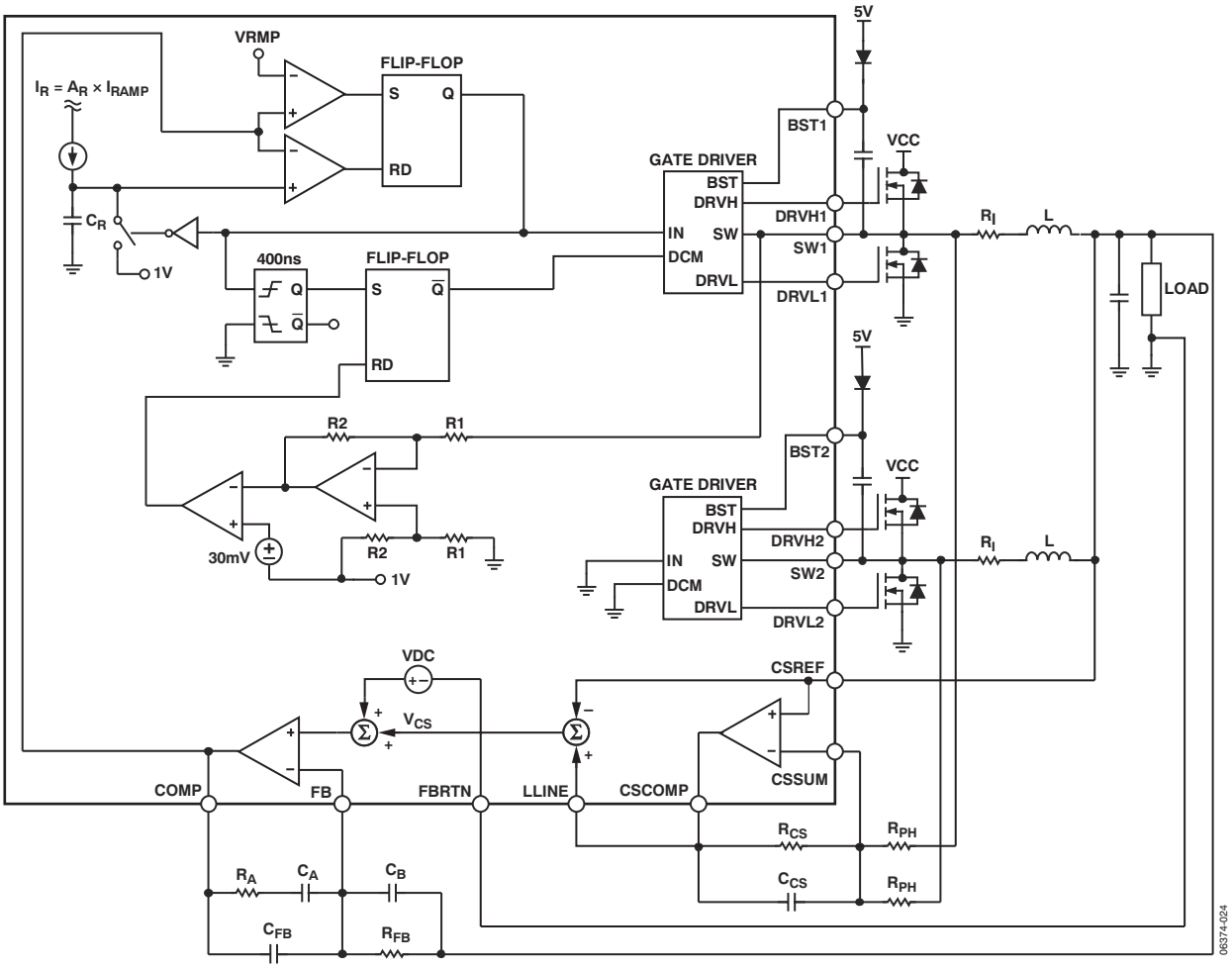


Figure 24. Single-Phase RPM Mode Operation

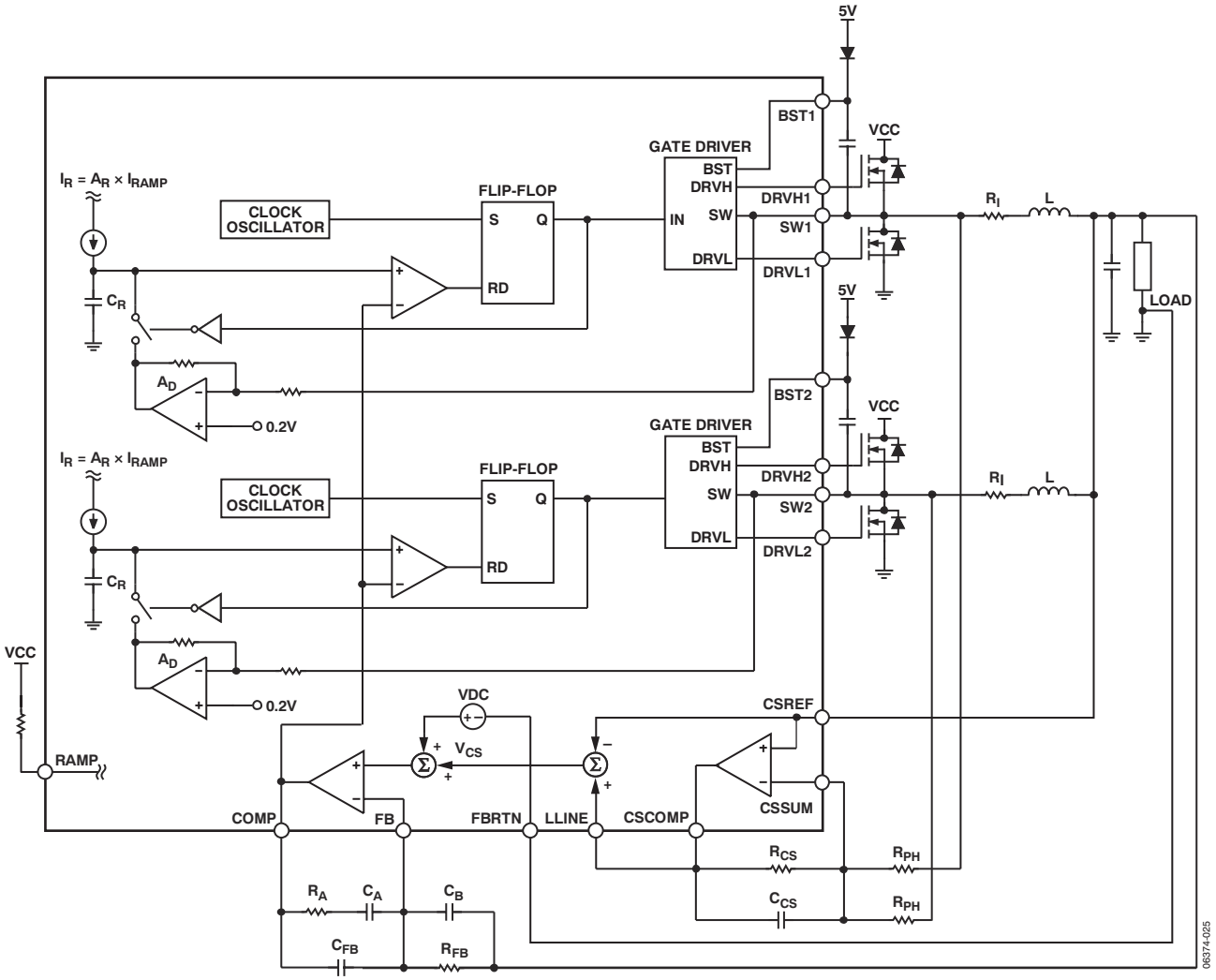


Figure 25. Dual-Phase PWM Mode Operation

Setting Switch Frequency

Master Clock Frequency in PWM Mode

When the ADP3208 runs in PWM, the clock frequency is set by an external resistor connected from the RT pin to GND. The frequency is constant at a given VID code but varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant V_{CORE} ripple and improves power conversion efficiency at lower VID voltages. Figure 15 shows the relationship between clock frequency and VID voltage, parameterized by RT resistance.

To determine the switching frequency per phase, divide the clock by the number of phases in use.

Switching Frequency in RPM Mode—Single-Phase Operation

In single-phase RPM mode, the switching frequency is controlled by the ripple voltage on the COMP pin, rather than by the master clock. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and VRPM, an internal ramp signal is started and DRVH1 is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One-third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH1 pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

DIFFERENTIAL SENSING OF OUTPUT VOLTAGE

The ADP3208 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP-6+ specification. In steady-state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst-case scenario within ±8 mV of the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point—the VCC remote sensing pin of the microprocessor. FBRTN should be connected directly to the negative remote sensing point—the V_{SS} sensing point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a maximum current of 200 μA for guaranteed accurate remote sensing.

OUTPUT CURRENT SENSING

The ADP3208 includes a dedicated current sense amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for over current detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low-side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSSUM pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by series summing resistors. The feedback resistor between the CSCOMP and CSSUM pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the microprocessor specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

ACTIVE IMPEDANCE CONTROL MODE

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying

the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feedforward response.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3208 has individual inputs for monitoring the current of each phase. The phase current information is combined with an internal ramp to create a current-balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent from the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so that the transient response of the system is optimal. The ADP3208 monitors the supply voltage to achieve feedforward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. More detail about programming the ramp is provided in the Application Information section.

The ADP3208 should not require external thermal balance circuitry if a good layout is used. However, if mismatch is desired due to uneven cooling in phase, external resistors can be added to individually control phase currents as long as the phase currents are mismatched by less than 30%. If unwanted mismatch exceeds 30%, a new layout that improves phase symmetry should be considered.

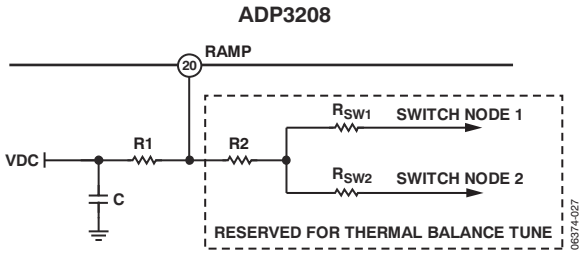


Figure 26. Optional Current Balance Resistors

In 2-phase operation, alternate cycles of the internal ramp control the duty cycle of the separate phases. Figure 26 shows the addition of two resistors from each switch node to the RAMP pin; this modifies the ramp-charging current individually for each phase. During Phase 1, SW Node 1 is high (practically at the input voltage potential) and SW Node 2 is low (practically at the ground potential). As a consequence, the RAMP pin, through the R2 resistor, sees the tap point of a divider connected to the input voltage, where R_{SW1} is the upper element and R_{SW2} is the lower element of the divider. During Phase 2, the voltages on SW Node 1 and SW Node 2 switch and the resistors swap functions. Tuning R_{SW1} and R_{SW2} allows the current to be optimally set for each phase. To increase the current for a given phase, decrease R_{SW} for that phase.

VOLTAGE CONTROL MODE

A high-gain bandwidth error amplifier is used for the voltage mode control loop. The noninverting input voltage is set via the 7-bit VID DAC. The VID codes are listed in Table 6. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

POWER-GOOD MONITORING

The power-good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output that can be pulled up through an external resistor to a voltage rail—not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the IMVP-6+ specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power-good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130 μs by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

POWER-UP SEQUENCE AND SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor tied from the SS pin to GND. The capacitance on the SS pin also determines the current limit latch-off time, as explained in the Current Limit, Short-Circuit, and Latch-Off Protection section. The power-up sequence, including the soft start is illustrated in Figure 27.

In VCC UVLO or shutdown mode, the SS pin is held at zero potential. When VCC ramps to a value greater than the upper UVLO threshold while EN is asserted high, the ADP3208 enables

the internal bias and starts a reset cycle of about 50 µs to 60 µs. When the initial reset is complete, the chip detects the number of phases set by the user and signals to ramp up the SS voltage. During soft start, the external SS capacitor is charged by an internal 8 µA current source. The V_{CORE} voltage follows the ramping SS voltage up to the V_{BOOT} voltage level determined by a burnt-in VID code (1.2 V according to the IMVP-6+ specification). While the V_{CORE} is regulated at the V_{BOOT} voltage, the SS capacitor continues to rise. When the SS pin voltage reaches 1.7 V, the ADP3208 immediately asserts the $\overline{CLKEN}$ signal low if the V_{CORE} voltage is within the power-good range defined by V_{BOOT}. In addition, the chip reads the VID codes provided by the CPU on the VID [0:6] input pins. The V_{CORE} voltage changes from the V_{BOOT} voltage to the VID voltage by a well-controlled soft transition slope (see the Soft Transient section). During this transition, the SS capacitor is quickly charged up to about a 2.9 V SS clamp level, controlled by the SS source current, which is increased to 48 µA (typical).

The PWRGD signal is asserted after a t_{CPU_PWRGD} delay of about 3 ms to 10 ms, as specified by IMVP-6+. The power-good delay can be programmed by the capacitor connected from the PGDELAY pin to GND. Before the $\overline{CLKEN}$ signal is asserted low, PGDELAY is reset to 0. Following the assertion of the $\overline{CLKEN}$ signal, an internal source current of 2 µA starts charging up the external capacitor on the PGDELAY pin. Assuming that the V_{CORE} voltage has settled within the power-good range defined by the VID DAC voltage, the PWRGD signal is asserted high when the PGDELAY voltage reaches the 2.9 V power-good delay termination threshold.

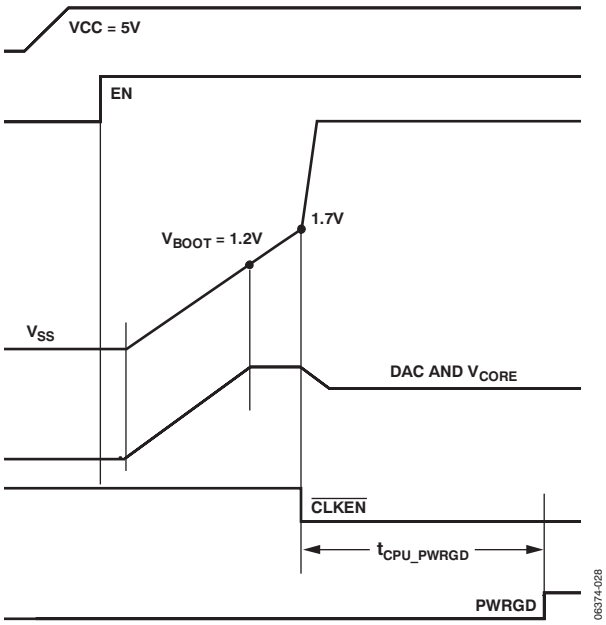


Figure 27. Power-Up Sequence of ADP3208

If EN is taken low or VCC drops below the VCC UVLO threshold, both the SS capacitor and the PGDELAY capacitor are reset to ground to prepare the chip for a subsequent soft start cycle.

SOFT TRANSIENT

The ADP3208 provides a soft transient function to reduce inrush current during various transitions, including entrance into and exit out of deeper sleep and the transition from V_{BOOT} to VID voltage. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented with an ST buffer amplifier that outputs constant sink or source current on the ST pin that is connected to an external capacitor. The capacitor is used to program the slew rate of V_{CORE} voltage during a VID voltage transient. During steady-state operation, the reference inputs of the voltage error amplifier and the ST amplifier are connected to the VID DAC output. Consequently, the ST voltage is a buffered version of VID DAC output. When system signals trigger a soft transition, the reference input of the voltage error amplifier switches from the DAC output to the ST output while the input of the ST amplifier remains connected to the DAC. The ST buffer input recognizes the almost instantaneous VID voltage change and tries to track it. However, tracking is not instantaneous because the slew rate of the buffer is limited by the source and sink current capabilities of the ST output. Therefore, the V_{CORE} voltage slew rate is controlled. When the transient period is complete, the reference input of the voltage amplifier reverts to the VID DAC output to improve accuracy.

Table 5 lists the source/sink current on the ST pin for various transitions. Charging/discharging the external capacitor on the ST pin programs the voltage slew rate of the ST pin and consequently of the V_{CORE} output. For example, a 390 pF ST capacitor results in a +10 mV/µs V_{CORE} slew rate for fast exit from deeper sleep and a ±3.3 mV/µs V_{CORE} slew rate for slow entry into or exit out of deeper sleep.

Table 5. Source/Sink Current of ST Pin

VID Transient	System Signals[1]		ST Pin Current (µA)
	DPRSLP	$\overline{DPRSTP}$	
Slow Entry into Deeper Sleep	High	*	−2.5
Fast Exit from Deeper Sleep	Low	*	+7.5
Slow Exit from Deeper Sleep	High	High	+2.5
Transient from V_{BOOT} to VID	*	*	±2.5

[1] * = do not care.

CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3208 compares the differential output of a current sense amplifier to a programmable current limit setpoint to provide the current-limiting function. The current limit threshold is set by the user with a resistor connected from the CLIM pin to GND, utilizing the fixed (10 μA typical) current sourced by the CLIM pin. The ground-referenced CLIM voltage is scaled down inside the chip by a factor of 10 in dual-phase operation and by a factor of 20 in single-phase operation. The scaled-down and level-shifted V_{CLTH} current limit threshold floats on top of the CSCOMP voltage. The current limit comparator monitors the differential voltage appearing across CSCOMP and CSREF and compares it with the floating V_{CLTH} threshold. If the sensed current exceeds the threshold, a current limit alert is released and the control of the internal COMP voltage is transferred from the voltage error amplifier to the current limit amplifier to maintain an average output current determined by the set current limit level.

When the output voltage is less than 200 mV during startup, a secondary current limit is activated. This is necessary because the voltage swing on the CSCOMP cannot extend below ground. The secondary current limit circuit clamps the internal COMP voltage at around 1.6 V, resulting in duty cycle–limited operation.

There is also an inherent per phase current limit that protects individual phases in case any of the phases stop functioning due to a faulty component. This limit is based on the maximum normal mode COMP voltage.

If the output current exceeds the current limit threshold or the output voltage is outside the PWRGD range, the SS pin is discharged by an internal sink current of 2 μA. A comparator monitors the SS pin voltage and shuts off the controller when the voltage drops to less than about 1.65 V. Because the voltage ramp (2.9 V − 1.65 V = 1.25 V) and the discharge current (2 μA) are internally fixed, the current limit latch-off delay time is determined by the external SS pin capacitor selection.

Figure 28 shows how the ADP3208 reacts to a current overload.

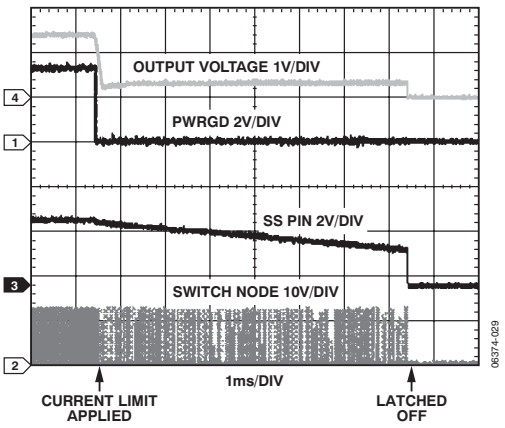


Figure 28. Current Overload

The controller cycles the phases during the latch-off delay time. If the current overload is removed and the PWRGD is recovered before the 1.65 V threshold is reached, the controller resumes normal operation and the SS pin voltage recovers to a 2.9 V clamp level.

The latch-off function can be reset either by removing and reapplying VCC or by briefly cycling the EN pin low and high. To disable the current limit latch-off function, an external pull-up resistor can be tied from the SS pin to the VCC rail. The pull-up current must override the 2 μA sink current of the SS pin to prevent the SS capacitor from discharging to a voltage level that is less than the 1.65 V latch-off threshold.

CHANGING VID ON THE FLY

The ADP3208 is designed to track dynamically changing VID code. As a consequence, the CPU VCC voltage can change without the need to reset the controller or the CPU. This concept is commonly referred to as VID on-the-fly (VID OTF) transient. A VID OTF can occur with either light or heavy load conditions. The processor alerts the controller that a VID change is occurring by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes, the ADP3208 detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7-bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 6, during a VID transient, the ADP3208 forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual-phase controller but is running in single-phase mode due to a light load condition, a current overload event causes the chip to switch to dual-phase mode to share the excessive load until the delayed current limit latch-off cycle terminates.

In user-set single-phase mode, the ADP3208 usually runs in RPM mode. When a VID transition occurs, however, the ADP3208 switches to dual-phase PWM mode.

Light Load RPM DCM Operation

In single-phase normal mode, DPRSLP is pulled low and the APD3208 operates in continuous conduction mode (CCM) over the entire load range. The upper and lower MOSFETs run synchronously and in complementary phase. See Figure 29 for the typical waveforms of the ADP3208 running in CCM with a 7 A load current.

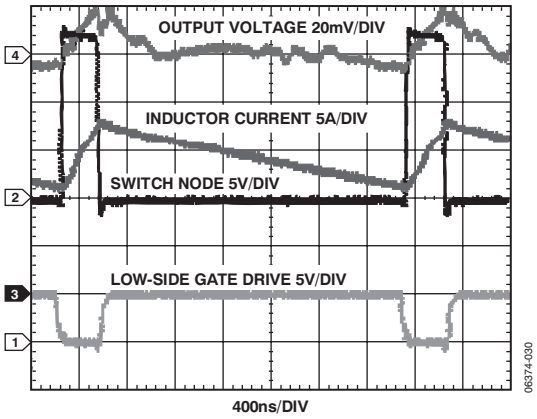


Figure 29. Single-Phase Waveforms in CCM

If DPRSLP is pulled high, the ADP3208 operates in RPM mode. If the load condition is light, the chip enters discontinuous conduction mode (DCM). Figure 30 shows a typical single-phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 31 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 32 the high-side FET is off and the low-side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high- and low-side FETs are off and no current flows into the inductor (see Figure 33). Figure 34 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3208 monitors the switch node voltage to determine when to turn off the low-side FET. Figure 35 shows a typical waveform in DCM with a 1 A load current. Between t_1 and t_2, the inductor current ramps down. The current flows through the source drain of the low-side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t_2. When the switch voltage is approximately −6 mV, the low-side FET is turned off.

Figure 34 shows a small, dampened ringing at t_2. This is caused by the LC created from capacitance on the switch node, including the C_{DS} of the FETs and the output inductor. This ringing is normal.

The ADP3208 automatically goes into DCM with a light load. Figure 35 shows the typical DCM waveform of the ADP3208. As the load increases, the ADP3208 enters into CCM. In DCM, frequency decreases with load current. Figure 36 shows switching frequency vs. load current for a typical design. In DCM, switching frequency is a function of the inductor, load current, input voltage, and output voltage.

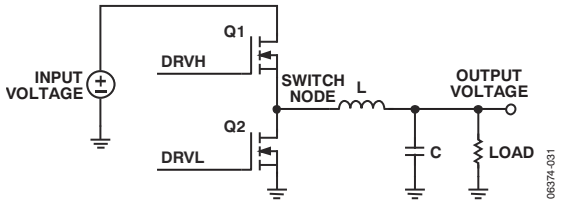


Figure 30. Buck Topology

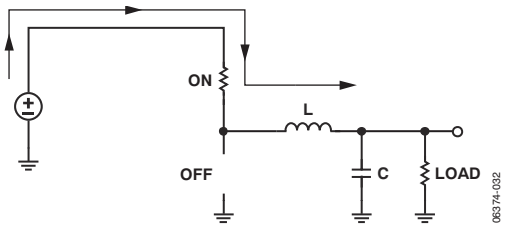


Figure 31. Buck Topology Inductor Current During t_0 and t_1

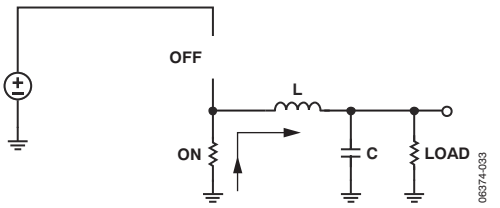


Figure 32. Buck Topology Inductor Current During t_1 and t_2

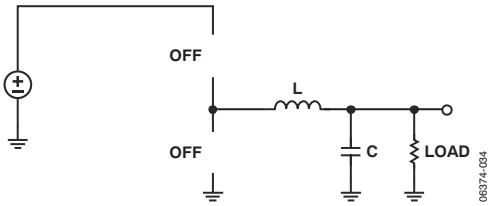


Figure 33. Buck Topology Inductor Current During t_2 and t_3

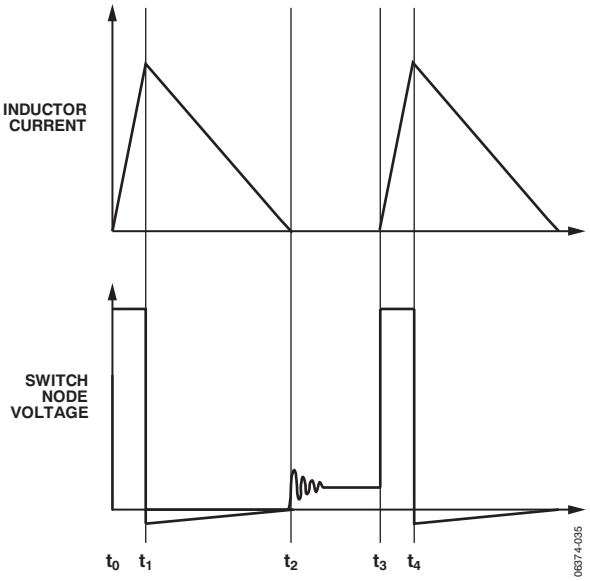


Figure 34. Inductor Current and Switch Node in DCM

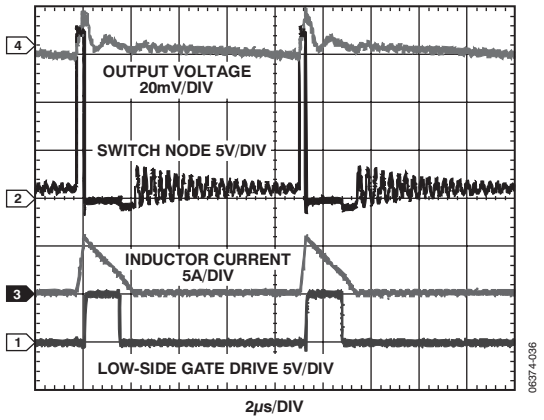


Figure 35. Single-Phase Waveforms in DCM with 1 A Load Current

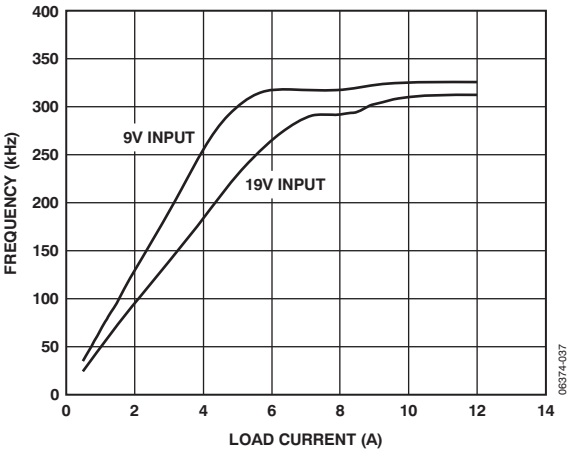


Figure 36. Single-Phase CCM/DCM Frequency vs. Load Current

OUTPUT CROWBAR

To prevent the CPU and other external components from damage due to overvoltage, the ADP3208 turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.7 V typical).

Turning on the low-side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain-source short of the high-side MOSFET, turning on the low-side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the ADP3208 is latched off. The latch-off function can be reset by removing and reapplying VCC to the ADP3208 or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

REVERSE VOLTAGE PROTECTION

Very large reverse current in inductors can cause negative V_{CORE} voltage, which is harmful to the CPU and other output components. The ADP3208 provides a reverse voltage protection (RVP) function without additional system cost. The V_{CORE} voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the ADP3208 triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2 low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built-up energy in the inductor into the input dc voltage source via the forward-biased body diode of the high-side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −100 mV.

Sometimes the crowbar feature inadvertently causes output reverse voltage because turning on the low-side MOSFETs results in a very large reverse inductor current. To prevent damage to the CPU caused from negative voltage, the ADP3208 maintains its RVP monitoring function even after OVP latch-off. During OVP latch-off, if the CSREF pin voltage drops to less than −300 mV, the low-side MOSFETs is turned off. DRVL outputs are allowed to turn back on when the CSREF voltage recovers to greater than −100 mV.

OUTPUT ENABLE AND UVLO

For the ADP3208 to begin switching, the VCC supply voltage to the controller must be greater than the V_{CCOK} threshold and the EN pin must be driven high. If the VCC voltage is less than the V_{CCUVLO} threshold or the EN pin is a logic low, the ADP3208 shuts off. In shutdown mode, the controller holds the PWM outputs low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives the DRVH and DRVL outputs low.

The user must adhere to proper power-supply sequencing during startup and shutdown of the ADP3208. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

THERMAL THROTTLING CONTROL

The ADP3208 includes a thermal monitoring circuit to detect whether the temperature of the VR has exceeded a user-defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the VCC pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSNS pin. An internal comparator circuit compares the TTSNS voltage to half the VCC threshold and outputs a logic level signal at the VRTT output when the temperature trips the user-set alarm threshold. The VRTT output is designed to drive an external transistor that in turn provides the high current, open-drain VRTT signal required by the IMVP-6+ specification.

The internal VRTT comparator has a hysteresis of approximately 100 mV to prevent high frequency oscillation of VRTT when the temperature approaches the set alarm point.

POWER MONITOR FUNCTION

The ADP3208 includes a power monitor. The circuit creates the product of the output voltage and the output current. The multiplication is done by converting the differential current sense signal from CSCOMP to CSREF into a pulse-modulated periodic signal stream and then scaling that signal with the output voltage. The duty cycle of the pulse-modulated PMON signal is proportional to the current, and the amplitude is proportional to the voltage. The maximum load current that corresponds to the full-scale (100%) modulated signal can be adjusted by a resistor, R_{PMONFS}, tied from PMONFS to GND. R_{PMONFS} also affects the clock frequency of the PWM circuit. An RC low-pass filter connected to the PMON output demodulates the PWM pulse stream and creates averaged output current or power information, depending on which rail the open-drain PMON output is pulled up to.

If PMON is pulled up to a dc voltage, the RC-filtered voltage is proportional to the averaged load current. Figure 37 shows the PMON configuration used to monitor load current.

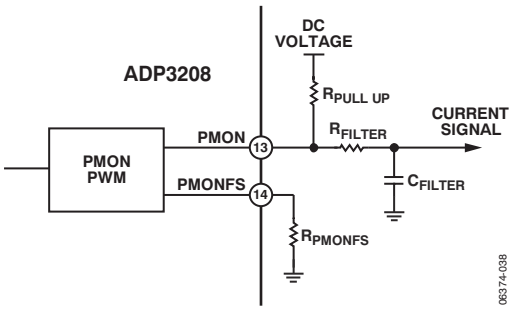


Figure 37. PMON Current Monitor Configuration

If PMON is pulled up to the converter output node, the demodulated voltage becomes proportional to the averaged power (see Figure 38).

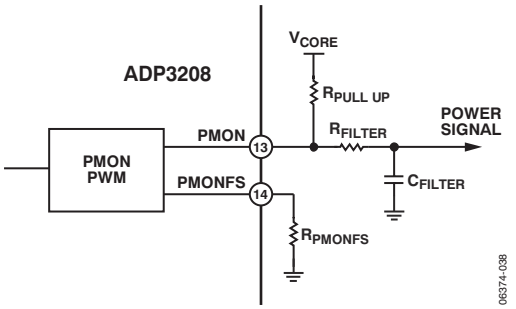


Figure 38. PMON Power Monitor Configuration

Table 6. VID Codes

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	0	0	0	0	0	0	1.5000 V
0	0	0	0	0	0	1	1.4875 V
0	0	0	0	0	1	0	1.4750 V
0	0	0	0	0	1	1	1.4625 V
0	0	0	0	1	0	0	1.4500 V
0	0	0	0	1	0	1	1.4375 V
0	0	0	0	1	1	0	1.4250 V
0	0	0	0	1	1	1	1.4125 V
0	0	0	1	0	0	0	1.4000 V
0	0	0	1	0	0	1	1.3875 V
0	0	0	1	0	1	0	1.3750 V
0	0	0	1	0	1	1	1.3625 V
0	0	0	1	1	0	0	1.3500 V
0	0	0	1	1	0	1	1.3375 V
0	0	0	1	1	1	0	1.3250 V
0	0	0	1	1	1	1	1.3125 V
0	0	1	0	0	0	0	1.3000 V
0	0	1	0	0	0	1	1.2875 V
0	0	1	0	0	1	0	1.2750 V
0	0	1	0	0	1	1	1.2625 V
0	0	1	0	1	0	0	1.2500 V
0	0	1	0	1	0	1	1.2375 V
0	0	1	0	1	1	0	1.2250 V
0	0	1	0	1	1	1	1.2125 V
0	0	1	1	0	0	0	1.2000 V
0	0	1	1	0	0	1	1.1875 V
0	0	1	1	0	1	0	1.1750 V
0	0	1	1	0	1	1	1.1625 V
0	0	1	1	1	0	0	1.1500 V
0	0	1	1	1	0	1	1.1375 V
0	0	1	1	1	1	0	1.1250 V
0	0	1	1	1	1	1	1.1125 V
0	1	0	0	0	0	0	1.1000 V
0	1	0	0	0	0	1	1.0875 V
0	1	0	0	0	1	0	1.0750 V
0	1	0	0	0	1	1	1.0625 V
0	1	0	0	1	0	0	1.0500 V
0	1	0	0	1	0	1	1.0375 V
0	1	0	0	1	1	0	1.0250 V
0	1	0	0	1	1	1	1.0125 V
0	1	0	1	0	0	0	1.0000 V
0	1	0	1	0	0	1	0.9875 V
0	1	0	1	0	1	0	0.9750 V
0	1	0	1	0	1	1	0.9625 V
0	1	0	1	1	0	0	0.9500 V
0	1	0	1	1	0	1	0.9375 V
0	1	0	1	1	1	0	0.9250 V
0	1	0	1	1	1	1	0.9125 V
0	1	1	0	0	0	0	0.9000 V
0	1	1	0	0	0	1	0.8875 V
0	1	1	0	0	1	0	0.8750 V
0	1	1	0	0	1	1	0.8625 V
0	1	1	0	1	0	0	0.8500 V
0	1	1	0	1	0	1	0.8375 V
0	1	1	0	1	1	0	0.8250 V
0	1	1	0	1	1	1	0.8125 V
0	1	1	1	0	0	0	0.8000 V
0	1	1	1	0	0	1	0.7875 V
0	1	1	1	0	1	0	0.7750 V
0	1	1	1	0	1	1	0.7625 V
0	1	1	1	1	0	0	0.7500 V
0	1	1	1	1	0	1	0.7375 V
0	1	1	1	1	1	0	0.7250 V
0	1	1	1	1	1	1	0.7125 V
1	0	0	0	0	0	0	0.7000 V
1	0	0	0	0	0	1	0.6875 V
1	0	0	0	0	1	0	0.6750 V
1	0	0	0	0	1	1	0.6625 V
1	0	0	0	1	0	0	0.6500 V
1	0	0	0	1	0	1	0.6375 V
1	0	0	0	1	1	0	0.6250 V
1	0	0	0	1	1	1	0.6125 V
1	0	0	1	0	0	0	0.6000 V
1	0	0	1	0	0	1	0.5875 V
1	0	0	1	0	1	0	0.5750 V
1	0	0	1	0	1	1	0.5625 V
1	0	0	1	1	0	0	0.5500 V
1	0	0	1	1	0	1	0.5375 V
1	0	0	1	1	1	0	0.5250 V
1	0	0	1	1	1	1	0.5125 V
1	0	1	0	0	0	0	0.5000 V
1	0	1	0	0	0	1	0.4875 V
1	0	1	0	0	1	0	0.4750 V
1	0	1	0	0	1	1	0.4625 V
1	0	1	0	1	0	0	0.4500 V
1	0	1	0	1	0	1	0.4375 V
1	0	1	0	1	1	0	0.4250 V
1	0	1	0	1	1	1	0.4125 V
1	0	1	1	0	0	0	0.4000 V
1	0	1	1	0	0	1	0.3875 V
1	0	1	1	0	1	0	0.3750 V
1	0	1	1	0	1	1	0.3625 V
1	0	1	1	1	0	0	0.3500 V
1	0	1	1	1	0	1	0.3375 V
1	0	1	1	1	1	0	0.3250 V
1	0	1	1	1	1	1	0.3125 V
1	1	0	0	0	0	0	0.3000 V
1	1	0	0	0	0	1	0.2875 V
1	1	0	0	0	1	0	0.2750 V
1	1	0	0	0	1	1	0.2625 V
1	1	0	0	1	0	0	0.2500 V
1	1	0	0	1	0	1	0.2375 V
1	1	0	0	1	1	0	0.2250 V
1	1	0	0	1	1	1	0.2125 V
1	1	0	1	0	0	0	0.2000 V
1	1	0	1	0	0	1	0.1875 V
1	1	0	1	0	1	0	0.1750 V
1	1	0	1	0	1	1	0.1625 V
1	1	0	1	1	0	0	0.1500 V
1	1	0	1	1	0	1	0.1375 V
1	1	0	1	1	1	0	0.1250 V
1	1	0	1	1	1	1	0.1125 V
1	1	1	0	0	0	0	0.1000 V
1	1	1	0	0	0	1	0.0875 V
1	1	1	0	0	1	0	0.0750 V
1	1	1	0	0	1	1	0.0625 V
1	1	1	0	1	0	0	0.0500 V
1	1	1	0	1	0	1	0.0375 V
1	1	1	0	1	1	0	0.0250 V
1	1	1	0	1	1	1	0.0125 V
1	1	1	1	0	0	0	0.0000 V
1	1	1	1	0	0	1	0.0000 V
1	1	1	1	0	1	0	0.0000 V
1	1	1	1	0	1	1	0.0000 V
1	1	1	1	1	0	0	0.0000 V
1	1	1	1	1	0	1	0.0000 V
1	1	1	1	1	1	0	0.0000 V
1	1	1	1	1	1	1	0.0000 V

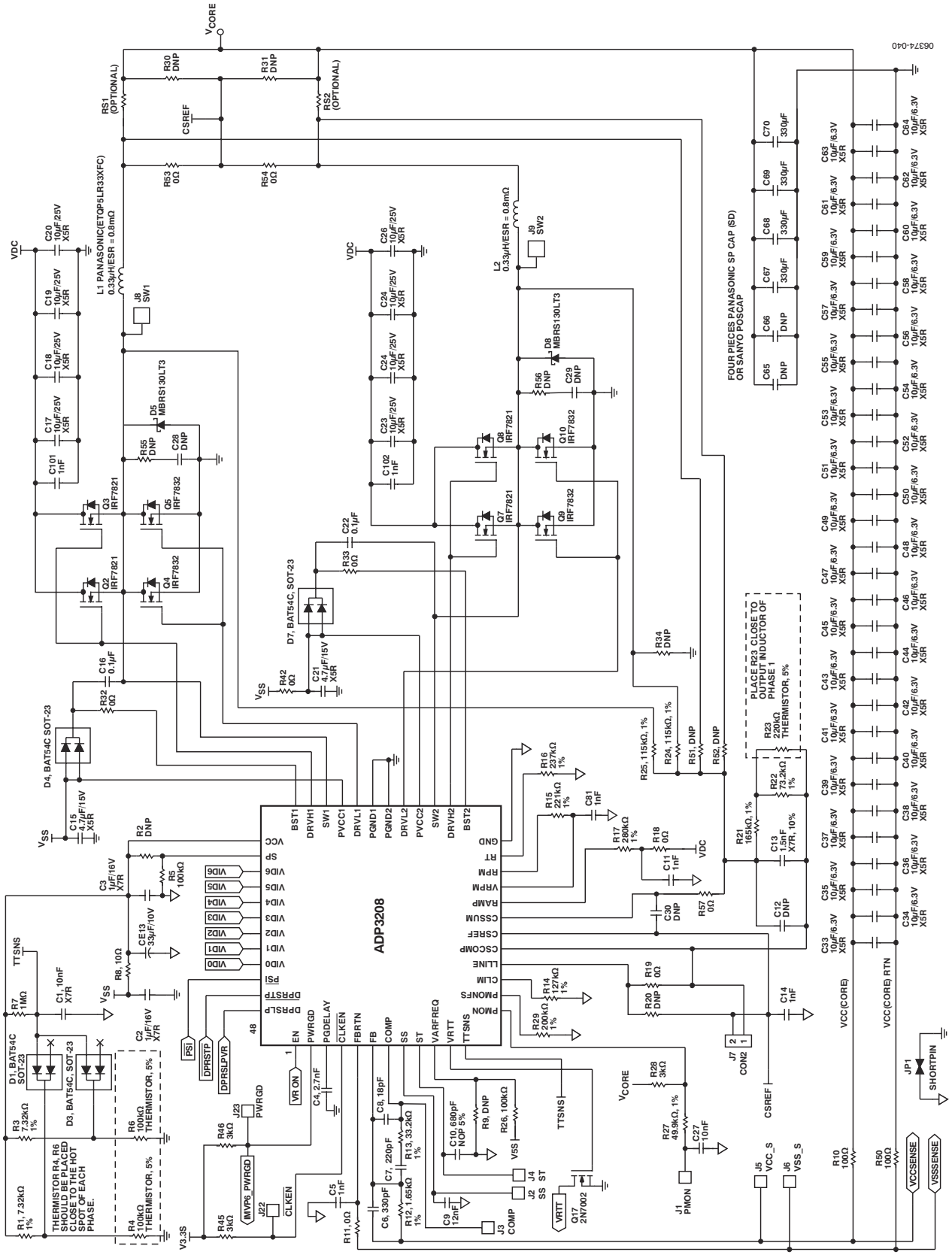


Figure 39. Typical Dual-Phase Application Circuit

APPLICATION INFORMATION

The design parameters for a typical IMVP-6+-compliant CPU core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8 V
- Output voltage by VID setting (V_{VID}) = 1.4375 V
- Maximum output current (I_O) = 40 A
- Droop resistance (R_O) = 2.1 mΩ
- Nominal output voltage at 40 A load (V_{OFL}) = 1.3535 V
- Static output voltage drop from no load to full load (ΔV) = $V_{ONL} - V_{OFL}$ = 1.4375 V − 1.3535 V = 84 mV
- Maximum output current step (ΔI_O) = 27.9 A
- Number of phases (n) = 2
- Switching frequency per phase (f_{SW}) = 300 kHz
- Duty cycle at maximum input voltage (D_{MAX}) = 0.18 V
- Duty cycle at minimum input voltage (D_{MIN}) = 0.076 V

SETTING THE CLOCK FREQUENCY FOR PWM

In PWM operation, the ADP3208 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For a dual-phase design, a clock frequency of 600 kHz sets the switching frequency to 300 kHz per phase. This selection represents the trade-off between the switching losses and the minimum sizes of the output filter components. To achieve a 600 kHz oscillator frequency at a VID voltage of 1.5 V, RT must be 250 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$RT = \frac{V_{VID} + 1.0\ \text{V}}{2 \times n \times f_{SW} \times 7.2\ \text{pF}} - 35\ \text{k}\Omega \quad (1)$$

where:
7.2 pF and 35 kΩ are internal IC component values.
V_{VID} is the VID voltage in volts.
n is the number of phases.
f_{SW} is the switching frequency in hertz for each phase.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

SETTING THE SWITCHING FREQUENCY FOR RPM OPERATION OF PHASE 1

During the RPM operation of Phase 1, the ADP3208 runs in pseudoconstant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner.

To save power with light loads, lower switching frequency is usually preferred during RPM operation. However, the V_{CORE} ripple specification of IMVP-6+ sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor between the VRPM and RPM pins sets the pseudo-constant frequency as follows:

$$R_{RPM} = \frac{4 \times RT}{(V_{VID} + 1.0\ \text{V})} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (2)$$

where:
A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMP pin to set the internal ramp magnitude (see the Ramp Resistor Selection section for information about the design of R_R resistance).

If R_R = 280 kΩ, the following resistance results in 300 kHz switching frequency in RPM operation.

$$R_{RPM} = \frac{4 \times 237\ \text{k}\Omega}{1.4375\ \text{V} + 1.0\ \text{V}} \times \frac{0.2 \times (1 - 0.076) \times 1.4375}{280\ \text{k}\Omega \times 5\ \text{pF} \times 300\ \text{kHz}} = 246\ \text{k}\Omega$$

SOFT START AND CURRENT LIMIT LATCH-OFF DELAY TIMES

The soft start and current limit latch-off delay functions share the SS pin; consequently, these parameters must be considered together. First, set C_{SS} for the soft start ramp. This ramp is generated with an 8 µA internal current source. The value for C_{SS} can be calculated as

$$C_{SS} = \frac{8\ \mu\text{A} \times t_{SS}}{V_{BOOT}} \quad (3)$$

where:
V_{BOOT} is the boot voltage for the CPU and is defined in IMVP-6+ as 1.2 V.
t_{SS} is the desired soft start time and is recommended in IMVP-6+ to be less than 3 ms.

Therefore, assuming a desired soft start time of 2 ms, C_{SS} is 13.3 nF, and the closest standard capacitance is 12 nF.

After C_{SS} is set, the current limit latch-off time can be calculated by using the following equation:

$$t_{DELAY} = \frac{1.2\ \text{V} \times C_{SS}}{2\ \mu\text{A}} \quad (4)$$

where C_{SS} is 7.2 ms.

PWRGD DELAY TIMER

The PWRGD delay, t_{CPU_PWRGD}, is defined in IMVP-6+ as the period between the CLKEN assertion and the PWRGD assertion. It is programmed by a capacitor connected to the PGDELAY pin and calculated as follows:

$$C_{PGDELAY} = \frac{2\ \mu A \times t_{CPU_PWRGD}}{2.9\ V} \quad (5)$$

IMVP-6+ specifies that the PWRGD delay is between 3 ms and 20 ms. Assuming a 5 ms PWRGD delay, $C_{PGDELAY}$ is 4.7 nF.

INDUCTOR SELECTION

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller-size inductors, and for a specified peak-to-peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. For a multiphase converter, the practical value for peak-to-peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 6 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current. Equation 7 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad (6)$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - (n \times D_{MIN})) \times (1 - D_{MIN})}{f_{SW} \times V_{RIPPLE}} \quad (7)$$

Solving Equation 7 for a 16 mV peak-to-peak output ripple voltage yields

$$L \geq \frac{1.4375\ V \times 2.1\ m\Omega \times (1 - 2 \times 0.076)(1 - 0.076)}{300\ kHz \times 16\ mV} = 493\ nH$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 490 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 9.0 A. The inductor should not saturate at the peak current of 24.5 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (20 A) plus the ac core loss. In this example, 330 nH is used.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 0.8 mΩ is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface-mount power inductors optimized for high power applications upon request:

- Vishay Dale Electronics, Inc.
  (605) 665-9301
- Panasonic
  (714) 373-7334
- Sumida Electric Company
  (847) 545-6700
- NEC Tokin Corporation
  (510) 324-4110

Output Droop Resistance

The design requires that the regulator output voltage measured at the CPU pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance (R_O).

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low-pass filter. The summing is implemented by the CS amplifier that is configured with resistor $R_{PH(x)}$ (summer) and resistors R_{CS} and C_{CS} (filters). The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_{SENSE} \quad (8)$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad (9)$$

where R_{SENSE} is the DCR of the output inductors.

Either R_{CS} or $R_{PH(x)}$ can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the R_{CS} resistance should be greater than 100 kΩ. For example, initially select R_{CS} to be equal to 200 kΩ, and then use Equation 9 to solve for C_{CS}:

$$C_{CS} = \frac{330\ nH}{0.8\ m\Omega \times 200\ k\Omega} = 2.1\ nF$$

If C_{CS} is not a standard capacitance, R_{CS} can be tuned. For example, if the optimal C_{CS} capacitance is 1.5 nF, adjust R_{CS} to 280 kΩ. For best accuracy, C_{CS} should be a 5% NPO capacitor. In this example, a 220 kΩ is used for R_{CS} to achieve optimal results.

Next, solve for $R_{PH(x)}$ by rearranging Equation 8 as follows:

$$R_{PH(x)} \geq \frac{0.8\ \text{m}\Omega}{2.1\ \text{m}\Omega} \times 220\ \text{k}\Omega = 83.8\ \text{k}\Omega$$

The standard 1% resistor for $R_{PH(x)}$ is 86.6 kΩ.

Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors R_{CS1} and R_{CS2} (see Figure 40) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

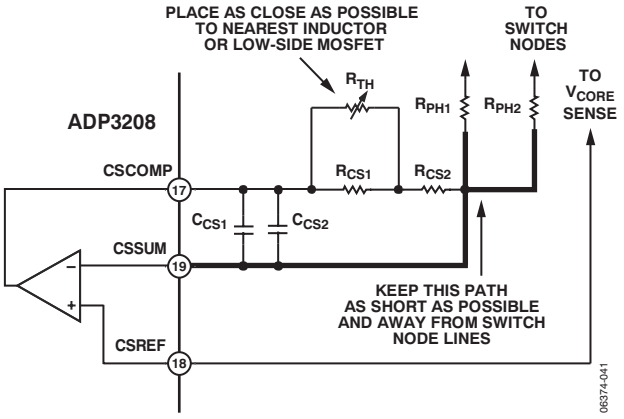


Figure 40. Temperature-Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to R_{CS} and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is R_{TH}(50°C)/R_{TH}(25°C)) and B (B is R_{TH}(90°C)/R_{TH}(25°C)). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of the two temperatures. The relative value of R_{CS} is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example.
   The relative values are called r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039, T_1 is 50°C, and T_2 is 90°C.
4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} by using the following equations:

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (10)$$

$$r_{CS1} = \frac{(1-A)}{\dfrac{1}{1-r_{CS2}} - \dfrac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\dfrac{1}{1-r_{CS2}} - \dfrac{1}{r_{CS1}}}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (11)$$

6. Calculate values for R_{CS1} and R_{CS2} by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (12)$$
$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2}))$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603-size thermistor with a value close to R_{CS} is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, r_{CS1} is 0.359, r_{CS2} is 0.729, and r_{TH} is 1.094. Solving for r_{TH} yields 241 kΩ, so a thermistor of 220 kΩ would be a reasonable selection, making k equal to 0.913. Finally, R_{CS1} and R_{CS2} are found to be 72.1 kΩ and 166 kΩ. Choosing the closest 1% resistor for R_{CS2} yields 165 kΩ. To correct for this approximation, 73.3 kΩ is used for R_{CS1}.

C_{OUT} SELECTION

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance (C_Z). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the physical limit is twenty 0805-size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 200 µF to 300 µF is recommended and is usually composed of multiple 10 µF or 22 µF capacitors.

Ensure that the total amount of bulk capacitance (C_X) is within its limits. The upper limit is dependent on the VID on-the-fly output voltage stepping (voltage step, V_V, in time, t_V, with error of V_{ERR}); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step, ΔI_O. The current version of the IMVP-6+ specification allows a maximum V_{CORE} overshoot (V_{OSMAX}) of 10 mV more than the VID voltage for a step-off load current.

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right) \quad (13)$$

$$C_{X(MAX)} \leq \frac{L}{n \times k^2 \times R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{n \times k \times R_O}{L} \right)^2} - 1 \right) - C_Z$$

$$\text{where } k = -\ln\left(\frac{V_{ERR}}{V_V} \right) \quad (14)$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not meet the VID on-the-fly and/or the deeper sleep exit specifications and may require less inductance or more phases. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if 30 pieces of 10 µF, 0805-size MLC capacitors (C_Z = 300 µF) are used, the fastest VID voltage change is when the device exits deeper sleep, during which the V_{CORE} change is 220 mV in 22 µs with a setting error of 10 mV. If k = 3.1, solving for the bulk capacitance yields

$$C_{X(MIN)} \geq \left(\frac{330\text{ nH} \times 27.9\text{ A}}{2 \times \left(2.1\text{ m}\Omega + \frac{10\text{ mV}}{27.9\text{ A}} \right) \times 1.4375\text{ V}} - 300\ \mu\text{F} \right) = 1.0\text{ mF}$$

$$C_{X(MAX)} \leq \frac{330\text{ nH} \times 220\text{ mV}}{2 \times 3.1^2 \times (2.1\text{ m}\Omega)^2 \times 1.4375\text{ V}} \times$$

$$\left(\sqrt{1 + \left(\frac{22\ \mu\text{s} \times 1.4375\text{ V} \times 2 \times 3.1 \times 2.1\text{ m}\Omega}{220\text{ mV} \times 490\text{ nH}} \right)^2} - 1 \right) - 300\ \mu\text{F}$$

= 21 mF

Using six 330 µF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields C_X = 1.98 mF and R_X = 1.2 mΩ.

Ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using

$$L_X \leq C_Z \times R_O{}^2 \times Q^2 \quad (15)$$

$$L_X \leq 300\ \mu\text{F} \times (2.1\text{ m}\Omega)^2 \times 2 = 2\text{ nH}$$

where:
Q is limited to the square root of 2 to ensure a critically damped system.
L_X is about 150 pH for the six SP capacitors, which is low enough to avoid ringing during a load change. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multimode control technique, an all ceramic capacitor design can be used if the conditions of Equations 13, 14, and 15 are satisfied.

POWER MOSFETS

For typical 20 A per phase applications, the N-channel power MOSFETs are selected for two high-side switches and two or three low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5 V, logic-level threshold MOSFETs must be used.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. In the ADP3208, currents are balanced between phases; the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the average total output current (I_O):

$$P_{SF} = (1-D)\times\left[\left(\frac{I_O}{n_{SF}}\right)^2 + \frac{1}{12}\times\left(\frac{n\times I_R}{n_{SF}}\right)^2\right]\times R_{DS(SF)} \qquad (16)$$

where:
D is the duty cycle and is approximately the output voltage divided by the input voltage.
I_R is the inductor peak-to-peak ripple current and is approximately

$$I_R = \frac{(1-D)\times V_{OUT}}{L\times f_{SW}}$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required $R_{DS(ON)}$ for the MOSFET. For 8-lead SOIC or 8-lead SOIC-compatible MOSFETs, the junction-to-ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for P_{SF} is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (40 A maximum), the $R_{DS(SF)}$ per MOSFET is less than 8.5 mΩ for two pieces of low-side MOSFETs. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 6 mΩ at room temperature, or 8.5 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high-side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2\times f_{SW}\times\frac{V_{DC}\times I_O}{n_{MF}}\times R_G\times\frac{n_{MF}}{n}\times C_{ISS} \qquad (17)$$

where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance.
C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D\times\left[\left(\frac{I_O}{n_{MF}}\right)^2 + \frac{1}{12}\times\left(\frac{n\times I_R}{n_{MF}}\right)^2\right]\times R_{DS(MF)} \qquad (18)$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8-lead SOIC) when combining the switching and conduction losses.

For example, an IRF7821 device can be selected as the main MOSFET (four in total; that is, n_{MF} = 4), with approximately C_{ISS} = 1010 pF (maximum) and $R_{DS(MF)}$ = 18 mΩ (maximum at T_J = 120°C), and an IR7832 device can be selected as the synchronous MOSFET (four in total; that is, n_{SF} = 4), with $R_{DS(SF)}$ = 6.7 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 40 A and I_R = 9.0 A yields 630 mW for each synchronous MOSFET and 590 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2\times n}\times\left(n_{MF}\times Q_{GMF} + n_{SF}\times Q_{GSF}\right) + I_{CC}\right]\times VCC \qquad (19)$$

where Q_{GMF} is the total gate charge for each main MOSFET, and Q_{GSF} is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation (I_{CC} times the VCC) of the driver.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use the following expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (20)$$

$$R_R = \frac{0.2 \times 330\ \text{nH}}{3 \times 5 \times 3.4\ \text{m}\Omega \times 5\ \text{pF}} = 256\ \text{k}\Omega$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 21). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of R_R in this example is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (21)$$

$$V_R = \frac{0.2 \times (1 - 0.076) \times 1.3475\ \text{V}}{280\ \text{k}\Omega \times 5\ \text{pF} \times 300\ \text{kHz}} = 0.59\ \text{V}$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 20, the factor of 3 sets the minimum ramp size that produces an optimal combination of good stability, transient response, and thermal balance.

COMP PIN RAMP

In addition to the internal ramp, there is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad (22)$$

where C_X is the total bulk capacitance, and R_O is the droop resistance of the regulator.

For this example, the overall ramp signal is 1.85 V.

CURRENT LIMIT SETPOINT

To select the current limit setpoint, the resistor value for R_{CLIM} must be determined. The current limit threshold for the ADP3208 is set with R_{CLIM}. R_{CLIM} can be found using the following equation:

$$R_{CLIM} = \frac{R_{CS} \times 10 \times R_{SENSE} \times I_{CLIM} \times 2}{R_{PH} \times 10\ \mu\text{A} \times n} \quad (23)$$

where:
R_{PH} is the resistor connecting the current sense resistor or inductor switch node to the current sense amplifier.
R_{CS} is the current sense amplifier feedback resistor.
R_{SENSE} is the sense current resistor or the inductor DCR.
n is the number of phases.
I_{CLIM} is the current limit setpoint.

If R_{CLIM} is greater than 500 kΩ, the current limit may be lower than expected and require an adjustment of R_{CLIM}. In this example, I_{CLIM} is the average current limit for the output of the supply. For this example, choosing 60 A for I_{CLIM} results in an R_{CLIM} of 126 kΩ, and the closest 1% standard resistance is 127 kΩ.

The following equation determines the per phase current limit previously described:

$$I_{PHLIM} = \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} - \frac{I_R}{2} \quad (24)$$

where:
$V_{COMP(MAX)}$ is the maximum COMP voltage and is 3.3 V.
V_{BIAS} is the COMP pin bias voltage and is 1.0 V.
A_D is the current-balancing amplifier gain and is 5.

Using a V_R of 0.59 V and a $R_{DS(MAX)}$ of 3.8 mΩ (low-side on resistance at 150°C) results in a per phase limit of 83 A. Although this number may seem high, this current level can be achieved using only an absolute short at the output, and the current limit latch-off function shuts down the regulator before overheating can occur.

This limit can be adjusted by changing the ramp voltage, V_R. However, the per phase limit must be set to be greater than the average per phase current (I_{CLIM}/n).

There is also a per phase initial duty cycle limit at the maximum input voltage:

$$D_{LIM} = D_{MIN} \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_R} \quad (25)$$

For this example, the duty cycle limit at the maximum input voltage is 0.3 V when D is 0.076.

POWER MONITOR

The PMON duty cycle is proportional to the load current. R_{PMONFS} sets the maximum duty cycle at the maximum current.

$$R_{PMONFS} = \frac{(I_{LOAD} \times R_O \times 9) + 1\,\text{V}}{10\,\mu\text{A}} \quad (26)$$

where I_{LOAD} is the load current in amps when PMON is 100% duty cycle, and R_O is the droop resistance in ohms.

When PMON is connected with a pull-up resistor to the output voltage, as shown in Figure 38, the average PMON voltage is given by

$$PMON = \frac{V_{GFX} \times I_{LOAD} \times R_O \times 9}{(R_{MONFS} \times 10\,\mu\text{A}) - 1\,\text{V}} \quad (27)$$

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3208 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multimode feedback structure of the ADP3208, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 41 shows the Type III amplifier used in the ADP3208. Figure 42 shows the locations of the two poles and two zeros created by this amplifier.

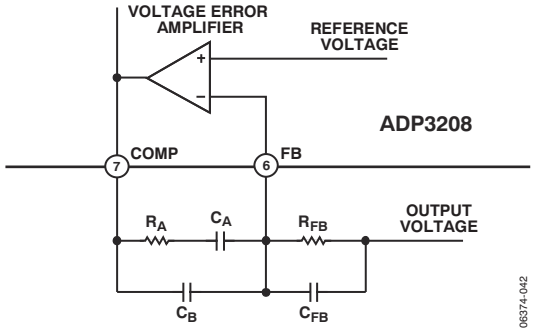


Figure 41. Voltage Error Amplifier

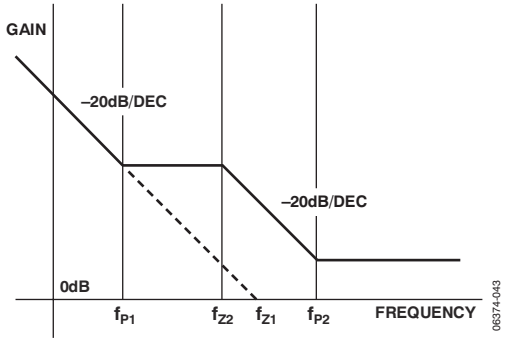


Figure 42. Poles and Zeros of Voltage Error Amplifier

The following equations give the locations of the poles and zeros shown in Figure 42:

$$f_{Z1} = \frac{1}{2\pi \times C_A \times R_A} \quad (28)$$

$$f_{Z2} = \frac{1}{2\pi \times C_{FB} \times R_{FB}} \quad (29)$$

$$f_{P1} = \frac{1}{2\pi (C_A + C_B) \times R_{FB}} \quad (30)$$

$$f_{P2} = \frac{C_A + C_B}{2\pi \times R_A \times C_B \times C_A} \quad (31)$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for ADP3208 section):

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - (n \times D)) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad (32)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad (33)$$

$$T_B = (R_X + R' - R_O) \times C_X \quad (34)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times R_E} \quad (35)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad (36)$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8-layer motherboard).

R_{DS} is the total low-side MOSFET for on resistance per phase.

A_D is 5.

V_{RT} is 1.25 V.

L_X is 150 pH for the six Panasonic SP capacitors.

The compensation values can be calculated as follows:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad (37)$$

$$R_A = \frac{T_C}{C_A} \quad (38)$$

$$C_B = \frac{T_B}{R_B} \quad (39)$$

$$C_{FB} = \frac{T_D}{R_A} \quad (40)$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for ADP3208 section.

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and an amplitude that is one-nth of the maximum output current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current occurs at the lowest input voltage and is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad (41)$$

$$I_{CRMS} = 0.18 \times 40\text{ A} \times \sqrt{\frac{1}{2 \times 0.18} - 1} = 9.6\text{ A}$$

where I_O is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by eight pieces of 10 µF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

SOFT TRANSIENT SETTING

As described in the Theory of Operation section, during the soft transient, the slew rate of the V_{CORE} reference voltage change is controlled by the ST pin capacitance. Because the timing of exiting deeper sleep is critical, the ST pin capacitance is set to satisfy the slew rate for a fast exit of deeper sleep as follows:

$$C_{ST} = \frac{7.5\,\mu\text{A}}{SLEWRATE_{C4E}} \quad (42)$$

where:
7.5 µA is the source/sink current of the ST pin.
$SLEWRATE_{C4E}$ is the voltage slew rate for exiting deeper sleep and is defined as 10 mV/µA in the IMVP-6+ specification.
C_{ST} is 750 pF, and the closest standard capacitance is 680 pF.

SELECTING THERMAL MONITOR COMPONENTS

To monitor the temperature of a single-point hot spot, set R_{TTSET1} equal to the NTC thermistor's resistance at the alarm temperature. For example, if the alarm temperature for VRTT is 100°C and a Vishey thermistor (NTHS-0603N011003J) with a resistance of 100 kΩ at 25°C, or 6.8 kΩ at 100°C, is used, the user can set R_{TTSET1} equal to 6.8 kΩ (the R_{TH1} at 100°C).

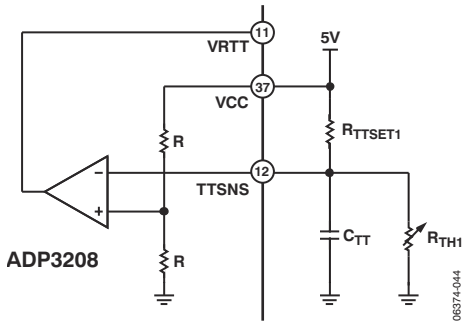


Figure 43. Single-Point Thermal Monitoring

To monitor the temperature of multiple-point hot spots, use the configuration shown in Figure 44. If any of the monitored hot spots reaches the alarm temperature, the VRTT signal is asserted. The following calculation sets the alarm temperature:

$$R_{TTSET1} = \frac{1/2 + \frac{V_{FD}}{V_{REF}}}{1/2 - \frac{V_{FD}}{V_{REF}}} \times R_{TH1AlarmTemperature} \quad (43)$$

where V_{FD} is the forward drop voltage of the parallel diode.

Because the forward current is very small, the forward drop voltage is very low, that is, less than 100 mV. Assuming the same conditions used for the single-point thermal monitoring example—that is, an alarm temperature of 100°C and use of an NTHS-0603N011003J Vishay thermistor—solving Equation 42 gives a R_{TTSET} of 7.37 kΩ, and the closest standard resistor is 7.32 kΩ (1%).

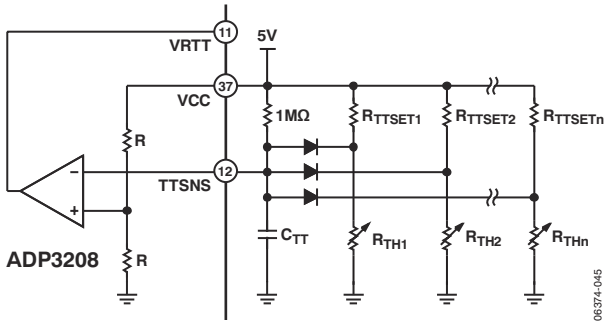


Figure 44. Multiple-Point Thermal Monitoring

The number of hot spots monitored is not limited. The alarm temperature of each hot spot can be individually set by using different values for R_{TTSET1}, R_{TTSET2}, … R_{TTSETn}.

TUNING PROCEDURE FOR ADP3208

Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the ADP3208 and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (V_{FLCOLD}). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot (V_{FLHOT}). If the difference between the two measured voltages is more than a few millivolts, adjust R_{CS2} using Equation 44.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (44)$$

3. Repeat Step 2 until no adjustment of R_{CS2} is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope (R_{OMEAS}).
5. If the difference between R_{OMEAS} and R_O is more than 0.05 mΩ, use the following equation to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (45)$$

6. Repeat Steps 4 and 5 until no adjustment of R_{PH} is needed. Once this is achieved, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 µs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 45. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 45. Do not measure the undershoot or overshoot that occurs immediately after the step.

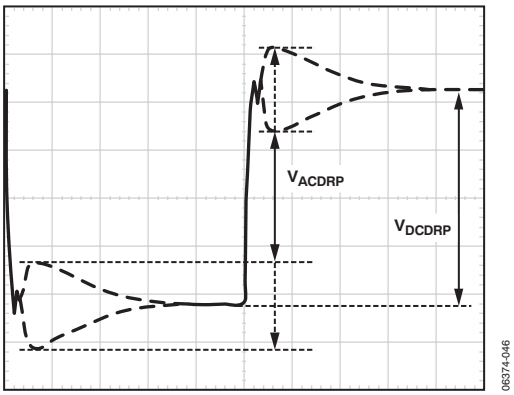


Figure 45. AC Load Line Waveform

6. If the difference between V_{ACDRP} and V_{DCDRP} is more than a couple of millivolts, use Equation 46 to adjust C_{CS}. It may be necessary to try several parallel values to obtain an adequate one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this reason).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (46)$$

7. Repeat Steps 5 and 6 until no adjustment of C_{CS} is needed. Once this is achieved, do not change C_{CS} for the rest of the procedure.
8. Set the dynamic load step to its maximum step size (but do not use a step size that is larger than needed) and verify that the output waveform is square, meaning V_{ACDRP} and V_{DCDRP} are equal.
9. Ensure that the load step slew rate and the power-up slew rate are set to ~150 A/µs to 250 A/µs (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive overshoot at power-up if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

Set the Initial Transient

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 µs/div to 5 µs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after V_{DROOP} (see Figure 46).

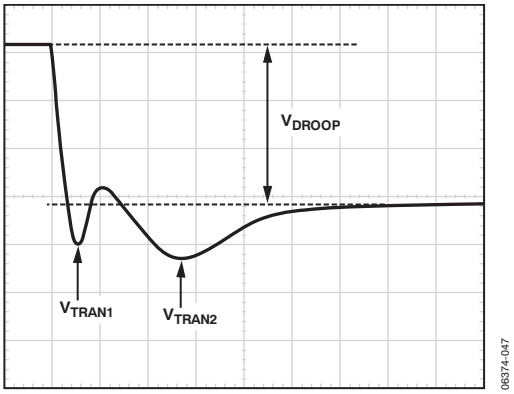


Figure 46. Transient Setting Waveform, Load Step

2. If both overshoots are larger than desired, try the following adjustments in the order shown.
   a. Increase the resistance of the ramp resistor (R_{RAMP}) by 25%.
   b. For V_{TRAN1}, increase C_B or increase the switching frequency.
   c. For V_{TRAN2}, increase R_A by 25% and decrease C_A by 25%.

   If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.
3. For load release (see Figure 47), if $V_{TRANREL}$ is larger than the value specified by IMVP-6+, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

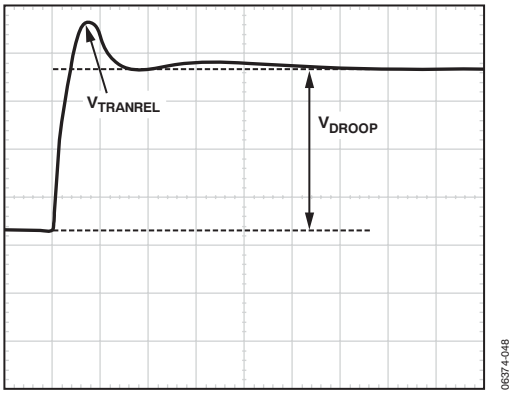


Figure 47. Transient Setting Waveform, Load Release

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the ADP3208) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the ADP3208 for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.
5. The components around the ADP3208 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are those to the FB and CSSUM pins. Refer to Figure 40 for more details on the layout for the CSSUM node.
6. The output capacitors should be connected as close as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
7. Avoid crossing signal lines over the switching power path loop, as described in the Power Circuitry section.

Power Circuitry

1. The switching power path on the PCB should be routed to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power-converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short, wide interconnection traces is especially critical in this

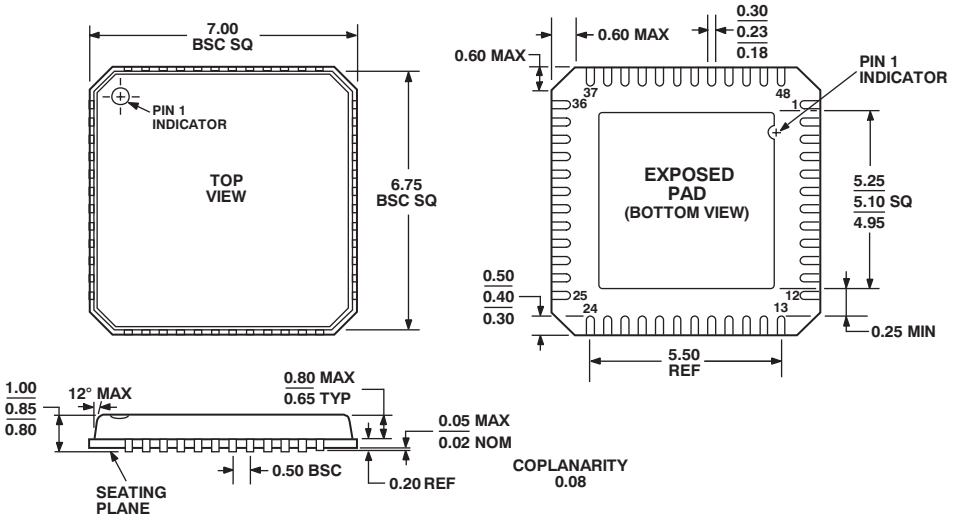
path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

2. When a power-dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer heat to the surrounding air. To achieve optimal thermal dissipation, mirror the pad configurations used to heat sink the MOSFETs on the opposite side of the PCB. In addition, improvements in thermal performance can be obtained using the largest possible pad area.
3. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
4. For best EMI containment, a solid power ground plane should be used as one of the inner layers and extended under all power components.

Signal Circuitry

1. The output voltage is sensed and regulated between the FB and FBRTN pins, and the traces of these pins should be connected to the signal ground of the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be as small as possible. Therefore, the FB and FBRTN traces should be routed adjacent to each other, atop the power ground plane, and back to the controller.
2. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the V_{CORE} common node for the inductors of all the phases.
3. On the back of the ADP3208 package, there is a metal pad that can be used to heat sink the device. Therefore, running vias under the ADP3208 is not recommended because the metal pad may cause shorting between vias.

OUTLINE DIMENSION



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 48. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3208JCPZ-RL[1]	0°C to 100°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1	2,500

[1] Z = RoHS Compliant Part.

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