P4 Series
P4080 multicore processor

Freescale QorIQ™ communications platforms are the next-generation evolution of our leading PowerQUICC® communications processors. Built using high-performance Power Architecture® cores, QorIQ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

QorIQ P4080 Multicore Processor

The QorIQ P4080 multicore processor, the first product offered in the QorIQ P4 platform series, delivers industry-leading performance in the under 30-watt power category. It combines eight Power Architecture e500mc cores operating at frequencies up to 1.5 GHz with high-performance datapath acceleration logic, as well as networking I/O and other peripheral bus interfaces.

The P4080, built in 45 nm technology, is designed to deliver high-performance, next-generation networking services in a very low power envelope.

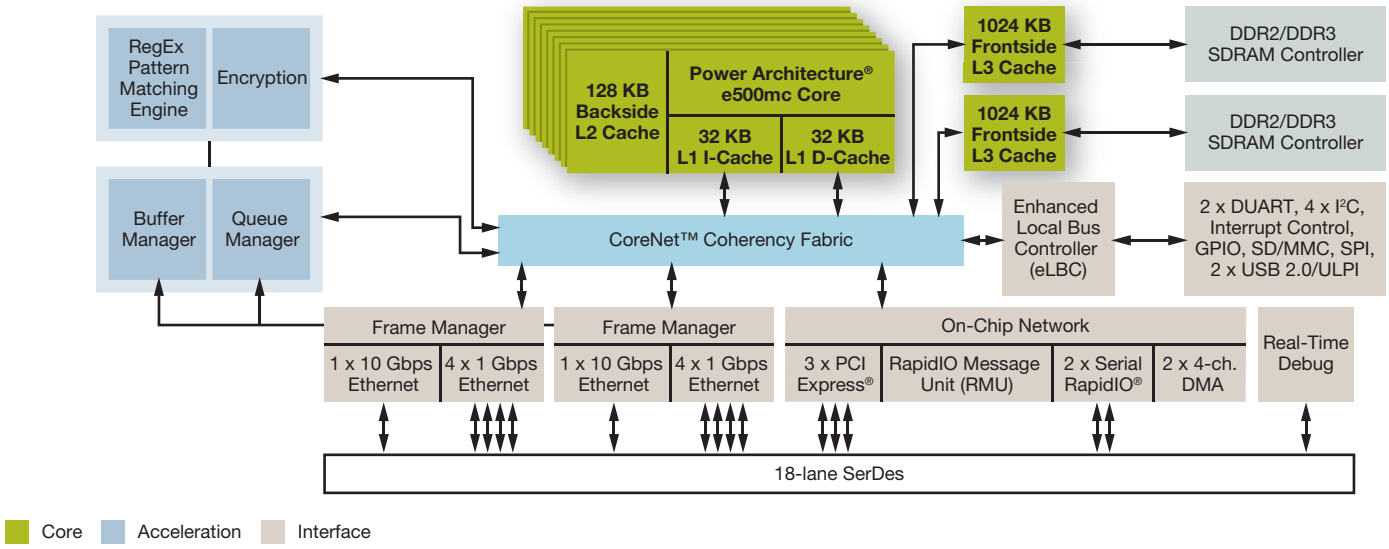
The QorIQ P4080 processor is designed for combined control and dataplane processing, enabling high-performance layers 2–7 processing. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also greatly simplifying board design. The processor is well-suited for applications that are highly compute-intensive, I/O-intensive or both. This makes it ideal for applications such as enterprise and service provider routers, switches, media gateways, base station controllers, radio network controllers (RNCs), access gateways for Long Term Evolution (LTE) and general-purpose embedded computing systems in the networking, telecom, industrial, aerospace and defense markets.

Key Features

Freescale delivers a groundbreaking three-tiered cache hierarchy on the QorIQ P4 platform. Each core has an integrated Level 1 (L1) cache as well as a dedicated Level 2 (L2) backside cache that can significantly improve performance. Finally, a multi-megabyte Level 3 (L3) cache is also provided for those tasks for which a shared cache is desirable.

The CoreNet™ coherency fabric is a key design component of the QorIQ P4 platform. It manages full coherency of the caches and provides scalable on-chip, point-to-point connectivity supporting concurrent traffic to and from multiple resources connected to the fabric, eliminating single-point bottlenecks for non-competing resources. This eliminates bus contention and latency issues associated with scaling shared bus/shared memory architectures that are common in other multicore approaches.

QorIQ™ P4080 Block Diagram



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The QorIQ P4080 multicore processor is extremely flexible and can be configured to meet many system application needs. The processor's e500mc cores, leveraging advanced virtualization technology, can work as eight symmetric multiprocessing (SMP) cores, or eight completely asymmetric multiprocessing (AMP) cores, or they can be operated with varying degrees of independence with a combination of SMP and AMP groupings. Full processor independence, including the ability to independently boot and reset each e500mc core, is a defining characteristic of the device. The ability of the cores to run different operating systems (OSes), or run OS-less, provides the user with significant flexibility in partitioning between control, datapath and applications processing. It also simplifies consolidation of functions previously spread across multiple discrete processors onto a single device.

Advanced virtualization technology brings a new level of hardware partitioning through an embedded hypervisor that allows system developers to ensure software running on any CPU only accesses the resources (memory, peripherals, etc.) that it is explicitly authorized to access. The embedded hypervisor enables safe and autonomous operation of multiple individual operating systems, allowing them to share system resources, including processor cores, memory and other on-chip functions.

Ecosystem and Developer Environment

Developers creating solutions with Power Architecture technology have long benefited from a vibrant support ecosystem, including high-quality tools, OSes and network protocol stacks. Freescale has collaborated with our partners on the QorIQ P4080 processor to continue our strong ecosystem heritage. This helps to ensure that the best enablement tools are available to cost-effectively meet the unique development challenges of multicore architectures and speed your time to market.

To this end, Freescale has partnered with Virtutech to offer a robust, innovative hybrid simulation environment that provides a controlled, deterministic and fully reversible environment for the development, debugging and benchmarking of software for complex multicore-based architectures. The hybrid simulator combines Virtutech's fast, functional Simics™ model, with a detailed performance model of the platform. This combination enables fast hardware concept testing and evaluation, as well as performance verification and helps accelerate your development cycle, provide more flexible debug capability and improve the overall quality of your software.

Freescale has also engineered capabilities into the QorIQ P4080 to enable advanced debugging while working in tandem with its ecosystem partners to assure availability of tools that can take advantage of these features. These capabilities include integrated instruction trace, watchpoint triggers, cross-event triggers, performance monitoring and other debug features as defined by the Power® ISA. These features enable dynamic debug essential for providing visibility into complex interactions that may occur among tasks running on different cores.

QorIQ P4080 Technical Specifications

- Eight high-performance Power Architecture e500mc cores, each with a 32 KB instruction and data L1 cache and a private 128 KB L2 cache
  - Three levels of instruction: user, supervisor and hypervisor
  - Independent boot and reset
  - Secure boot capability
- 2 MB shared L3 CoreNet platform cache
- Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - 800 Gbps coherent read bandwidth
  - Queue manager fabric supporting packet-level queue management and quality of service scheduling
- Two 64-bit DDR2/DDR3 SDRAM memory controllers with ECC and interleaving support
- Datapath Acceleration Architecture incorporating acceleration for the following functions:
  - Packet parsing, classification and distribution
  - Queue management for scheduling, packet sequencing and congestion management
  - Hardware Buffer Management for buffer allocation and de-allocation
  - Cryptographic Security Acceleration (SEC 4.0)
  - RegEx Pattern Matching (PME 2.0)
- Ethernet interfaces
  - Two 10 Gbps Ethernet (XAUI) controllers
  - Eight 1 Gbps Ethernet (SGMII) controllers
- High-speed peripheral interfaces
  - Three PCI Express® V2.0 controllers/ports running at up to 5 GHz
  - Two Serial RapidIO® 1.2 controllers/ports running at up to 3.125 GHz
- Additional peripheral interfaces
  - Two USB controllers with ULPI interface to external PHY
  - SD/MMC
  - SPI controller
  - Four I^2C controllers
  - Two dual UARTs
  - Enhanced local bus controller (eLBC)
- Multicore programmable interrupt controller (PIC)
- Two 4-channel DMA engines

For more information about Virtutech Simics, please visit **www.virtutech.com**.

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com/multicore**.

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