74F656A

Octal buffer/driver with parity; non-inverting; 3-state Rev. 6 — 14 December 2011 Product

Product data sheet

1. **General description**

The 74F656A is an octal buffer and line driver with parity generation/checking. The 74F656A can be used as memory address driver, clock driver and bus-oriented transmitter/receiver. The inclusion of parity generation/checking improves PCB density.

Features and benefits 2.

- Combines 74F244 and 74F280A functions in one device
- High impedance NPN base inputs for reduced input current (40 μA in HIGH and LOW
- I_{IL} = 20 μA compared to 600 μA in FAST family specification
- For applications with high output drive and light bus loading
- Non-inverting
- 3-state output sink capability I_{OL} = 64 mA and source I_{OH} = 15 mA
- Inputs and outputs on separate sides simplifies board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (-40 °C to +85 °C)

Ordering information 3.

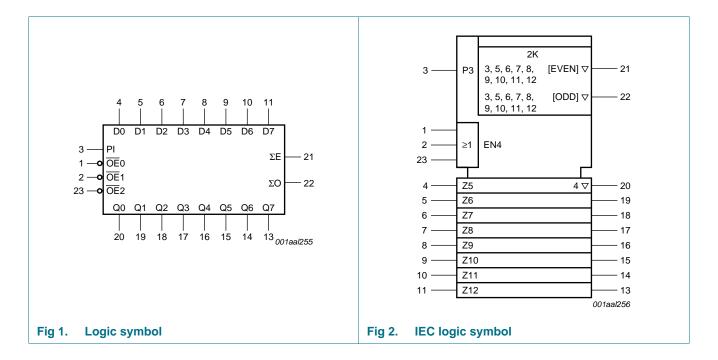
Table 1. **Ordering information**

Type number	Package	Package										
	Temperature range	Name	Description	Version								
N74F656AD	0 °C to 70 °C	SO24	plastic small outline package; 24 leads;	SOT137-1								
174F656AD	–40 °C to +85 °C		body width 7.5 mm									



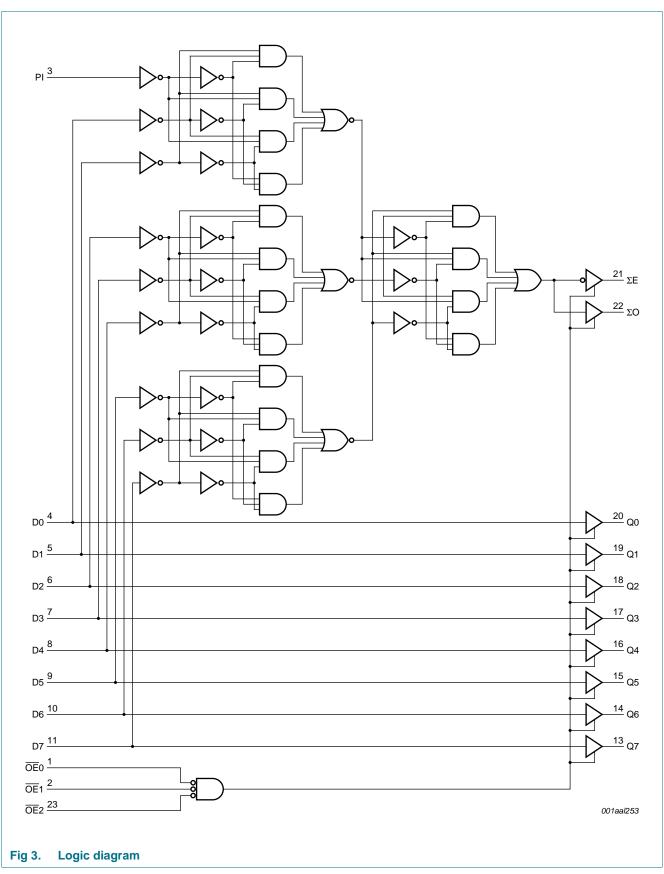
Octal buffer/driver with parity; non-inverting; 3-state

4. Functional diagram



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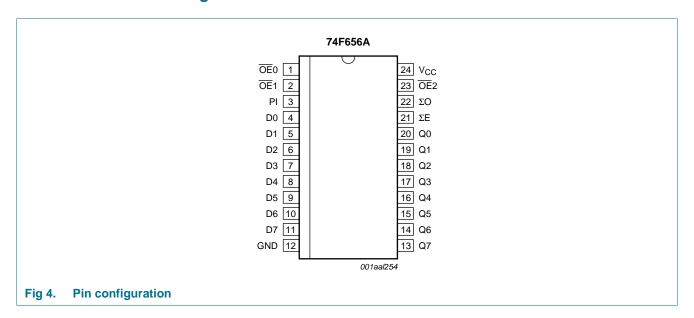
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Octal buffer/driver with parity; non-inverting; 3-state

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value ^[1] HIGH/LOW
OE0	1	output enable input (active LOW)	1.0/0.033	20 μΑ/20 μΑ
OE1	2	output enable input (active LOW)	1.0/0.033	20 μΑ/20 μΑ
PI	3	parity input	1.0/0.033	20 μΑ/20 μΑ
D0 to D7	4, 5, 6, 7, 8, 9, 10, 11	data input	2.0/0.066	40 μΑ/40 μΑ
GND	12	ground (0 V)		
Q0 to Q7	20, 19, 18, 17, 16, 15, 14, 13	data output	750/106.7	15 mA/64 mA
ΣΕ	21	even parity output	750/106.7	15 mA/64 mA
ΣΟ	22	odd parity output	750/106.7	15 mA/64 mA
OE2	23	output enable input (active LOW)	1.0/0.033	20 μΑ/20 μΑ
V_{CC}	24	supply voltage		

^[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

Octal buffer/driver with parity; non-inverting; 3-state

6. Functional description

6.1 Function table

Table 3. Function selection[1]

Input					Status
OE0	OE1	OE2	Dn	Qn	
L	L	L	L	L	transparent
L	L	L	Н	Н	
Н	Χ	Χ	X	Z	disabled
X	Н	X	X	Z	
Χ	Χ	Н	Х	Z	

^[1] H = HIGH voltage level;

Table 4. Function parity outputs[1]

Inputs	State	Parity output			
		ΣΕ	ΣΟ		
Even number of inputs (0, 2, 4, 6, 8)	Н	Н	L		
Odd number of inputs (1, 3, 5, 7, 9)	Н	L	Н		
Any OEn	Н	Z	Z		

^[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

Z = high-impedance OFF-state.

L = LOW voltage level;

Z = high-impedance OFF-state.

Octal buffer/driver with parity; non-inverting; 3-state

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		<u>[1]</u> –0.5	+7.0	V
Vo	output voltage	output in HIGH-state	<u>[1]</u> -0.5	V_{CC}	V
I _{IK}	input clamping current	$V_I < 0 V$	-30	+5	mA
Io	output current	output in LOW-state	-	128	mA
T _{amb}	ambient temperature	in free-air	<u>[2]</u>		
		commercial	0	70	°C
		industrial	-40	+85	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Cumbal	Parameter	Conditions	Min	Tun	Max	Unit
Symbol	Parameter	Conditions	IVIII	Тур	IVIAX	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
I _{IK}	input clamping current		-	-	-18	mA
I _{OH}	HIGH-level output current		–15	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA

9. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions		25 °C			+85 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-1.2	-0.73	-	-1.2	-	V
011	HIGH-level output	V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V						
	voltage	$I_{OH} = -3 \text{ mA}$						
		V _{CC} = ±10 %	-	-	-	2.4	-	V
		V _{CC} = ±5 %	-	3.3	-	2.7	-	V
		$I_{OH} = -15 \text{ mA}$						
		V _{CC} = ±10 %	-	-	-	2.0	-	V

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

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Table 7. Static characteristics ...continued

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		Unit
			Mir	ı Typ <mark>[1]</mark>	Max	Min	Max	
V_{OL}	LOW-level output	$V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$						
	voltage	I _{OL} = 64 mA						
		V _{CC} = ±10 %	-	-	-	-	0.55	V
		V _{CC} = ±5 %	-	0.42	-	-	0.55	V
I _I	input leakage current	$V_{CC} = 0 \text{ V}; V_I = 7.0 \text{ V}$	-	-	-	-	100	μΑ
I _{IH}	HIGH-level input current	V_{CC} = 5.5 V; V_I = 2.7 V; commercial						
		pin Dn	-	-	-	-	40	μΑ
		pin PI, OE n	-	-	-	-	20	μΑ
		$V_{CC} = 5.5 \text{ V}; V_I = 2.7 \text{ V}; industrial}$						
		pin Dn	-	-	-	-	80	μΑ
		pin PI, OE n	-	-	-	-	40	μΑ
I _{IL}	LOW-level input current	$V_{CC} = 5.5 \text{ V}; V_I = 0.5 \text{ V}$						
		pin Dn	-	-	-	-	-40	μΑ
		pin PI, OE n	-	-	-	-	-20	μΑ
l _{OZ}	OFF-state output current	V _{CC} = 5.5 V						
		$V_0 = 2.7 \text{ V}$	-	-	-	-	50	μΑ
		$V_{O} = 0.5 \text{ V}$	-	-	-	-	-50	μΑ
Io	output current	V _{CC} = 5.5 V	2] _	-	-	-100	-225	mΑ
I _{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	50	-	-	80	mΑ
		outputs LOW-state	-	78	-	-	110	mΑ
		outputs OFF-state	-	83	-	-	90	mΑ

^[1] All typical values are measured at $V_{CC} = 5 \text{ V}$.

10. Dynamic characteristics

Table 8. Dynamic characteristics GND = 0 V; for test circuit, see <u>Figure 7</u>.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V		0 °C to 70 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		-40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t _{PLH} LOW to HIGH propagation delay	Dn to Qn; see Figure 5	2.0	4.0	6.5	2.0	7.0	2.0	8.0	ns	
		Dn to ΣE , ΣO ; see Figure 5	5.5	10.0	13.0	5.5	14.0	4.5	16.5	ns
TILL	HIGH to LOW propagation delay	Dn to Qn; see <u>Figure 5</u>	2.5	5.5	7.0	2.5	7.5	2.5	9.0	ns
		Dn to ΣE , ΣO ; see Figure 5	5.5	11.0	14.5	5.5	16.5	5.5	18.0	ns
t _{PZH}	OFF-state to HIGH propagation delay	OEn to Qn; see Figure 6	3.5	7.0	10.5	3.5	11.5	3.0	13.0	ns

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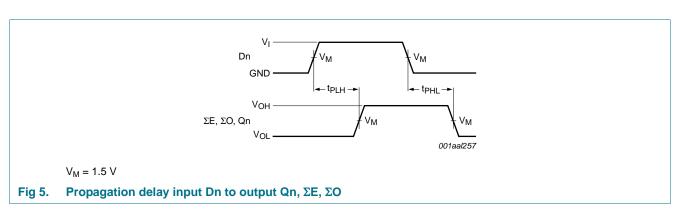
^[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

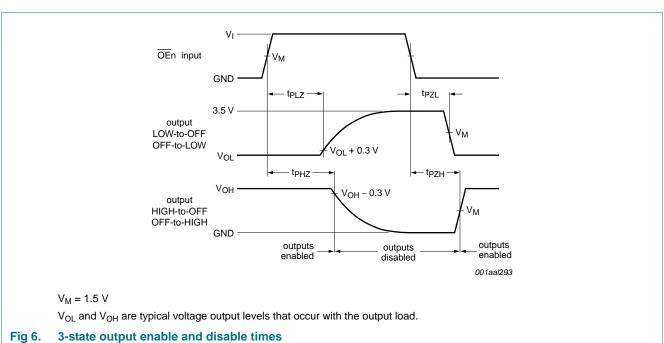
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Table 8. Dynamic characteristics ...continued GND = 0 V; for test circuit, see <u>Figure 7</u>.

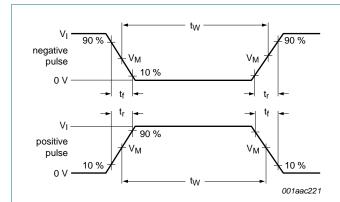
Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V		0 °C to 70 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		-40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	OEn to Qn; see Figure 6	4.0	8.0	11.0	4.5	12.0	4.0	13.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	OEn to Qn; see Figure 6	1.5	4.5	8.0	1.5	9.0	1.5	10.0	ns
t _{PLZ}	LOW to OFF-state propagation delay	OEn to Qn; see Figure 6	2.0	5.0	8.0	2.0	9.0	1.5	10.0	ns

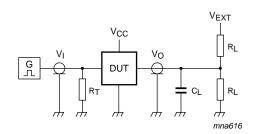
11. Waveforms





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a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in <u>Table 9</u>.

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 V_{EXT} = Test voltage for switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

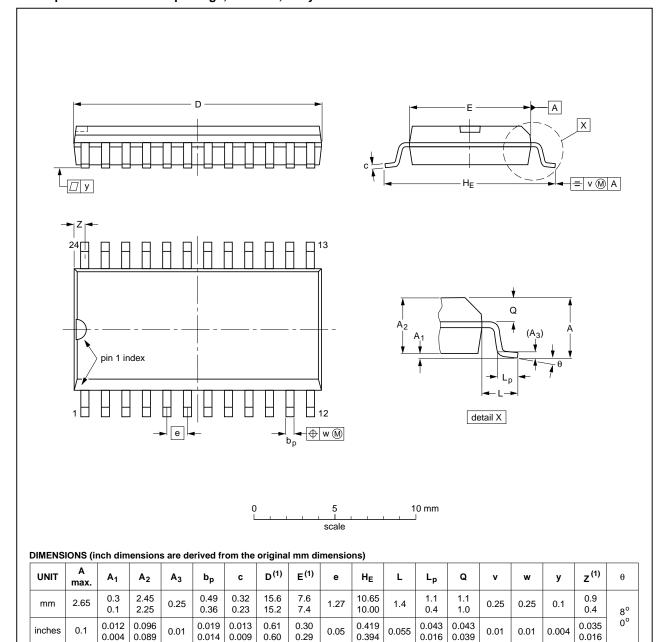
Input			Load		V _{EXT}			
VI	f _I	t _W	t _r , t _f	C _L	R_L	t_{PHL} , t_{PLH}	t_{PZH} , t_{PHZ}	t _{PZL} , t _{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500Ω	open	open	7.0 V

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12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE REFERENCES					EUROPEAN	ISSUE DATE
VERSION	N IEC JEDEC JEITA			PROJECTION	155UE DATE	
SOT137-1	075E05	MS-013				99-12-27 03-02-19

Fig 8. Package outline SOT137-1 (SO24)

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Octal buffer/driver with parity; non-inverting; 3-state

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
PCB	Printed-Circuit Board

14. Revision history

Table 11. Revision history

	-			
Document ID	Release date	Data sheet status	Change notice	Supersedes
74F656A v.6	20111214	Product data sheet	-	74F656A v.5
Modifications:	 Legal pages 	s updated.		
74F656A v.5	20100325	Product data sheet	-	74F656A v.4
74F656A v.4	20100205	Product data sheet	-	74F656A v.3
74F656A v.3	20000630	Product specification	-	74F656A v.2
74F656A v.2	19910717	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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