74F827

10-bit buffer/line driver; non-inverting; 3-state

Rev. 04 — 29 January 2010 Product data sheet

1. General description

The 74F827 10-bit buffer, provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The device has NOR output enables ($\overline{OE}0$, $\overline{OE}1$) for maximum control flexibility.

2. Features

- High impedance NPN base inputs for reduced loading (20 μA input current in HIGH and LOW states)
- I_{IL} = 20 μA compared to 600 μA in FAST family specification
- Ideal for high speed, light bus loading with increased fan-in
- Controlled rise and fall times to minimize ground bounce
- Glitch-free power-up in 3-state
- Flow-through pinout architecture for microprocessor oriented applications
- Output sink capability, I_{OL} = 64 mA

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F827D	0 °C to 70 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F827DB	0 °C to 70 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

founded by Philips

4. Functional diagram

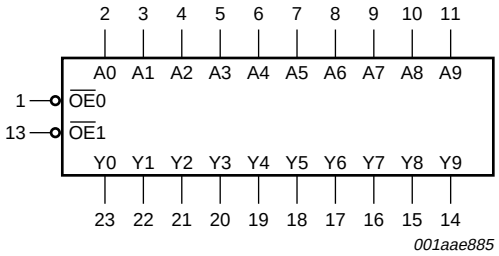

Fig 1. Logic symbol

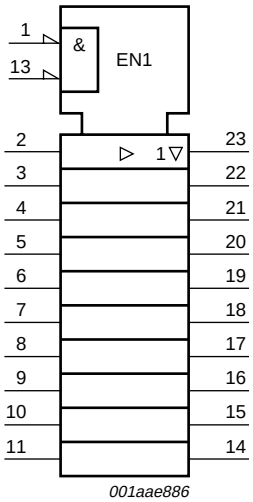

Fig 2. IEC logic symbol

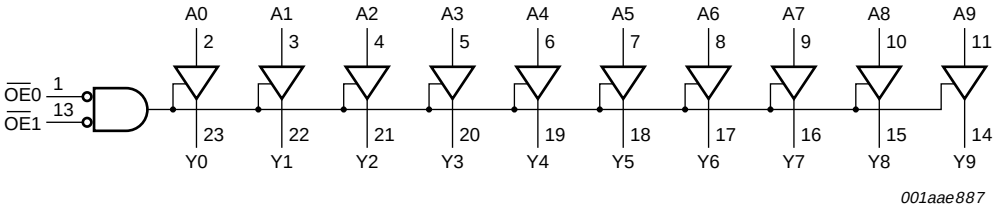

Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

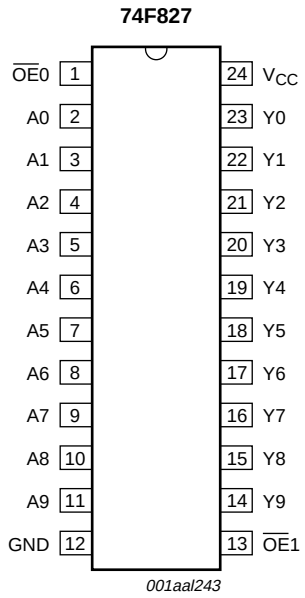

Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value[1] HIGH/LOW
$\overline{OE}$0	1	output enable input (active LOW)	1.0/0.033	20 μA/20 μA
A0 to A9	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input	1.0/0.033	20 μA/20 μA
GND	12	ground (0 V)	-	-
$\overline{OE}$1	13	output enable input (active LOW)	1.0/0.033	20 μA/20 μA
Y0 to Y9	23, 22, 21, 20, 19, 18, 17, 16, 15, 14	data output	1200/106.7	24 mA/64 mA
V_{CC}	24	supply voltage	-	-

[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

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6. Functional description

6.1 Function table

Table 3. Function selection[1]

Input		Output	Status
$\overline{OE}$n	An	Yn	
L	L	L	transparent
L	H	H	
H	X	Z	disabled

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in HIGH-state	[1]	–0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V		–30	+5	mA
I_O	output current	output in LOW-state		-	128	mA
T_{amb}	ambient temperature	in free-air	[2]	0	70	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{IK}	input clamping current		–18	-	-	mA
I_{OH}	HIGH-level output current		–24	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			0 °C to 70 °C		Unit
				Min	Typ[1]	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–1.2	–0.73	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V							
		I_{OH} = –15 mA							
		V_{CC} = ±10 %		-	-	-	2.4	-	V
		V_{CC} = ±5 %		-	3.3	-	2.4	-	V
		I_{OH} = –24 mA							
		V_{CC} = ±10 %		-	-	-	2.0	-	V
		V_{CC} = ±5 %		-	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V							
		I_{OL} = 64 mA							
		V_{CC} = ±10 %		-	-	-	-	0.55	V
		V_{CC} = ±5 %		-	0.42	-	-	0.55	V
I_I	input leakage current	V_{CC} = 0 V; V_I = 7.0 V		-	-	-	-	100	µA
I_{IH}	HIGH-level input current	V_{CC} = 5.5 V; V_I = 2.7 V		-	-	-	-	20	µA
I_{IL}	LOW-level input current	V_{CC} = 5.5 V; V_I = 0.5 V		-	-	-	-	–20	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V							
		V_O = 2.7 V		-	-	-	-	50	µA
		V_O = 0.5 V		-	-	-	-	–50	µA
I_O	output current	V_{CC} = 5.5 V	[2]	-	-	-	–100	–225	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	50	-	-	70	mA
		outputs LOW-state		-	70	-	-	100	mA
		outputs OFF-state		-	60	-	-	90	mA

[1] All typical values are measured at V_{CC} = 5 V.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			0 °C to 70 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Yn; see Figure 5						
		C_L = 50 pF	2.0	5.5	8.5	2.0	9.0	ns
		C_L = 300 pF, 1 output switching	-	9.5	13.0	-	14.0	ns
		C_L = 300 pF, 10 outputs switching	-	12.0	16.0	-	17.0	ns

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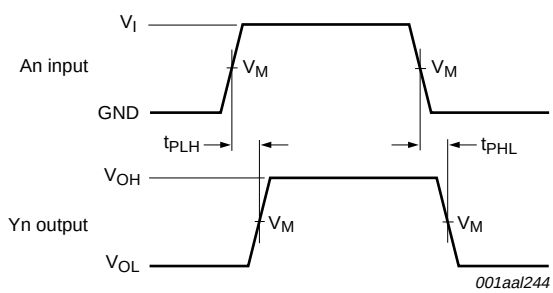
Table 7. Dynamic characteristics *...continued*

GND = 0 V; for test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			0 °C to 70 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	An to Yn; see Figure 5						
		C_L = 50 pF	2.0	4.5	8.5	2.0	9.0	ns
		C_L = 300 pF, 1 output switching	-	7.5	10.0	-	11.0	ns
		C_L = 300 pF, 10 outputs switching	-	14.0	17.0	-	18.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$n to Yn; see Figure 6						
		C_L = 50 pF	5.0	8.0	12.0	4.5	14.0	ns
		C_L = 300 pF, 1 output switching	-	15.0	20.0	-	21.0	ns
		C_L = 300 pF, 10 outputs switching	-	15.0	20.0	-	21.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$n to Yn; see Figure 6						
		C_L = 50 pF	4.0	6.0	10.5	4.0	11.5	ns
		C_L = 300 pF, 1 output switching	-	9.5	13.0	-	14.0	ns
		C_L = 300 pF, 10 outputs switching	-	17.0	21.0	-	21.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$n to Yn; see Figure 6						
		C_L = 50 pF	2.5	5.0	8.0	2.0	8.5	ns
		C_L = 300 pF, 1 output switching	-	15.0	19.0	-	20.0	ns
		C_L = 300 pF, 10 outputs switching	-	15.0	19.0	-	20.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$n to Yn; see Figure 6						
		C_L = 50 pF	2.5	5.0	8.0	2.0	8.5	ns
		C_L = 300 pF, 1 output switching	-	9.5	13.5	-	14.0	ns
		C_L = 300 pF, 10 outputs switching	-	12.5	15.5	-	16.0	ns

11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (An) to output (Yn)

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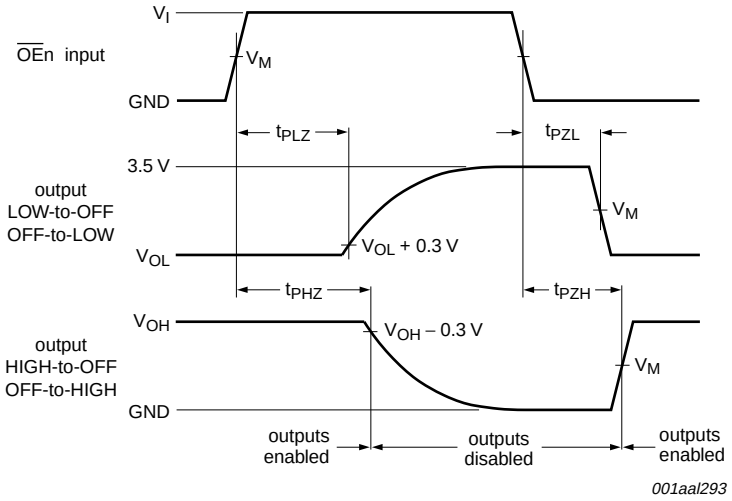

V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay 3-state output enable time to LOW-level and output disable time from LOW-level

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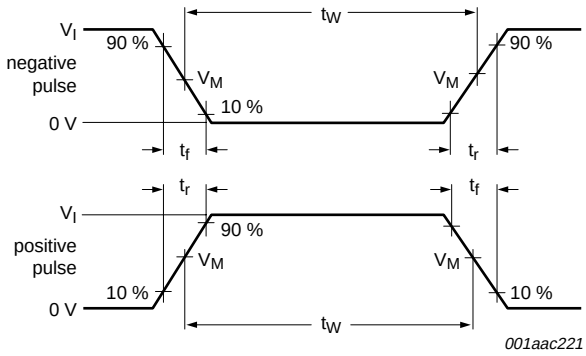
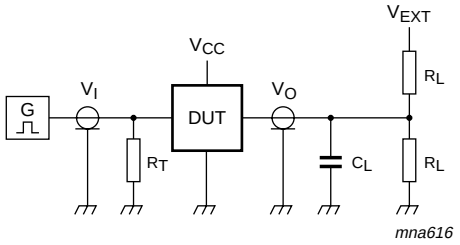


a. Input pulse definition



b. Test circuit

Test data and V_{EXT} levels are given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

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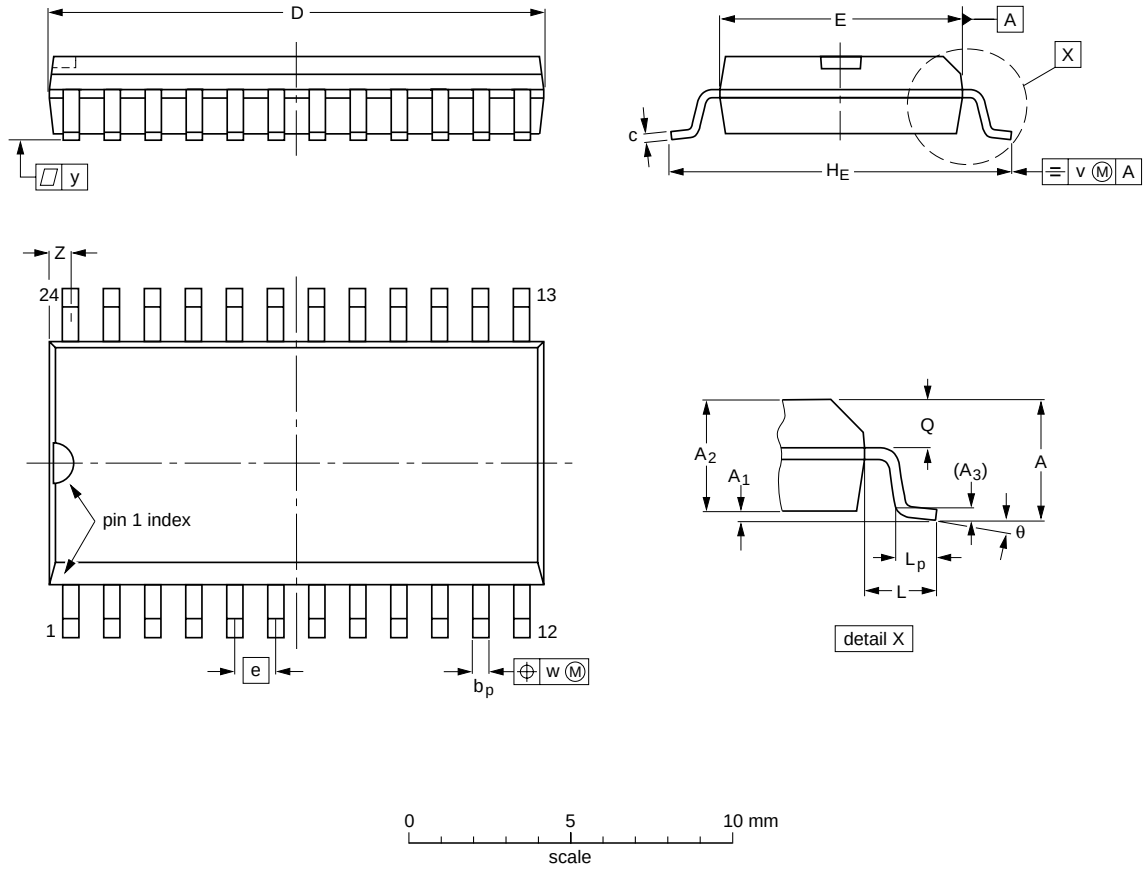
12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT137-1 (SO24)

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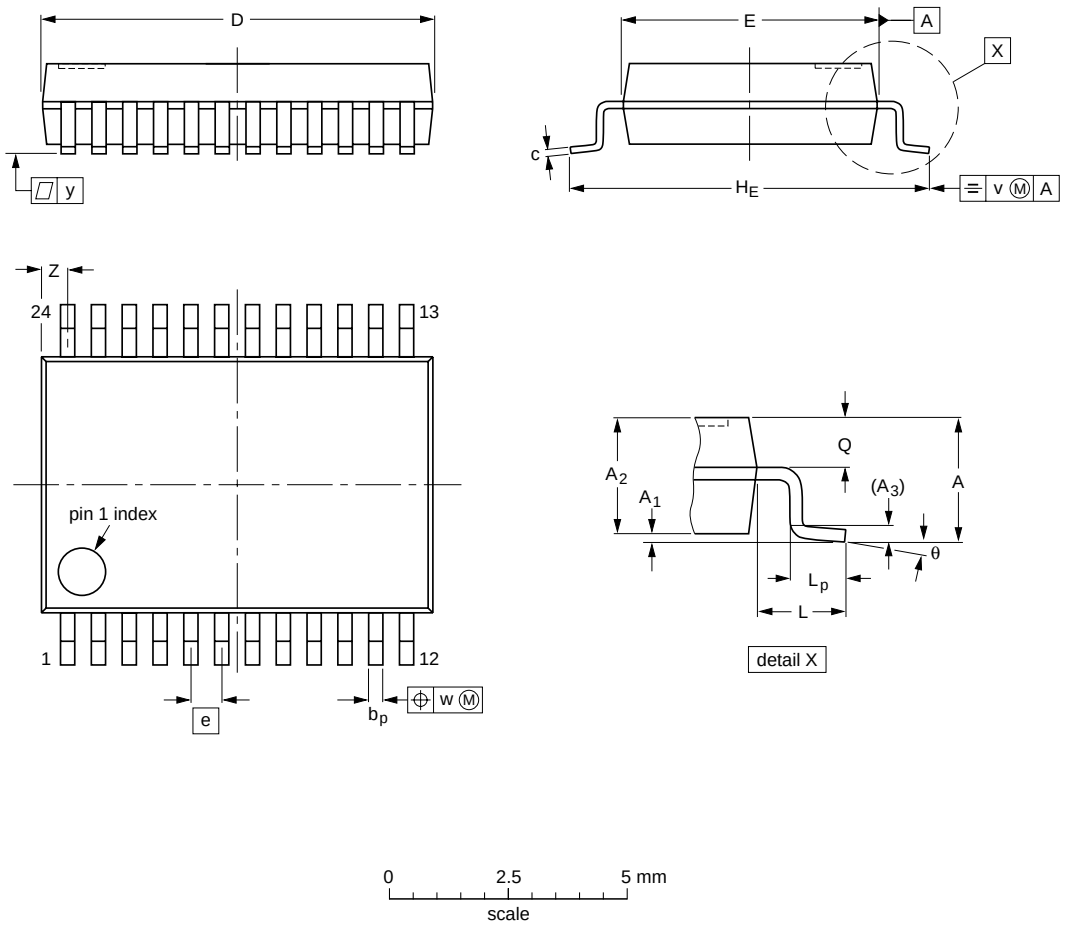
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT340-1 (SSOP24)

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13. Abbreviations

Table 9. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F827_4	20100129	Product data sheet	-	74F827_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”			
74F827_3	20040121	Product specification	-	74F827_74F828_2
74F827_74F828_2	19941205	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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