74HCT534

5 V octal D-type flip-flop; positive-edge trigger; inverting; 3-state

Rev. 03 — 18 October 2004 Product data sheet

1. General description

The 74HCT534 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HCT534 is specified in compliance with JEDEC standard no. 7A.

The 74HCT534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74HCT534 is functionally identical to the 74HCT374, but has inverted outputs.

2. Features

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input.

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	C_L = 15 pF; V_{CC} = 5 V		-	13	-	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V		-	40	-	MHz
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per flip-flop	C_L = 50 pF; V_{CC} = 4.5 V	[1] [2]	-	19	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;

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V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC} – 1.5 V.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT534N	–40 °C t0 +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT534D	–40 °C t0 +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

5. Functional diagram

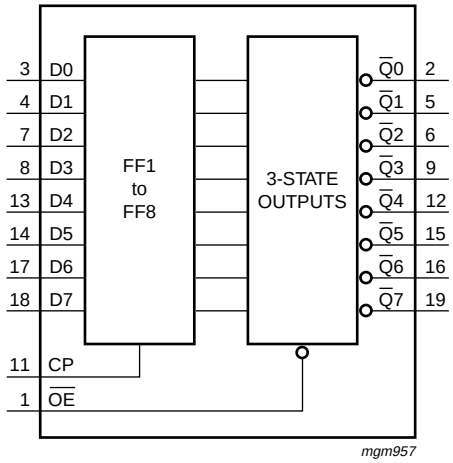

Fig 1. Functional diagram.

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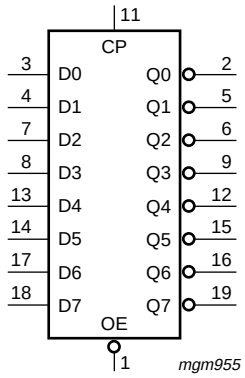

Fig 2. Logic symbol.

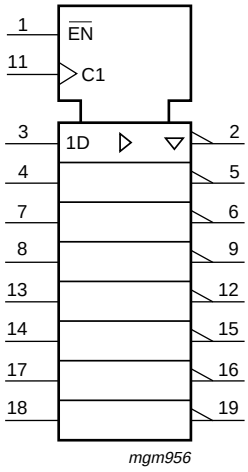

Fig 3. IEC logic symbol.

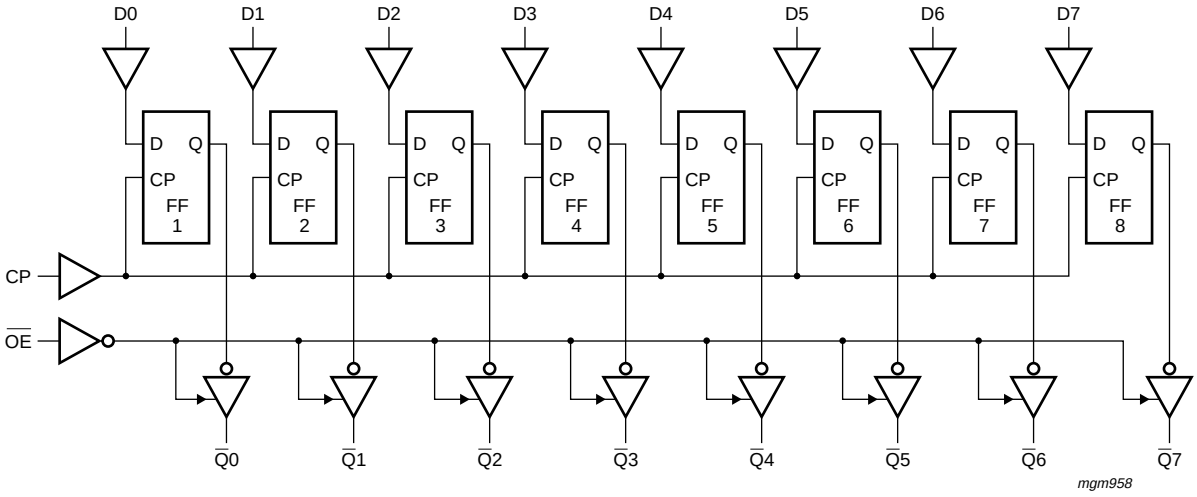

Fig 4. Logic diagram.

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6. Pinning information

6.1 Pinning

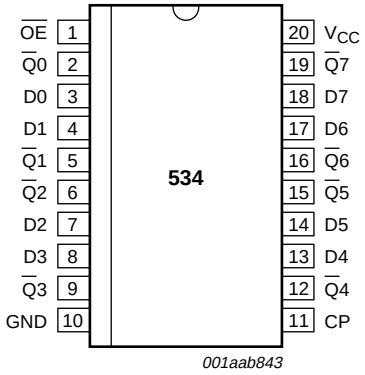

Fig 5. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
$\overline{Q}0$	2	3-state output
D0	3	data input
D1	4	data input
$\overline{Q}1$	5	3-state output
$\overline{Q}2$	6	3-state output
D2	7	data input
D3	8	data input
$\overline{Q}3$	9	3-state output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
$\overline{Q}4$	12	3-state output
D4	13	data input
D5	14	data input
$\overline{Q}5$	15	3-state output
$\overline{Q}6$	16	3-state output
D6	17	data input
D7	18	data input
$\overline{Q}7$	19	3-state output
V_{CC}	20	supply voltage

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7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Internal flip-flops	Output $\overline{Q}$n
	$\overline{OE}$	CP	Dn		
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V		-	±20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V		-	±20	mA
I_O	output source or sink current	V_O = –0.5 V to V_{CC} + 0.5 V		-	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±70	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP20 package		[1]	-	750	mW
	SO20 package		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V

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Table 6: Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	V_{CC} = 4.5 V	-	6.0	500	ns
T_{amb}	ambient temperature	see Section 10 and 11	–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 μA	4.4	4.5	-	V
		I_O = –6 mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	0	0.1	V
		I_O = 6.0 mA	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	μA
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL}; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; I_O = 0 A	-	-	±0.5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V; other inputs $V_I = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
		pin $\overline{OE}$	-	125	450	μA
		pin CP	-	90	325	μA
		pins Dn	-	35	125	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 μA	4.4	-	-	V
		I_O = –6 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	μA

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Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL}; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	±5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pin $\overline{OE}$	-	-	560	μA
		pin CP	-	-	405	μA
		pins Dn	-	-	155	μA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ μA	4.4	-	-	V
		$I_O = -6$ mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ μA	-	-	0.1	V
		$I_O = 6.0$ mA	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±1.0	μA
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL}; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pin $\overline{OE}$	-	-	610	μA
		pin CP	-	-	440	μA
		pins Dn	-	-	170	μA

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $V_{CC} = 4.5$ V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see Figure 9

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	see Figure 6				
		$C_L = 50$ pF; $V_{CC} = 4.5$ V	-	16	30	ns
		$C_L = 15$ pF; $V_{CC} = 5$ V	-	13	-	
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7	-	16	30	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; V_{CC} = 4.5 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7		-	18	30	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6		-	5	12	ns
t_W	clock pulse width HIGH or LOW	see Figure 6		23	14	-	ns
t_{su}	set-up time Dn to CP	see Figure 8		12	4	-	ns
t_h	hold time Dn to CP	see Figure 8		5	–1	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6					
		C_L = 50 pF; V_{CC} = 4.5 V		22	36	-	MHz
		C_L = 15 pF; V_{CC} = 5 V		-	40	-	MHz
C_{PD}	power dissipation capacitance per flip-flop		[1] [2]	-	19	-	pF
T_{amb} = –40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	see Figure 6		-	-	38	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7		-	-	38	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7		-	-	38	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6		-	-	15	ns
t_W	clock pulse width HIGH or LOW	see Figure 6		29	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8		15	-	-	ns
t_h	hold time Dn to CP	see Figure 8		5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6		18	-	-	MHz
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	see Figure 6		-	-	45	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7		-	-	45	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7		-	-	45	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6		-	-	18	ns
t_W	clock pulse width HIGH or LOW	see Figure 6		35	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8		18	-	-	ns
t_h	hold time Dn to CP	see Figure 8		5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6		15	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC} – 1.5 V.

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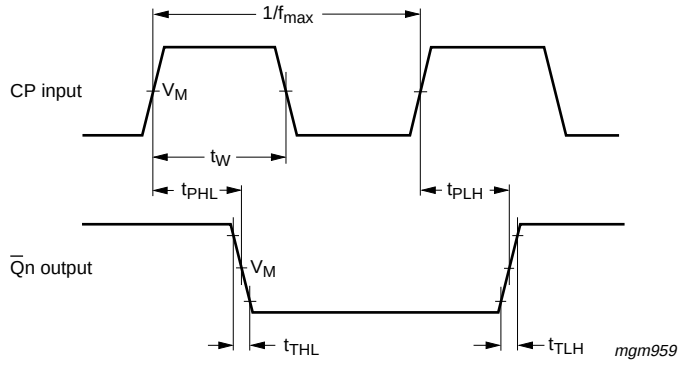
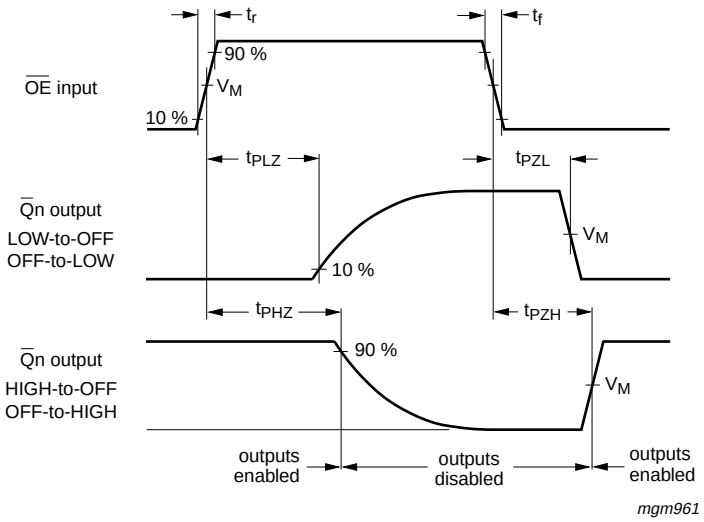
12. Waveforms



V_M = 1.3 V; V_I = GND to 3 V.

Fig 6. Waveforms showing the clock (CP) to output ($\overline{Q}$n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



V_M = 1.3 V; V_I = GND to 3 V.

Fig 7. Waveforms showing the 3-state enable and disable times.

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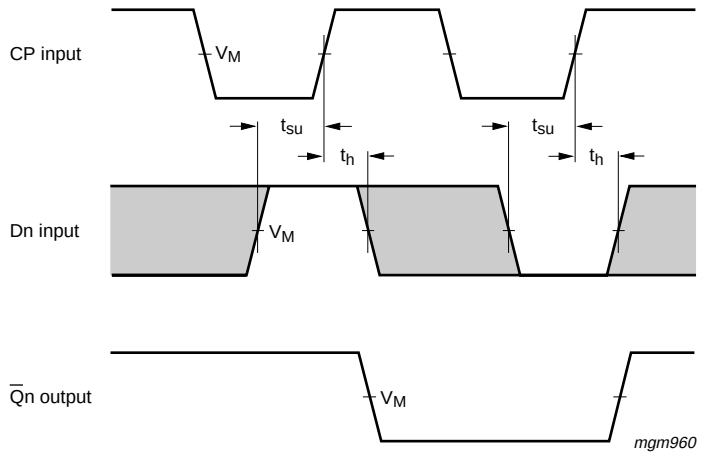
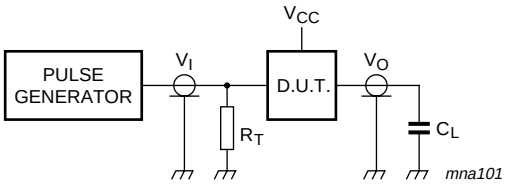


V_M = 1.3 V; V_I = GND to 3 V.

Fig 8. Waveforms showing the data set-up and hold times for Dn input.



Definitions test circuits:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance (See Section 11 for the value).

Fig 9. Load circuitry for switching times.

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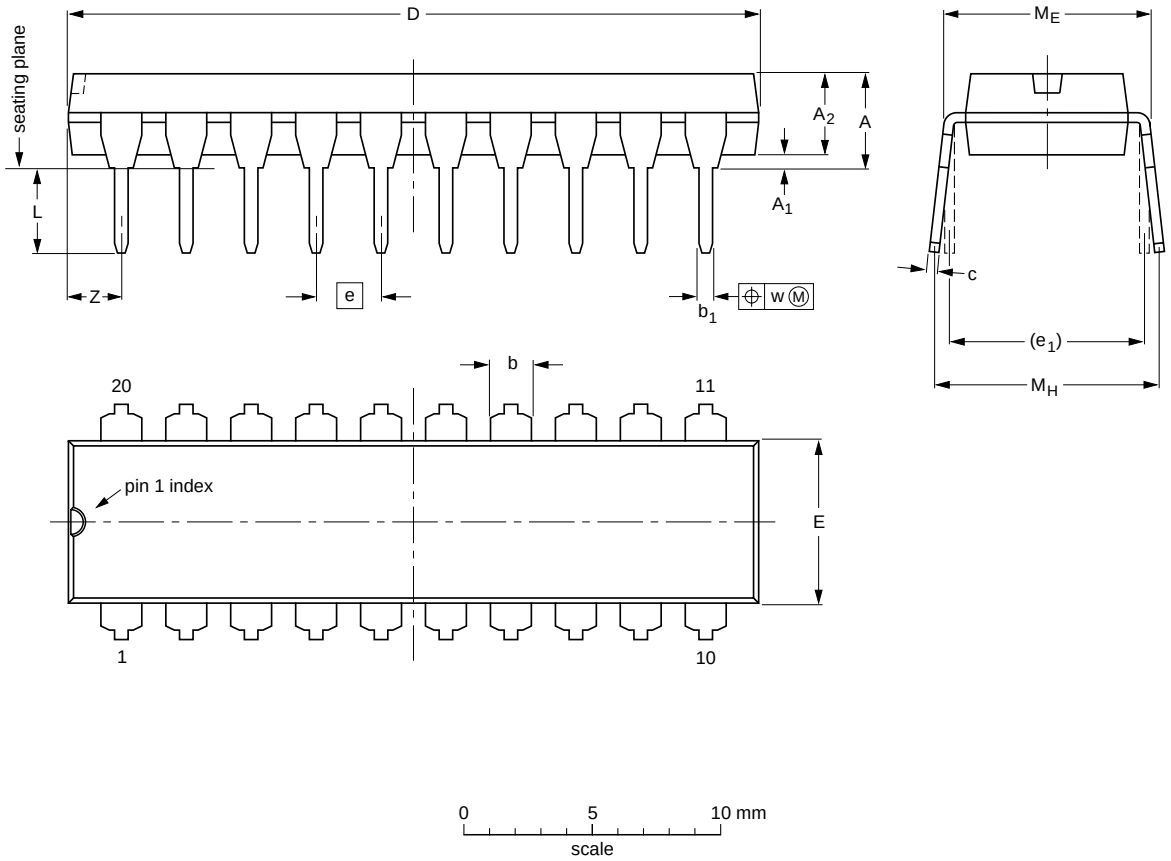
13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT146 (DIP20).

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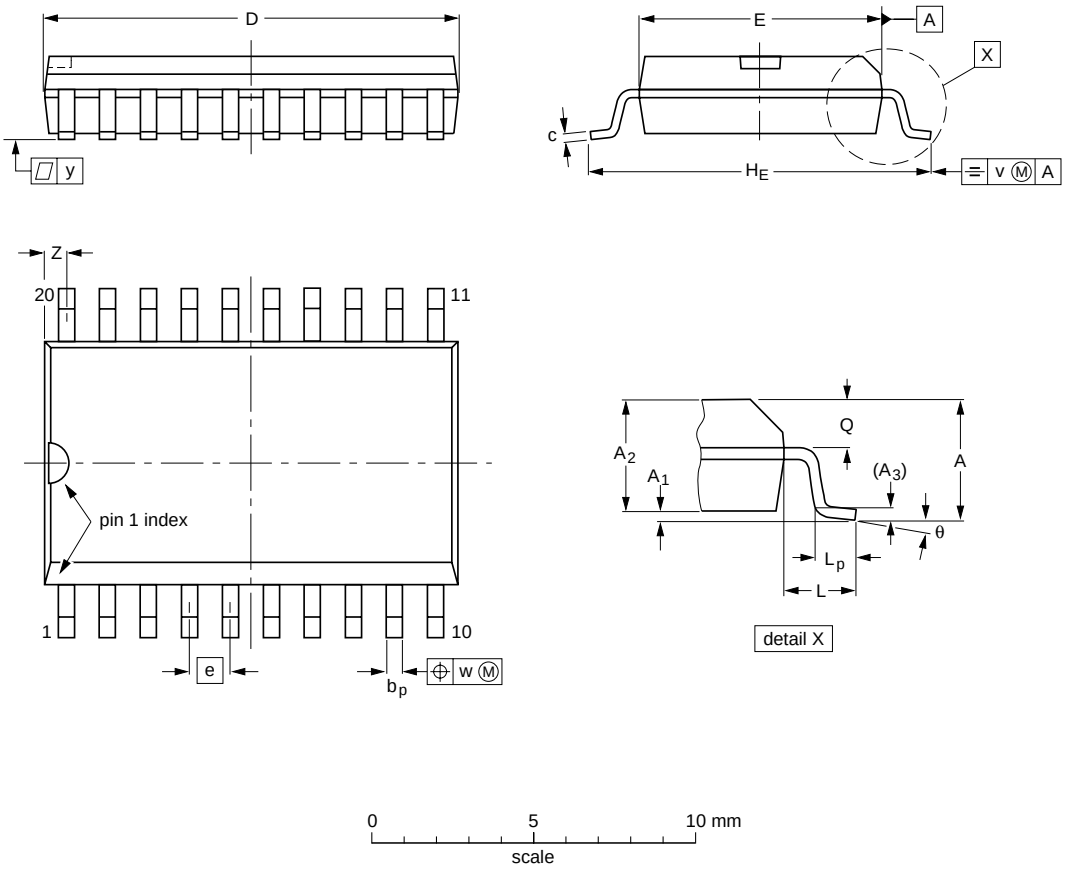
SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163 (SO20).

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14. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HCT534_3	20041018	Product data sheet	-	9397 750 13817	74HC_HCT534_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Information related to 74HC534 type is deleted • Reference to family specifications is replaced by the actual information.				
74HC_HCT534_CNV_2	19980410	Product specification	-	-	74HC_HCT534_1

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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16. Definitions

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