74LV165A

8-bit parallel-in/serial-out shift register

Rev. 2 — 4 September 2013 Product data sheet

1. General description

The 74LV165A is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and $\overline{Q7}$) available from the last stage. When the parallel-load input ($\overline{PL}$) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input $\overline{PL}$ is HIGH, data enters the register serially at the input DS. It shifts one place to the right (Q0 → Q1 → Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output Q7 to the input DS of the succeeding stage.

The clock input is a gate-OR structure which allows one input to be used as an active LOW clock enable input ($\overline{CE}$) input. The pin assignment for the inputs CP and $\overline{CE}$ is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input $\overline{CE}$ should only take place while CP HIGH for predictable operation.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times. It is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging current backflow through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- CMOS LOW power consumption
- 5.5 V tolerant inputs/outputs
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
  - JESD8-1A (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114-A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV165AD	–40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV165APW	–40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

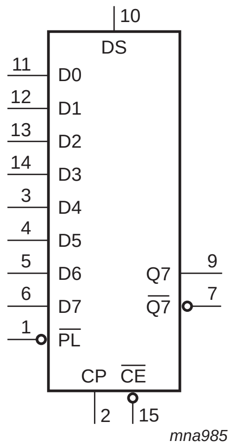


Fig 1. Logic symbol

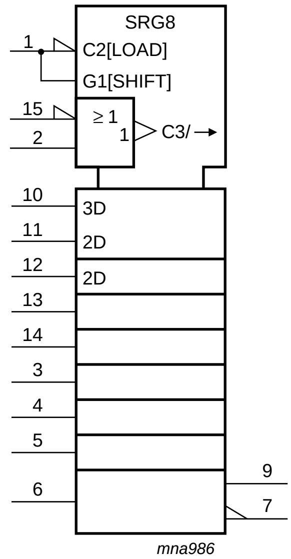


Fig 2. IEC logic symbol

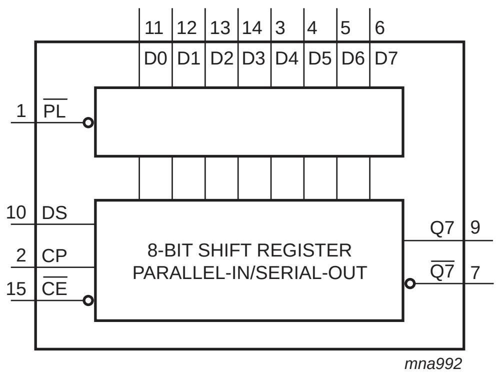


Fig 3. Functional diagram

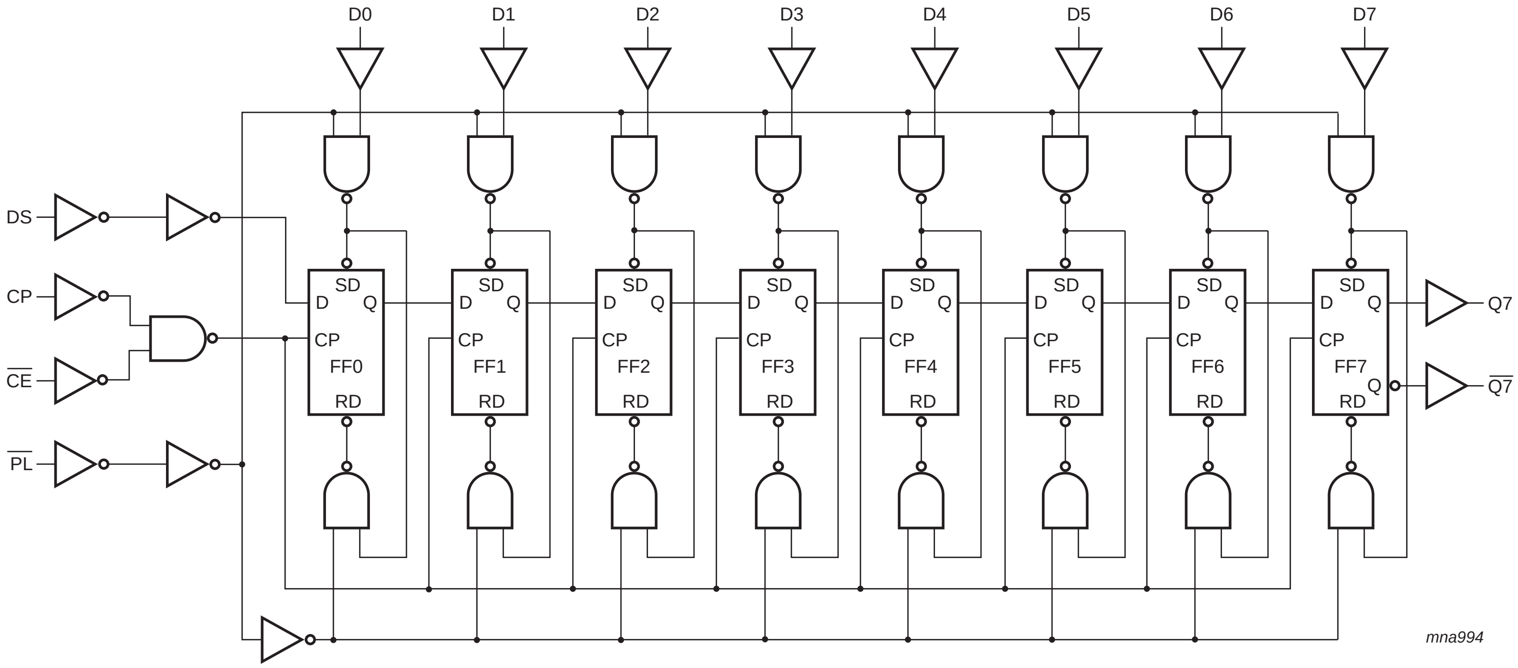


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

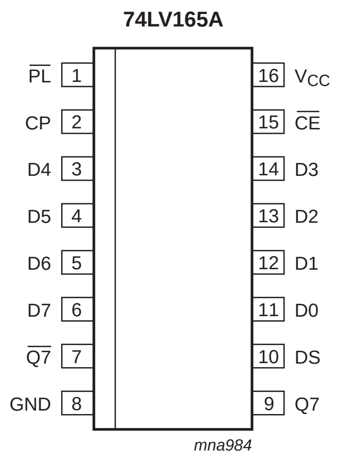


Fig 5. Pin configuration (SO16 and TSSOP16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{PL}$	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	serial output from the last stage
GND	8	ground (0 V)
Q7	9	asynchronous master reset (active LOW)
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
$\overline{CE}$	15	clock enable input (active LOW)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table[1]

Operating modes	Inputs					Qn registers		Output	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

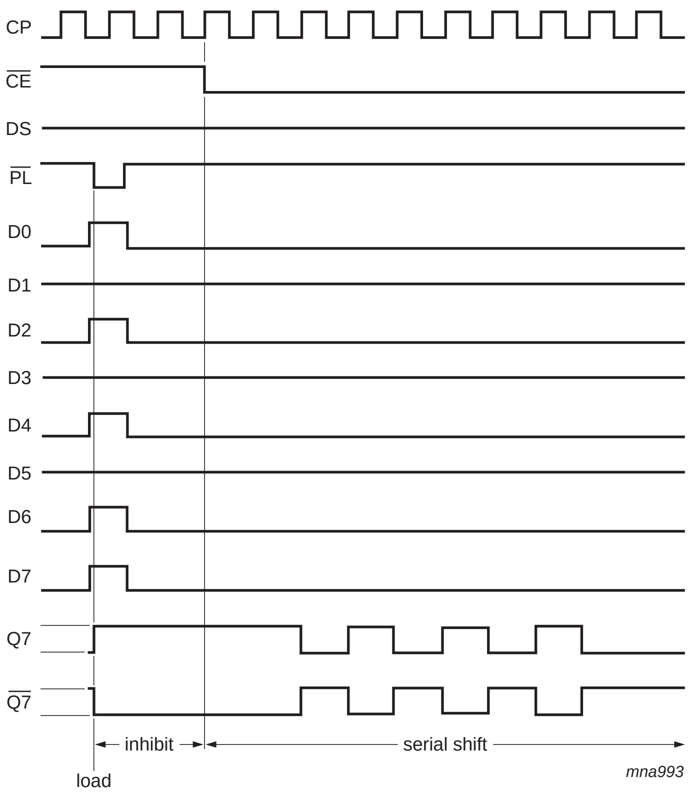


Fig 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–20	mA
V_I	input voltage			–0.5	+7	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$		-	±50	mA
V_O	output voltage			–0.5	V_{CC} + 0.5	V
		power-down mode		–0.5	+7	V
I_O	output current	0 V < V_O < V_{CC}		-	±25	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C				
		SO16 package	[2]	-	500	mW
		TSSOP16 package	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V	0	-	200	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 2.3 V to 2.7 V	$0.7V_{CC}$	-	-	V
		V_{CC} = 3.0 V to 3.6 V	$0.7V_{CC}$	-	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 2.3 V to 2.7 V	-	-	$0.3V_{CC}$	V
		V_{CC} = 3.0 V to 3.6 V	-	-	$0.3V_{CC}$	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −50 μA; V_{CC} = 2.0 V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		I_O = −2.0 mA; V_{CC} = 2.3 V	2.0	-	-	V
		I_O = −6.0 mA; V_{CC} = 3.0 V	2.48	-	-	V
		I_O = −12 mA; V_{CC} = 4.5 V	3.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 μA; V_{CC} = 2.0 V to 5.5 V	-	-	0.10	V
		I_O = 2.0 mA; V_{CC} = 2.3 V	-	-	0.40	V
		I_O = 6.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	±0.01	±1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0.0 V	-	±0.05	±5	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.2	20	μA
C_I	input capacitance		-	3.0	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Figure 12

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
t_{pd}	propagation delay	$\overline{CE}$, CP to Q7, $\overline{Q7}$; C_L = 15 pF; see Figure 7 and Figure 8	[2]				
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	11.0	22.0	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	7.5	18.0	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	5.5	11.5	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; C_L = 15 pF; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	11.5	23.5	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	8.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	5.5	11.5	ns
		D7 to Q7, $\overline{Q7}$; C_L = 15 pF; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	12.0	24.0	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	8.5	16.5	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	6.0	10.5	ns
		$\overline{CE}$, CP to Q7, $\overline{Q7}$; see Figure 7 and Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	13.0	26.0	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	9.0	21.5	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	6.1	13.5	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	14.0	28.0	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	10.0	22.0	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	6.5	13.5	ns
		D7 to Q7, $\overline{Q7}$; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[3]	1.0	14.0	28.0	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	1.0	10.0	20	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	6.5	12.5	ns
t_W	pulse width	CP input HIGH to LOW; see Figure 7					
		V_{CC} = 2.3 V to 2.7 V	[3]	9.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	4.0	-	-	ns
		$\overline{PL}$ input LOW; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[3]	13.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	9.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	6.0	-	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[3]	8.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	4.0	-	-	ns

Table 7. Dynamic characteristics *...continued*
GND (ground = 0 V); for test circuit, see Figure 12

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
t_{su}	set-up time	DS to CP, $\overline{CE}$; see Figure 10					
		V_{CC} = 2.3 V to 2.7 V	[3]	6.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	4.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	7.0	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; see Figure 10					
		V_{CC} = 2.3 V to 2.7 V	[3]	7.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	3.5	-	-	ns
		D7 to $\overline{PL}$; see Figure 11					
		V_{CC} = 2.3 V to 2.7 V	[3]	12	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	8.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	5.0	-	-	ns
t_h	hold time	DS to CP, $\overline{CE}$; $\overline{PL}$ to CP, $\overline{CE}$; see Figure 10					
		V_{CC} = 2.3 V to 2.7 V	[3]	0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	0.5	-	-	ns
		Dn to $\overline{PL}$; see Figure 11					
		V_{CC} = 2.3 V to 2.7 V	[3]	0.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[4]	0.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[5]	1.0	-	-	ns
f_{max}	maximum frequency	CP input; C_L = 15 pF; see Figure 7					
		V_{CC} = 2.3 V to 2.7 V	[3]	45	80	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[4]	50	115	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[5]	90	165	-	MHz
		CP input; see Figure 7					
		V_{CC} = 2.3 V to 2.7 V	[3]	35	65	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[4]	50	90	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[5]	85	125	-	MHz

Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); for test circuit, see Figure 12

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V	[6]	-	24	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] Typical values are measured at V_{CC} = 2.5 V.

[4] Typical values are measured at V_{CC} = 3.3 V.

[5] Typical values are measured at V_{CC} = 5.0 V.

[6] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ (P_D in μW), where:

f_i = input frequency in MHz;

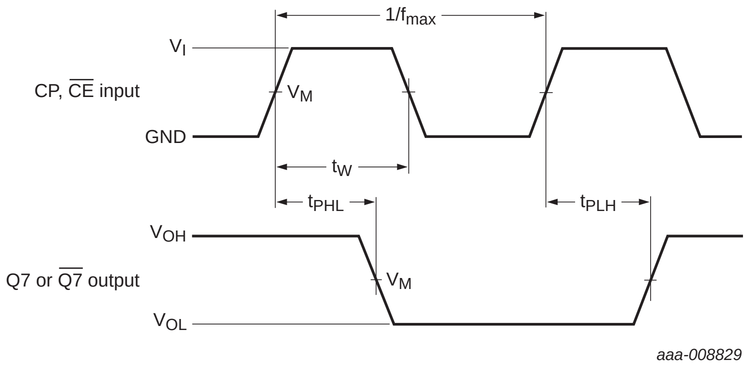
f_o = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

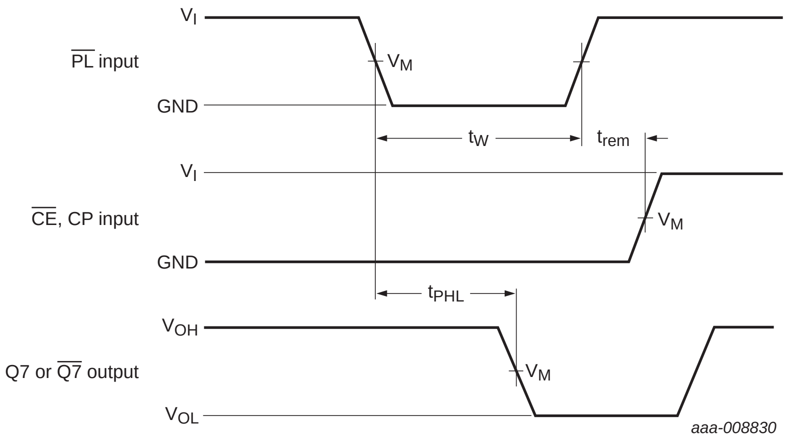
11. Waveforms



Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

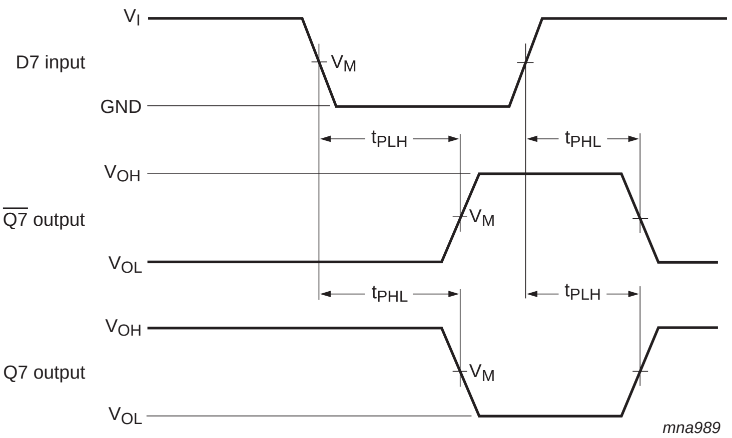
Fig 7. Clock pulse (CP) and clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, clock pulse width and maximum clock frequency



Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

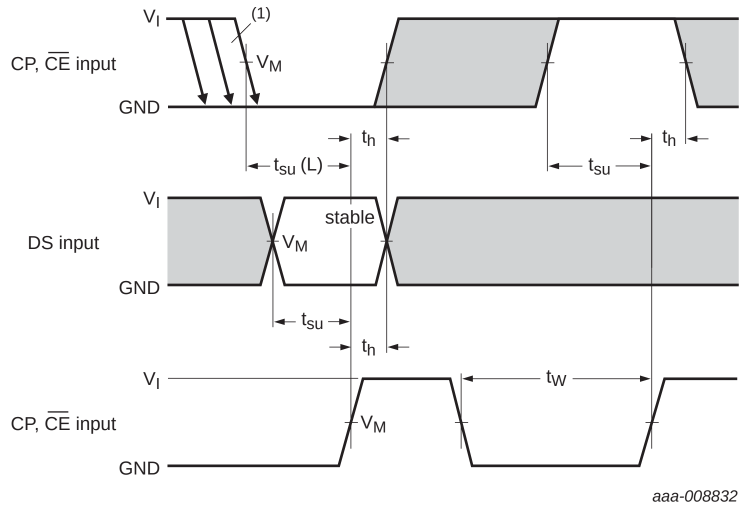
Fig 8. Parallel load (PL) pulse width, parallel load to output (Q7 or Q7) propagation delays, parallel load to clock (CP) and clock enable (CE) recovery time



Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

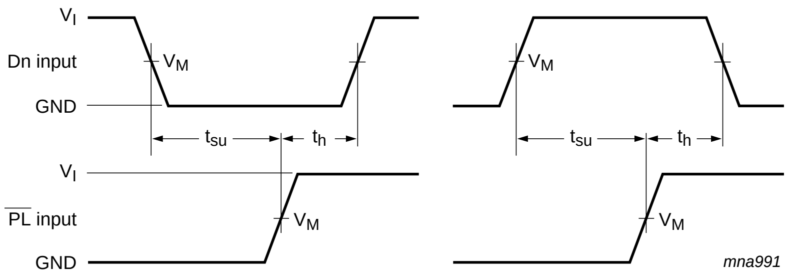
Fig 9. Data input (D7) to output (Q7 or Q7) propagation delays when PL is LOW



Measurement points are given in Table 8.

(1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 10. Set-up and hold times

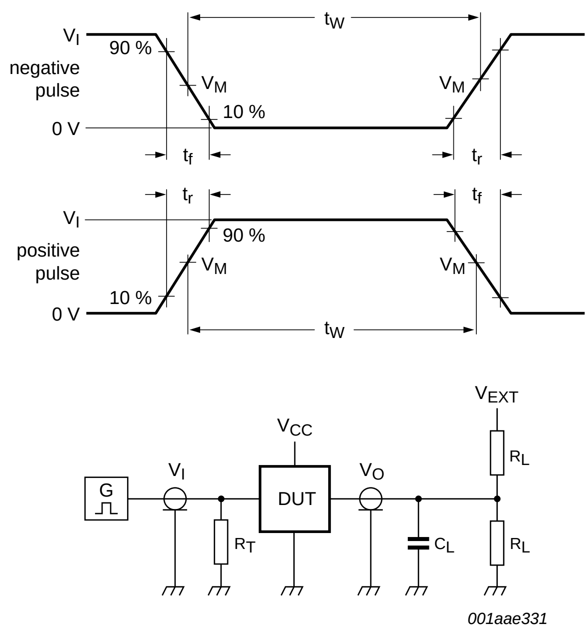


Measurement points are given in Table 8.

Fig 11. Set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
2.0 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

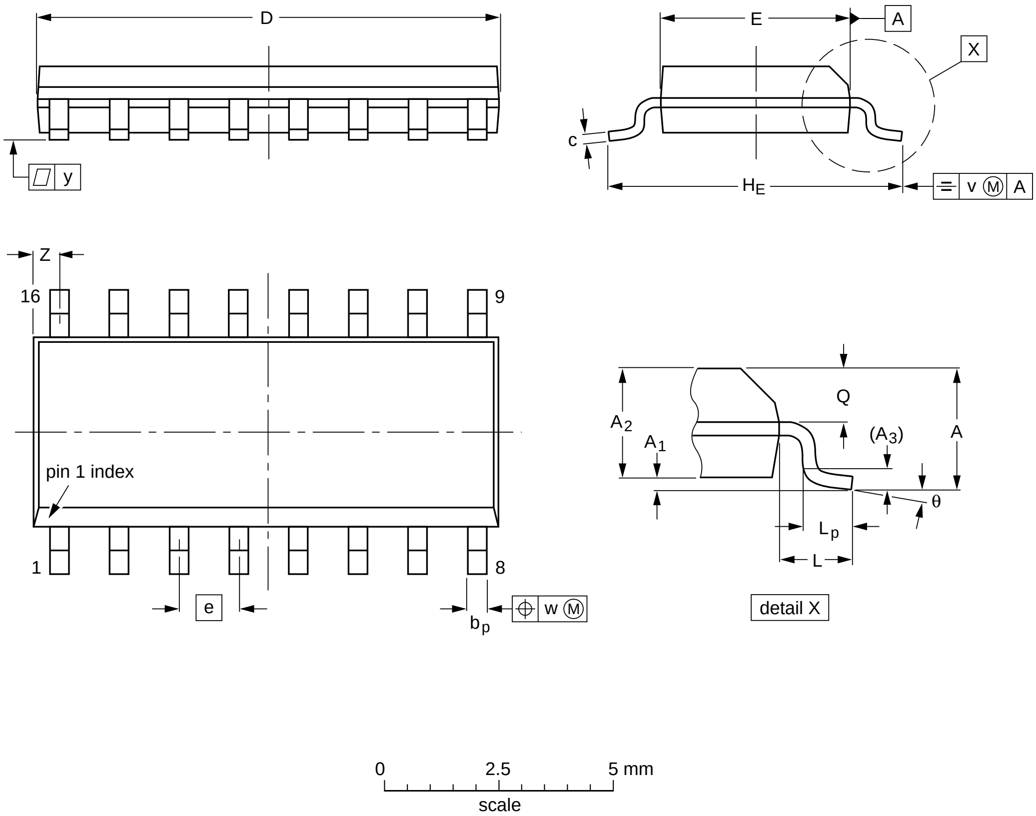
Fig 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
2.0 V to 5.5 V	V_{CC}	3.0 ns	50 pF, 15 pF	1 kΩ	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

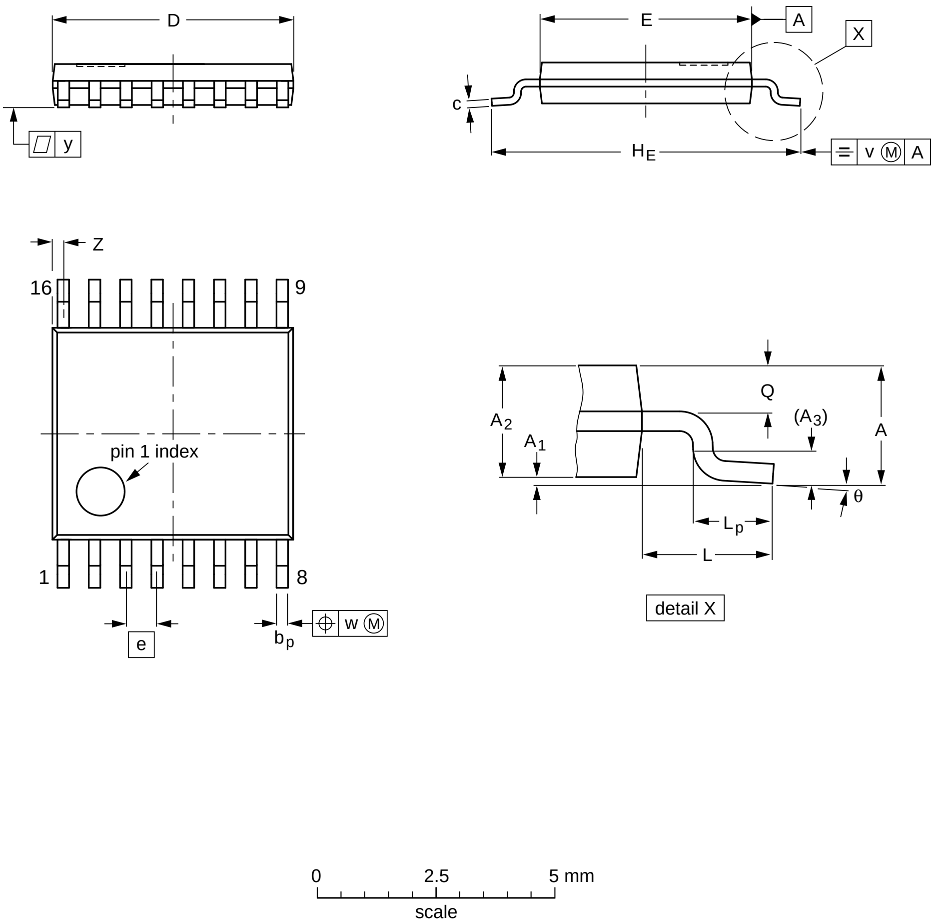
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV165A v.2	20130904	Product data sheet	-	74LV165A_CNV_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Family data added, see Section 9 “Static characteristics”			
74LV165A_CNV_1	December 1990	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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