

# 74LVC132A-Q100

## Quad 2-input NAND Schmitt trigger

Rev. 1 — 4 April 2013

Product data sheet

### 1. General description

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The 74LVC132A-Q100 provides four 2-input NAND gates with Schmitt trigger inputs. It can transform slowly changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the input hysteresis voltage  $V_H$ .

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environment.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.2 V to 3.6 V
- 5 V tolerant inputs for interfacing with 5 V logic
- CMOS low-power consumption
- Direct interface with TTL levels
- Unlimited input rise and fall times
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- Multiple package options

### 3. Applications

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- Wave and pulse shapers for highly noisy environments
- Astable multivibrator
- Monostable multivibrator.



4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC132AD-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC132APW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC132ABQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

mna212

Fig 1. Logic symbol

mna246

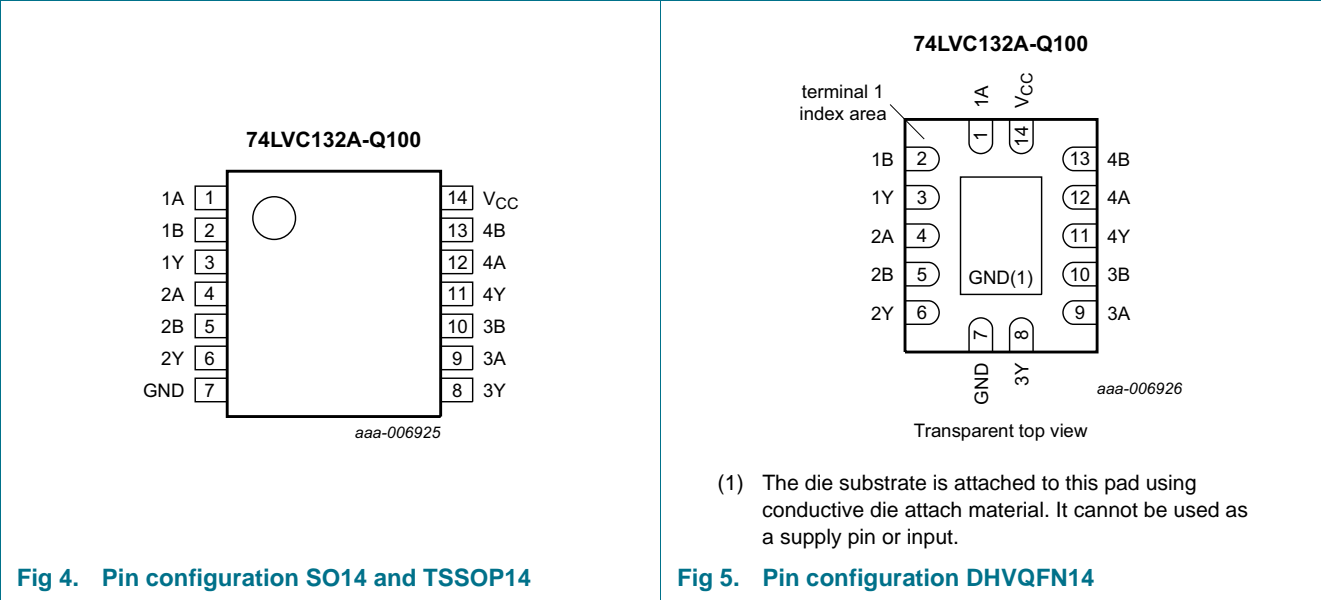
Fig 2. IEC logic symbol

001aac532

Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;  
L = LOW voltage level.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$V_I$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$V_O$	output voltage		<sup>[2][3]</sup> -0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<sup>[4]</sup> -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 3.6 V in normal operation.

[4] For SO14 packages:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
For TSSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
For DHVQFN14 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> - 0.45	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	µA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	pF
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	-	±20	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	5	mA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{pd}$	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		$V_{CC} = 1.2\text{ V}$	-	18.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.0	7.2	12.8	2.0	16.0	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	4.0	7.6	1.5	9.6	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.8	7.6	1.5	9.6	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.4	6.4	1.5	8.0	ns
$t_{sk(o)}$	output skew time	<sup>[3]</sup>	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$ <sup>[4]</sup>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	10.5	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	10.8	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	11.4	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}$ , and  $3.3\text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

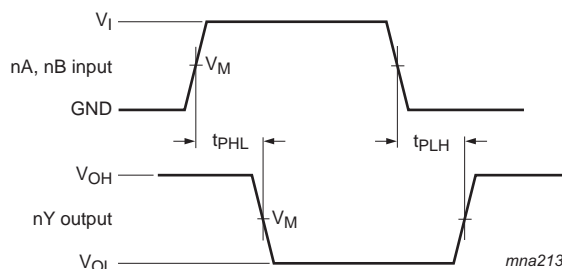
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 12. Waveforms

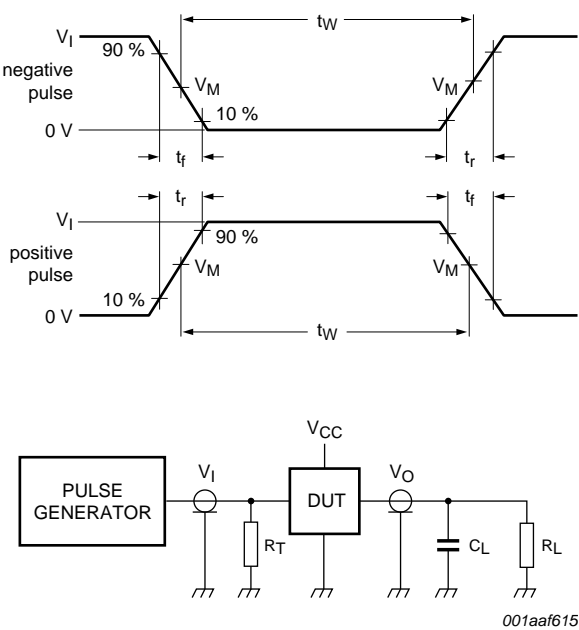


$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The input (nA, nB) to output (nY) propagation delays**



Test data is given in [Table 8](#). Definitions for test circuit:  
 $R_L$  = Load resistance  
 $C_L$  = Load capacitance including jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Load circuitry for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$

### 13. Transfer characteristics

**Table 9. Transfer characteristics**

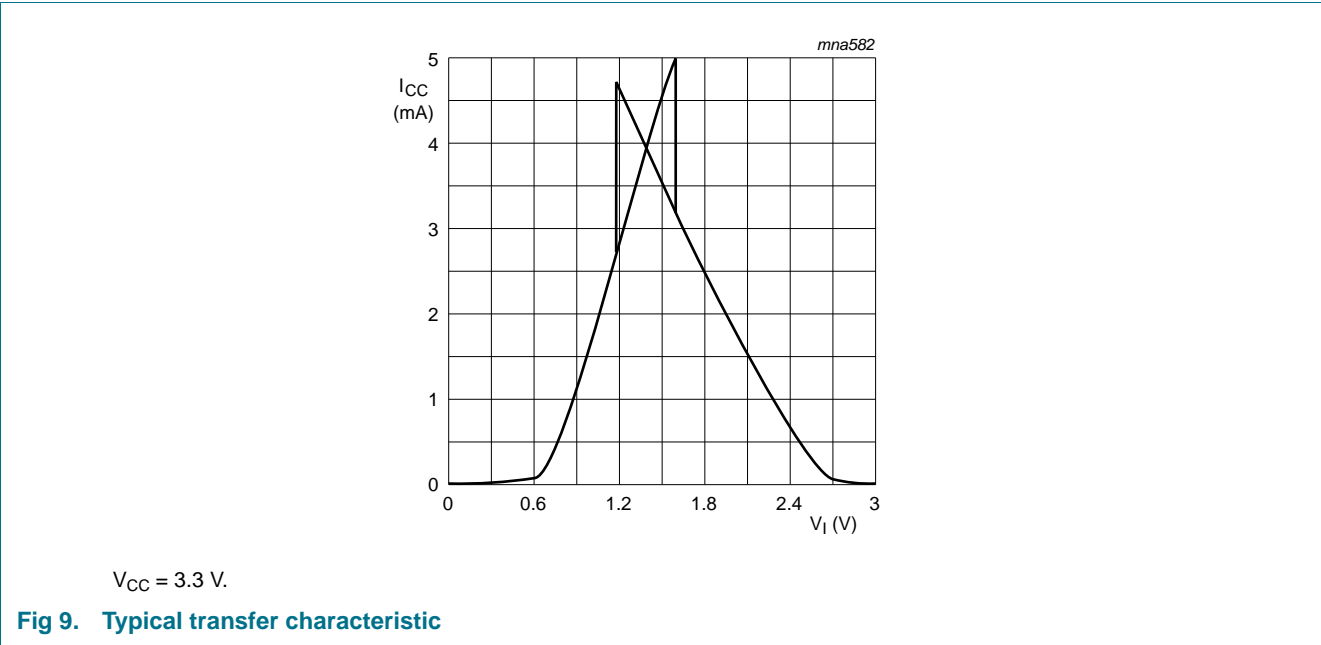
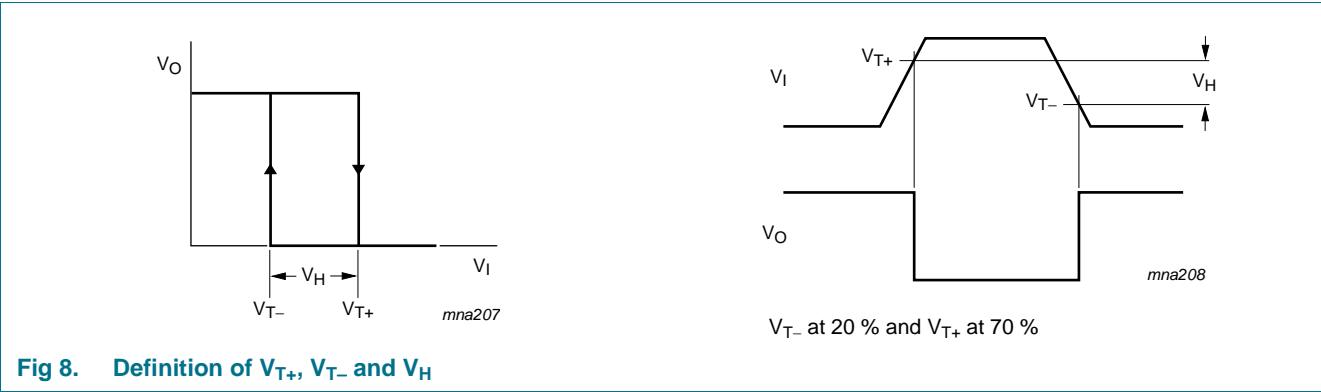
Voltages are referenced to GND (ground = 0 V); see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 1.2 V	0.2	1.0	0.2	1.0	V
		V <sub>CC</sub> = 1.65 V	0.4	1.3	0.4	1.3	V
		V <sub>CC</sub> = 1.95 V	0.6	1.5	0.6	1.5	V
		V <sub>CC</sub> = 2.3 V	0.8	1.7	0.8	1.7	V
		V <sub>CC</sub> = 2.5 V	0.9	1.7	0.9	1.7	V
		V <sub>CC</sub> = 2.7 V	1.1	2	1.1	2	V
		V <sub>CC</sub> = 3 V	1.2	2	1.2	2	V
		V <sub>CC</sub> = 3.6 V	1.2	2	1.2	2	V
V <sub>T–</sub>	negative-going threshold voltage	V <sub>CC</sub> = 1.2 V	0.12	0.75	0.12	0.75	V
		V <sub>CC</sub> = 1.65 V	0.15	0.85	0.15	0.85	V
		V <sub>CC</sub> = 1.95 V	0.25	0.95	0.25	0.95	V
		V <sub>CC</sub> = 2.3 V	0.4	1.1	0.4	1.1	V
		V <sub>CC</sub> = 2.5 V	0.4	1.2	0.4	1.2	V
		V <sub>CC</sub> = 2.7 V	0.8	1.4	0.8	1.4	V
		V <sub>CC</sub> = 3 V	0.8	1.5	0.8	1.5	V
		V <sub>CC</sub> = 3.6 V	0.8	1.5	0.8	1.5	V
V <sub>H</sub>	hysteresis voltage	(V <sub>T+</sub> – V <sub>T–</sub> )					
		V <sub>CC</sub> = 1.2 V	0.1	1.0	0.1	1.0	V
		V <sub>CC</sub> = 1.65 V	0.2	1.15	0.2	1.15	V
		V <sub>CC</sub> = 1.95 V	0.2	1.25	0.2	1.25	V
		V <sub>CC</sub> = 2.3 V	0.3	1.3	0.3	1.3	V
		V <sub>CC</sub> = 2.5 V	0.3	1.3	0.3	1.3	V
		V <sub>CC</sub> = 2.7 V	0.3	1.1	0.3	1.1	V
		V <sub>CC</sub> = 3 V	0.3	1.2	0.3	1.2	V
		V <sub>CC</sub> = 3.6 V <a href="#">[1]</a>	0.3	1.2	0.3	1.2	V

[1] Typical transfer characteristic is displayed in [Figure 9](#).



14. Waveforms transfer characteristics



15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

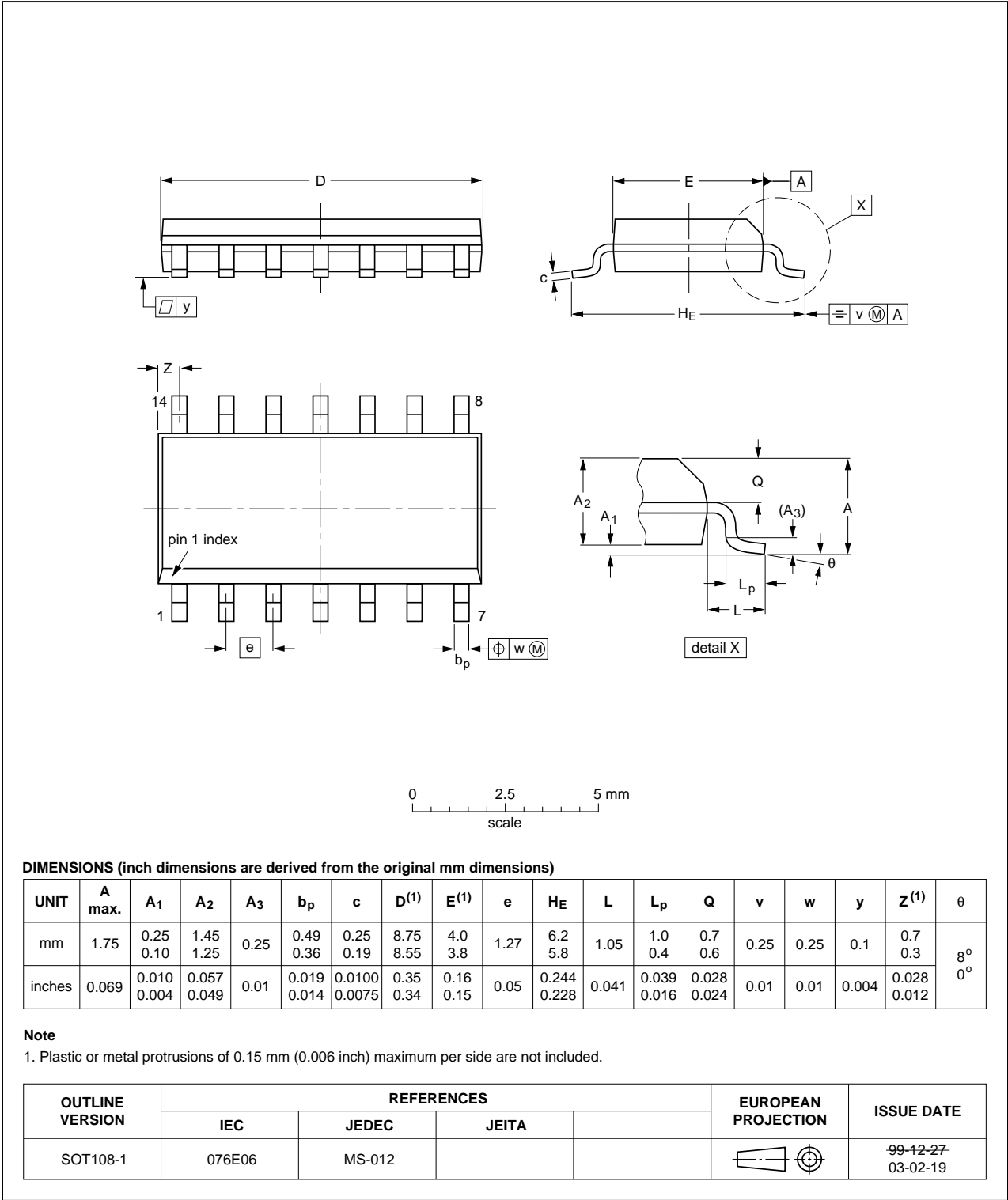


Fig 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

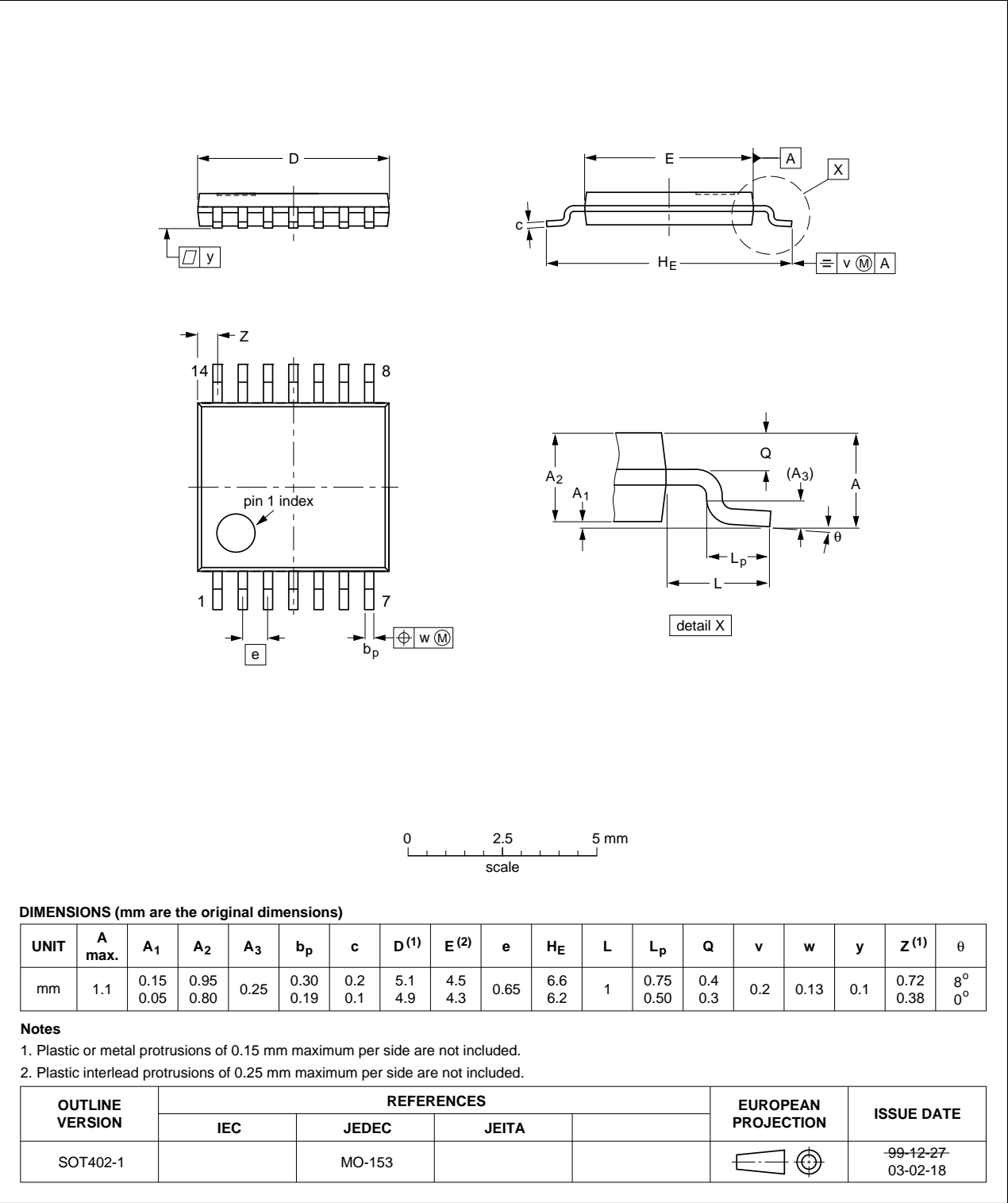


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

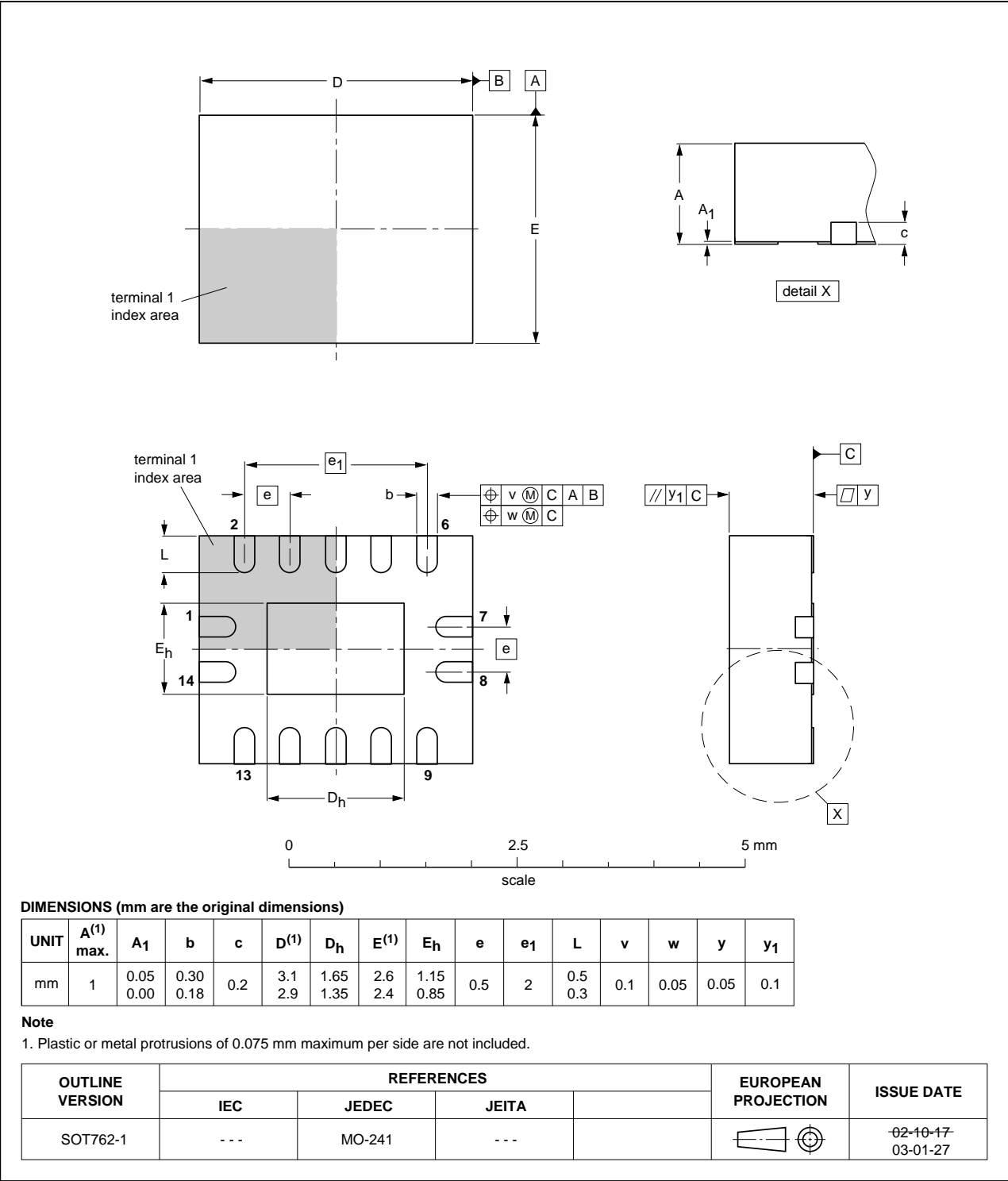


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 16. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 17. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC132A_Q100 v.1	20130404	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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