

74LVC1G123

Single retriggerable monostable multivibrator; Schmitt trigger inputs

Rev. 4 — 27 November 2013

Product data sheet

1. General description

The 74LVC1G123 is a single retriggerable monostable multivibrator with Schmitt trigger inputs. Output pulse width is controlled by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (\overline{A}) or the active HIGH-going edge input (B). By repeating this process, the output pulse period ($Q = \text{HIGH}$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input \overline{CLR} , which also inhibits the triggering.
3. An internal connection from \overline{CLR} to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input \overline{CLR} .

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment. Schmitt trigger inputs, makes the circuit highly tolerant to slower input rise and fall times.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt trigger on all inputs
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- Power-on-reset on outputs
- Latch-up performance exceeds 100 mA
- Direct interface with TTL levels



- Inputs accept voltages up to 5.5 V
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G123DP	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G123DC	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC1G123GT	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5\text{ mm}$	SOT833-1
74LVC1G123GF	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8	extremely thin small outline package; no leads; 8 terminals; body $1.35 \times 1 \times 0.5\text{ mm}$	SOT1089
74LVC1G123GD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5\text{ mm}$	SOT996-2
74LVC1G123GN	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8	extremely thin small outline package; no leads; 8 terminals; body $1.2 \times 1.0 \times 0.35\text{ mm}$	SOT1116
74LVC1G123GS	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8	extremely thin small outline package; no leads; 8 terminals; body $1.35 \times 1.0 \times 0.35\text{ mm}$	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC1G123DP	Y3
74LVC1G123DC	Y3
74LVC1G123GT	Y3
74LVC1G123GF	Y3
74LVC1G123GD	Y3
74LVC1G123GN	Y3
74LVC1G123GS	Y3

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

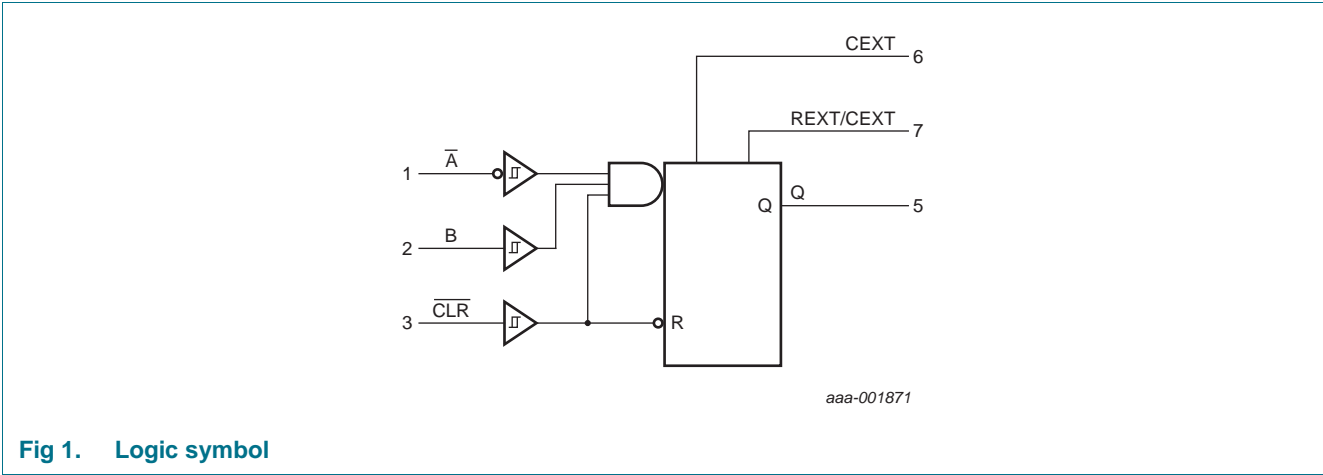


Fig 1. Logic symbol

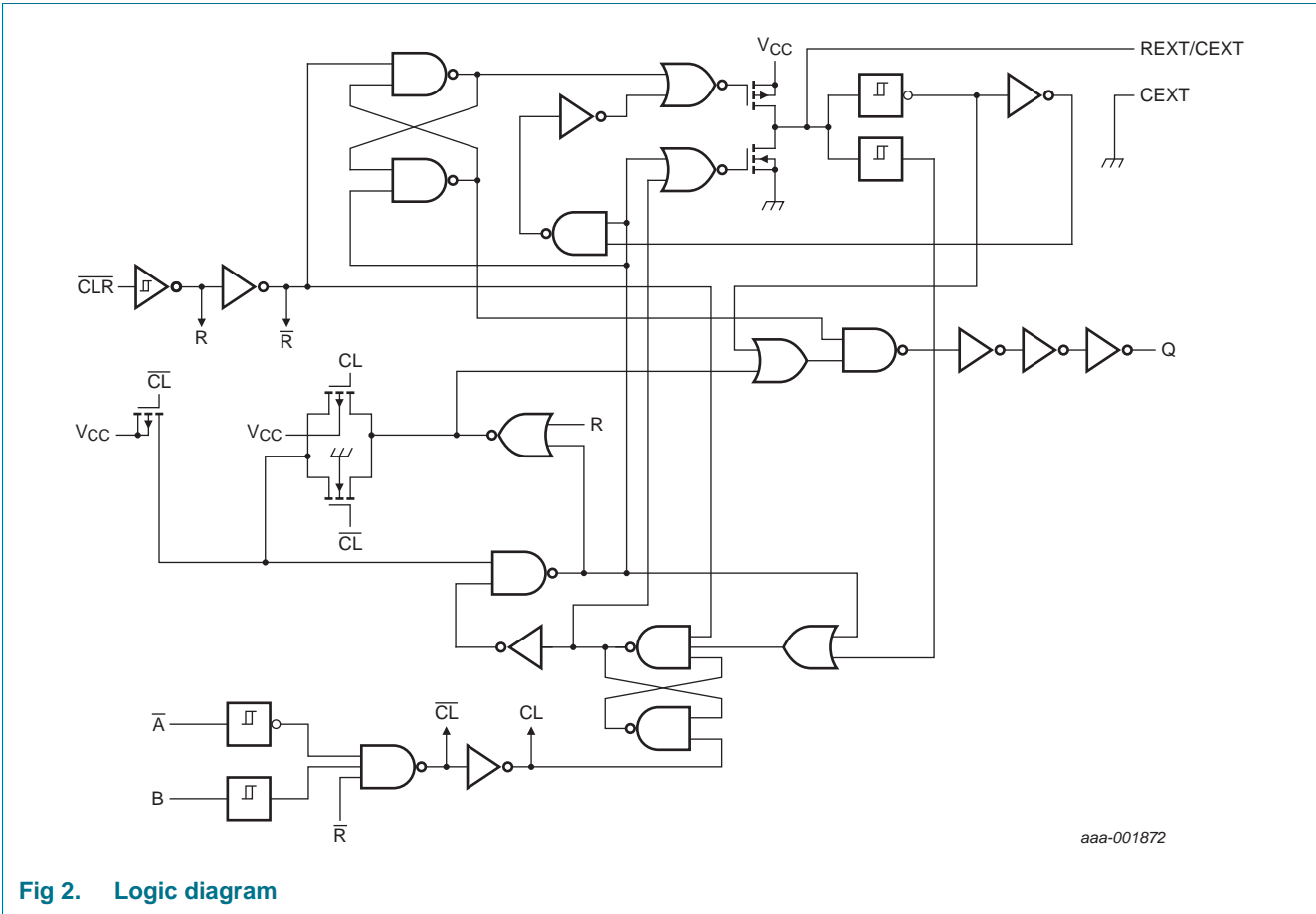
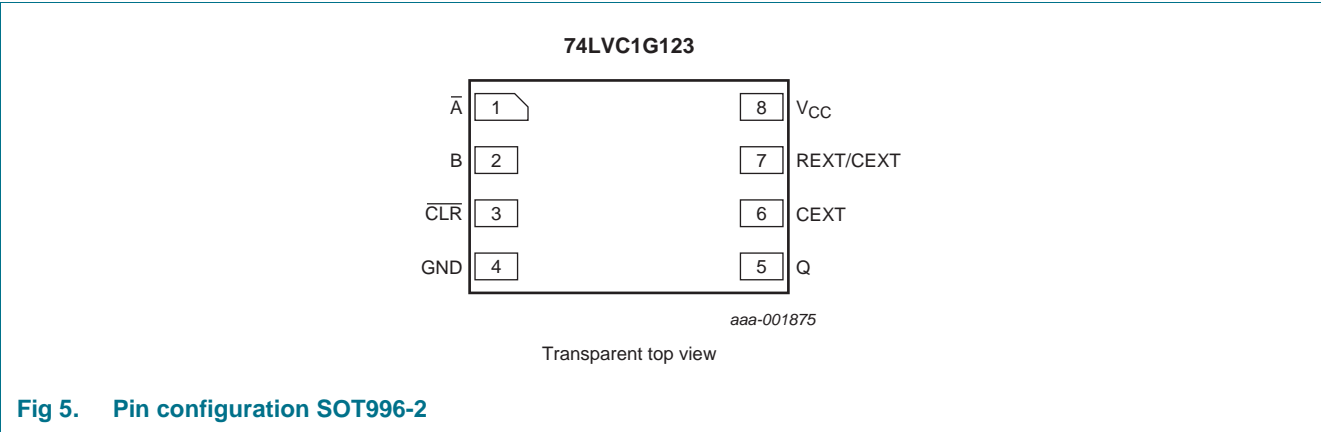
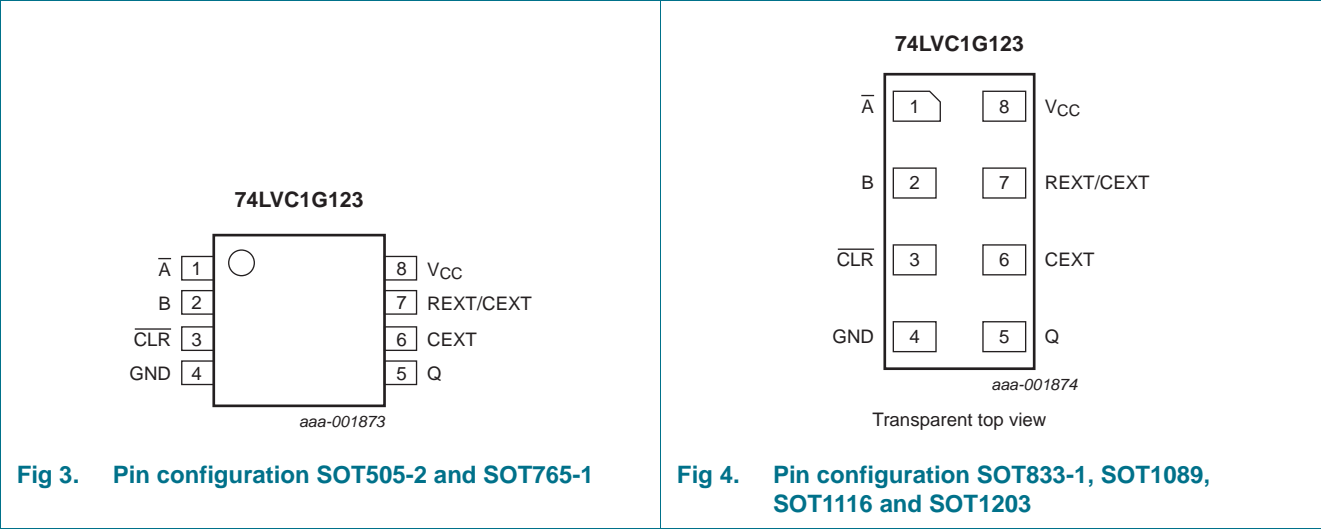


Fig 2. Logic diagram

6. Pinning information

6.1 Pinning






6.2 Pin description

Table 3. Pin description



Symbol	Pin	Description
\overline{A}	1	negative-edge triggered input
B	2	positive-edge triggered input
\overline{CLR}	3	direct reset LOW and positive-edge triggered input
GND	4	ground (0 V)
Q	5	active HIGH output
CEXT	6	external capacitor connection
REXT/CEXT	7	external resistor and capacitor connection
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input			Output
\overline{CLR}	\overline{A}	B	Q
L	X	X	L
X	H	X	L ^[2]
X	X	L	L ^[2]
H	L	↑	
H	↓	H	
↑	L	H	

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;  = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse continues as programmed.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		[1] -0.5	+6.5	V
V_O	output voltage	Active mode	[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode	[1][2] -0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 5.5 V	-	1	ms/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.4	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±2	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND;				
		Quiescent; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	10	µA
		Active state; R _{EXT} /C _{EXT} = 0.5V _{CC}				
		V _{CC} = 1.65 V	-	-	80	µA
		V _{CC} = 2.3 V	-	-	130	µA
		V _{CC} = 3 V	-	-	240	µA
		V _{CC} = 4.5 V	-	-	400	µA
		V _{CC} = 5.5 V	-	-	650	µA
C _I	input capacitance		-	2.0	-	pF

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.4	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±10	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±10	µA
I _{CC}	supply current	V _I = 5.5 V or GND;				
		Quiescent; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	-	20	µA
		Active state; R _{EXT} /C _{EXT} = 0.5V _{CC}				
		V _{CC} = 1.65 V	-	-	80	µA
		V _{CC} = 2.3 V	-	-	130	µA
		V _{CC} = 3 V	-	-	240	µA
		V _{CC} = 4.5 V	-	-	400	µA
		V _{CC} = 5.5 V	-	-	650	µA

[1] All typical values are measured at T_{amb} = 25 °C.

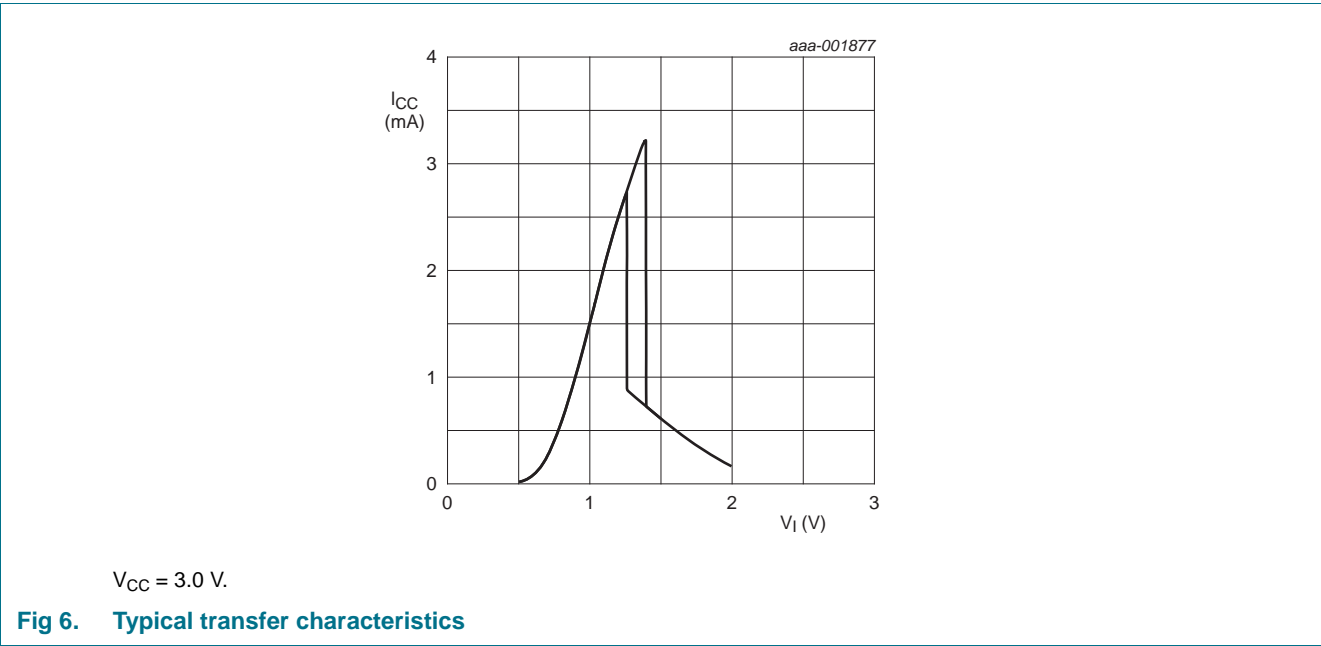
Table 8. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{T+}	positive-going threshold voltage	\overline{A} , B and \overline{CLR} input; see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	0.72	0.98	1.22	0.71	1.22	V
		V _{CC} = 2.3 V to 2.7 V	0.97	1.26	1.52	0.97	1.52	V
		V _{CC} = 3.0 V to 3.6 V	1.20	1.58	1.90	1.20	1.90	V
		V _{CC} = 4.5 V to 5.5 V	1.74	2.27	2.75	1.74	2.78	V
V _{T−}	negative-going threshold voltage	\overline{A} , B and \overline{CLR} input; see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	0.56	0.81	1.04	0.56	1.04	V
		V _{CC} = 2.3 V to 2.7 V	0.83	1.09	1.33	0.82	1.33	V
		V _{CC} = 3.0 V to 3.6 V	1.08	1.40	1.70	1.08	1.72	V
		V _{CC} = 4.5 V to 5.5 V	1.61	2.07	2.53	1.61	2.57	V
V _H	hysteresis voltage	\overline{A} , B and \overline{CLR} input; (V _{T+} − V _{T−}); see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	61	170	295	54	295	mV
		V _{CC} = 2.3 V to 2.7 V	41	174	304	41	304	mV
		V _{CC} = 3.0 V to 3.6 V	40	183	319	40	319	mV
		V _{CC} = 4.5 V to 5.5 V	32	199	363	26	363	mV

[1] All typical values are measured at T_{amb} = 25 °C

10.1 Waveform transfer characteristics



11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	\overline{A} , B to Q; see Figure 7 ^[2]						
		$C_L = 15 \text{ pF}$;						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.5	7.1	16.3	2.5	17.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.9	-	10.3	1.9	11.2	ns
		$V_{CC} = 2.7 \text{ V}$	1.9	-	8.5	1.9	9.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	7.6	1.5	8.3	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.2	-	5.3	1.2	5.8	ns
		$C_L = 30 \text{ pF or } C_L = 50 \text{ pF}$						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.9	7.8	17.6	2.9	19.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.2	-	11.3	2.2	12.3	ns
		$V_{CC} = 2.7 \text{ V}$	2.7	-	10.5	2.7	11.4	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	9.5	2.0	10.3	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.5	-	6.7	1.5	7.2	ns
		\overline{CLR} to Q; see Figure 7						
		$C_L = 15 \text{ pF}$;						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.0	6.9	16.2	3.0	17.4	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.2	-	9.6	2.2	10.5	ns
		$V_{CC} = 2.7 \text{ V}$	2.2	-	8.2	2.2	8.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	7.3	2.0	8.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.5	-	5.1	1.5	5.5	ns
		$C_L = 30 \text{ pF or } C_L = 50 \text{ pF}$						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.3	7.5	17.2	3.8	18.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.5	-	10.3	2.0	11.2	ns
		$V_{CC} = 2.7 \text{ V}$	2.8	-	9.3	2.8	10.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	8.4	1.5	9.2	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.5	-	6.0	1.5	6.6	ns

Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	CLR to Q (trigger); see Figure 7						
		$C_L = 15 \text{ pF}$;						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.7	7.6	17.4	2.7	18.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.1	-	11.0	2.1	12.0	ns
		$V_{CC} = 2.7 \text{ V}$	2.1	-	9.2	2.1	10.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.7	-	8.2	1.7	8.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.4	-	5.9	1.4	6.4	ns
		$C_L = 30 \text{ pF or } C_L = 50 \text{ pF}$						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.1	8.3	18.8	3.3	20.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.5	-	12.0	2.5	13.1	ns
		$V_{CC} = 2.7 \text{ V}$	2.8	-	11.1	2.8	12.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	10.1	2.0	11.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.5	-	7.1	1.5	7.7	ns
t_W	pulse width	input \overline{A} LOW; B HIGH; see Figure 7 and Figure 8						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	8.0	-	-	8.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.5	-	-	2.5	-	ns
		input \overline{CLR} LOW; see Figure 7 and Figure 9						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	8.0	-	-	8.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.5	-	-	2.5	-	ns

Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_W	pulse width	output Q HIGH; see Figure 7 , Figure 8 and Figure 9 ; $R_{EXT} = 10\text{ k}\Omega$ $C_{EXT} = 100\text{ pF}$						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	1.4	2.2	-	2.2	μs
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	1.3	1.8	-	1.8	μs
		$V_{CC} = 2.7\text{ V}$	-	1.2	1.8	-	1.8	μs
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	1.2	1.8	-	1.8	μs
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	1.8	-	1.8	μs
		$C_{EXT} = 0.01\text{ }\mu\text{F}$						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	100	110	-	110	μs
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	100	110	-	110	μs
		$V_{CC} = 2.7\text{ V}$	-	100	110	-	110	μs
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	100	110	-	110	μs
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	100	110	-	110	μs
		$C_{EXT} = 0.1\text{ }\mu\text{F}$						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	1.0	1.05	-	1.05	ms
		$V_{CC} = 2.7\text{ V}$	-	1.0	1.05	-	1.05	ms
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	1.0	1.05	-	1.05	ms
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	1.0	1.05	-	1.05	ms
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.0	1.05	-	1.05	ms
t_{rtrig}	retrigger time	\bar{A} , B; see Figure 8 $C_{EXT} = 100\text{ pF}$; $R_{EXT} = 5\text{ k}\Omega$						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	174	-	-	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	59	-	-	-	ns
		$C_{EXT} = 100\text{ pF}$; $R_{EXT} = 1\text{ k}\Omega$						
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	32	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	20	-	-	-	ns
		$C_{EXT} = 100\text{ }\mu\text{F}$; $R_{EXT} = 5\text{ k}\Omega$						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	14	-	-	-	ms
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	10	-	-	-	ms
		$C_{EXT} = 100\text{ }\mu\text{F}$; $R_{EXT} = 1\text{ k}\Omega$						
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	10	-	-	-	ms
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	8	-	-	-	ms
R_{ext}	external resistance	see Figure 12 , Figure 13 and Figure 14 $V_{CC} = 2.0\text{ V}$	5	-	-	-	-	k Ω
		$V_{CC} \geq 3.0\text{ V}$	1	-	-	-	-	k Ω
		$V_{CC} = 5.0\text{ V}$; see Figure 12 , Figure 13 and Figure 14	-	-	-	-	-	pF

Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; C _{EXT} = 0 pF;						
		R _{EXT} = 5 kΩ						
		V _{CC} = 1.8 V	-	35	-	-	-	pF
		V _{CC} = 2.5 V	-	35	-	-	-	pF
		R _{EXT} = 1 kΩ						
		V _{CC} = 3.3 V	-	27	-	-	-	pF
		V _{CC} = 5.0 V	-	29	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}; t_i is the same as t_{THL} and t_{TLH}

[3] For other R_{EXT} and C_{EXT} combinations see [Figure 12](#), [Figure 13](#) and [Figure 14](#). If C_{EXT} > 10 nF, the next formula is valid.

t_W = K × R_{EXT} × C_{EXT}, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = constant = 1; see [Figure 15](#) for typical "K" factor as function of V_{CC}.

12. Waveforms, graphs and test circuit

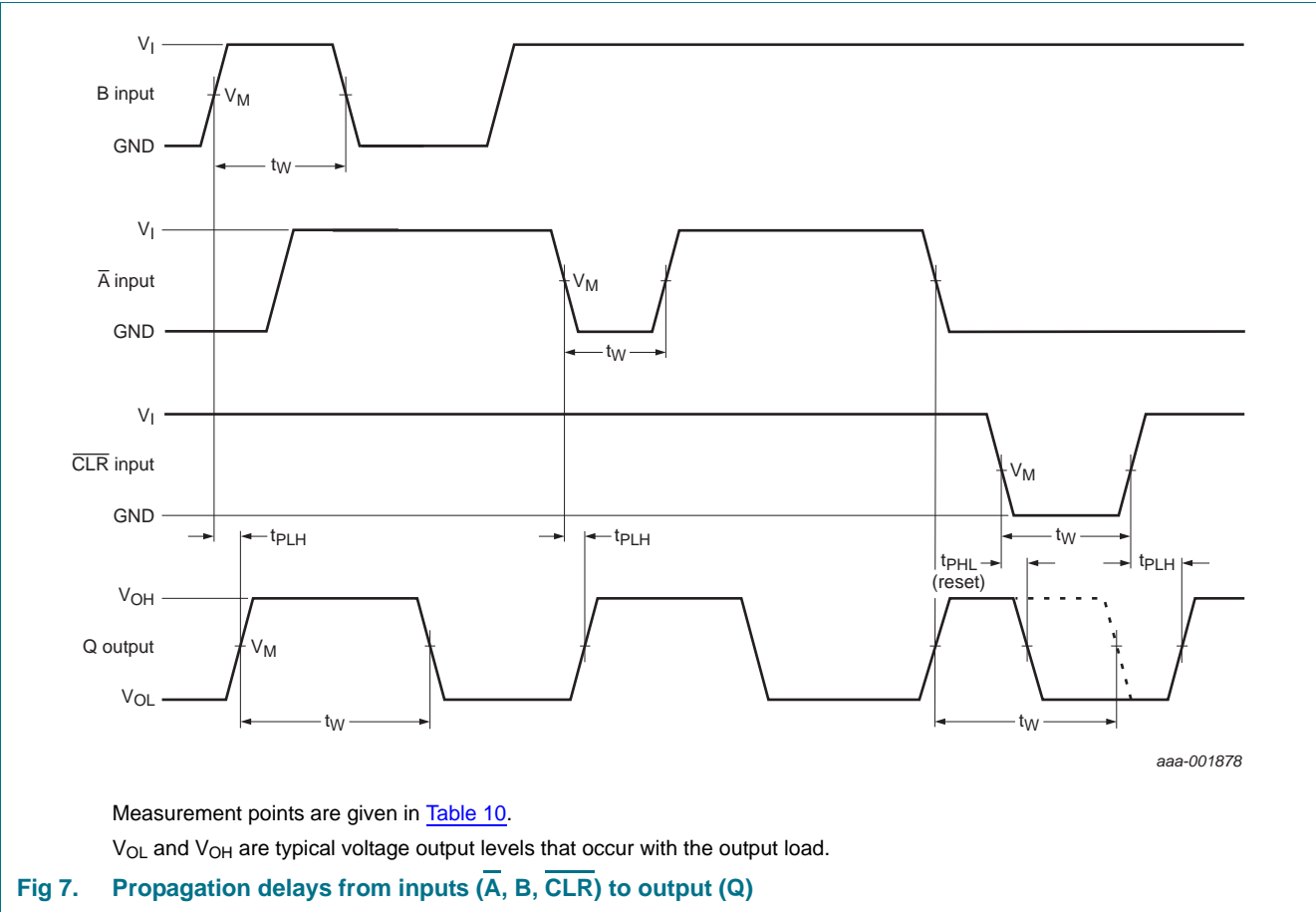
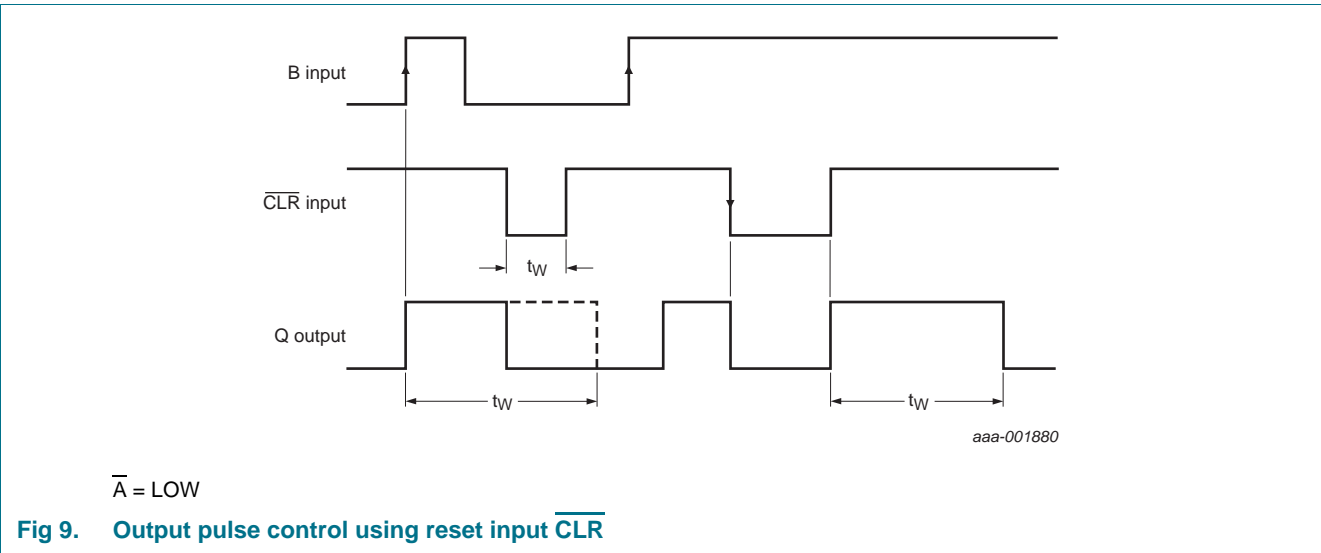
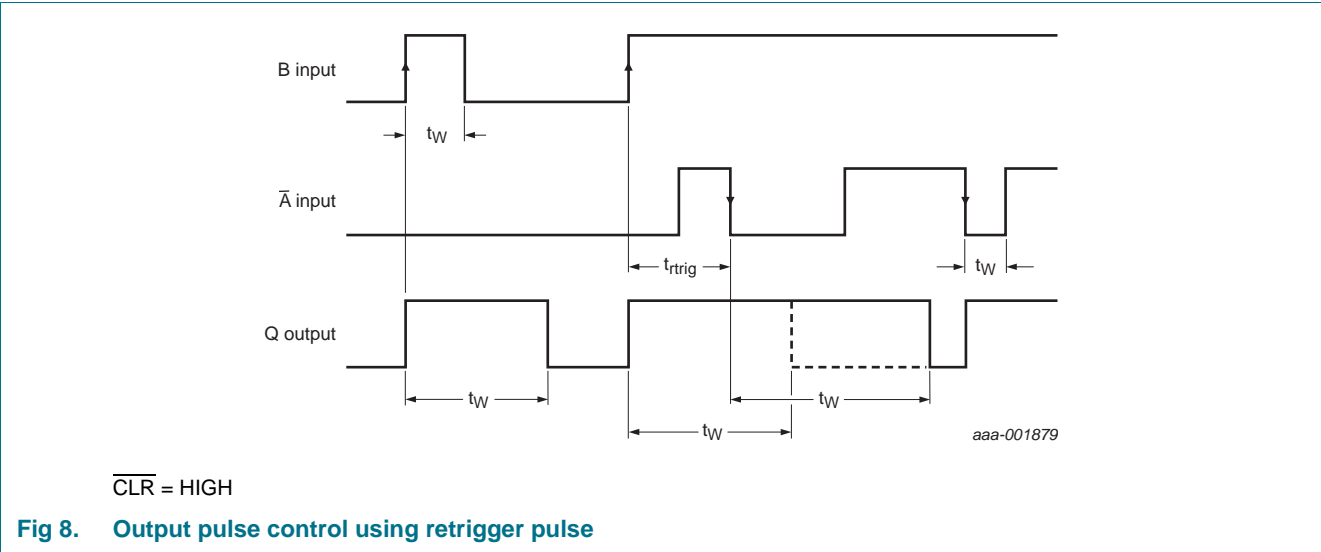


Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



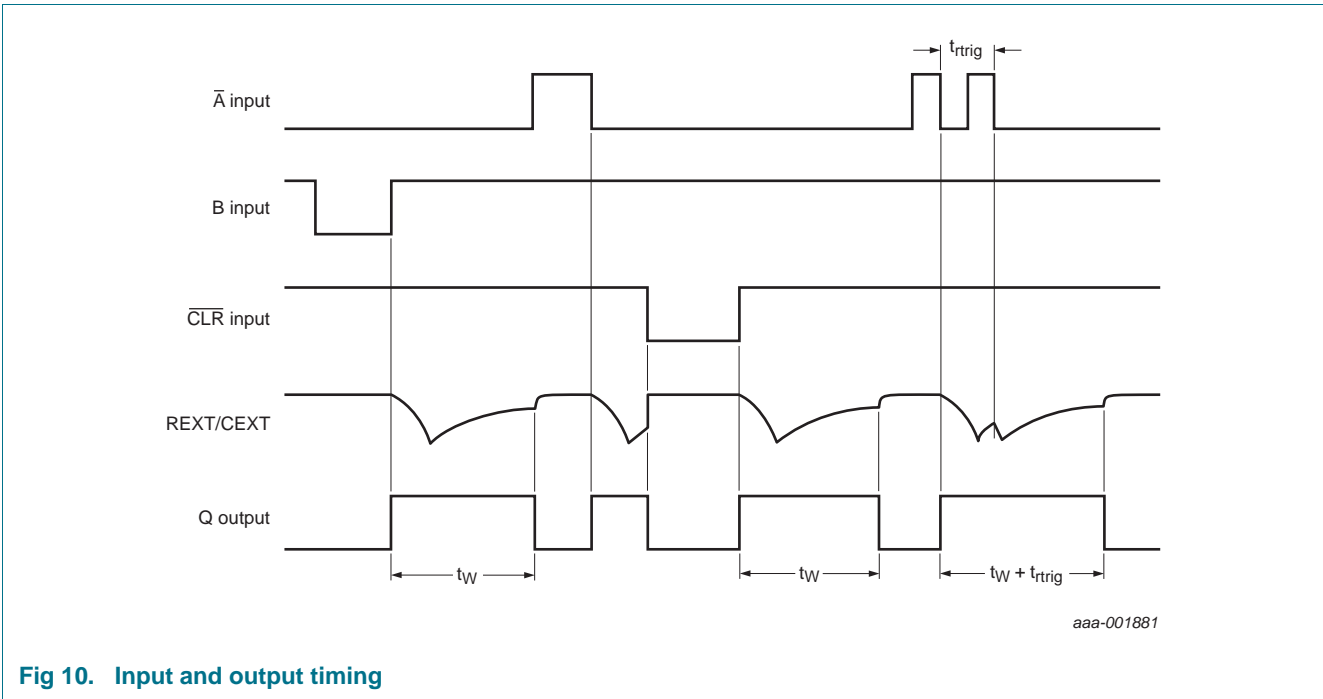


Fig 10. Input and output timing

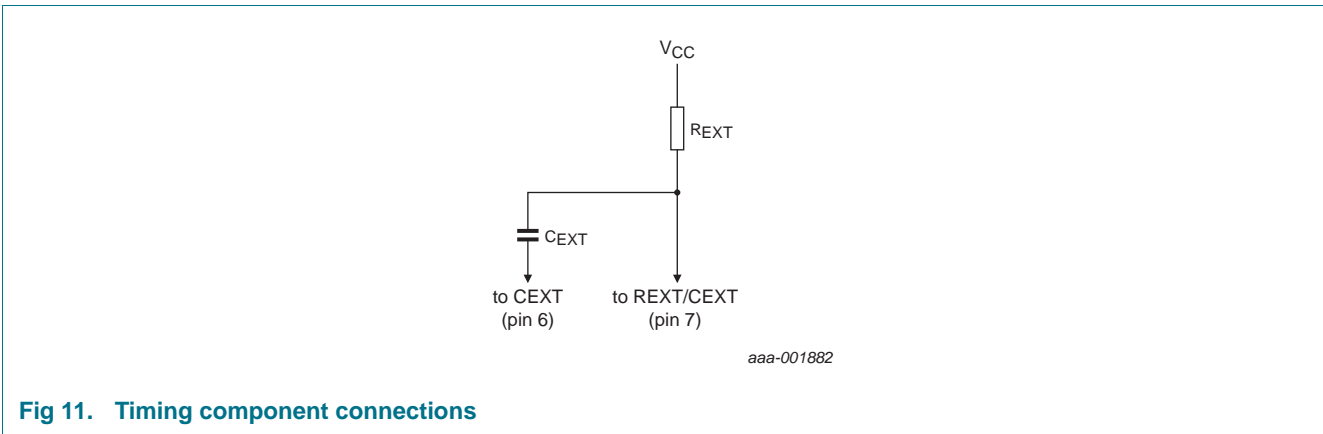
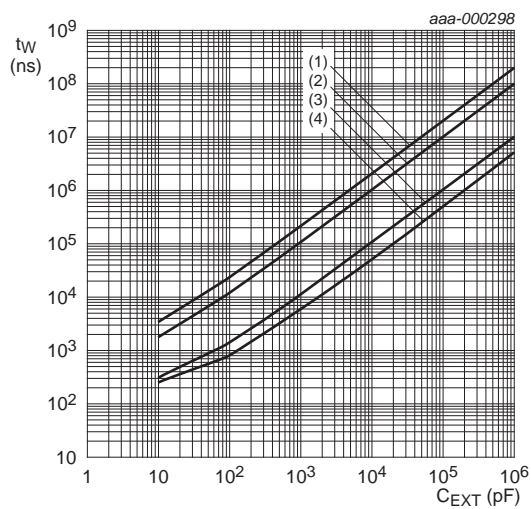


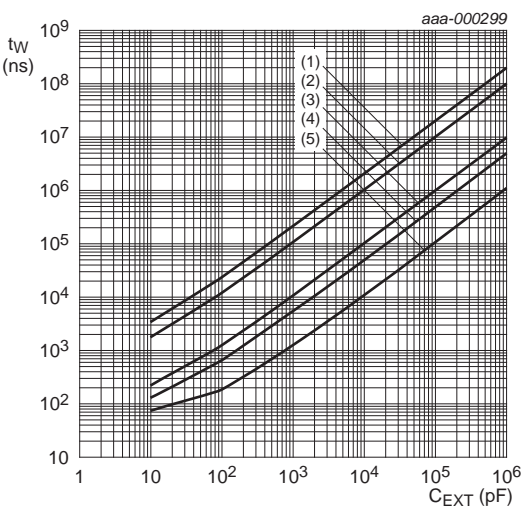
Fig 11. Timing component connections



$V_{CC} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

- (1) $R_{EXT} = 200\text{ k}\Omega$
- (2) $R_{EXT} = 100\text{ k}\Omega$
- (3) $R_{EXT} = 10\text{ k}\Omega$
- (4) $R_{EXT} = 5\text{ k}\Omega$

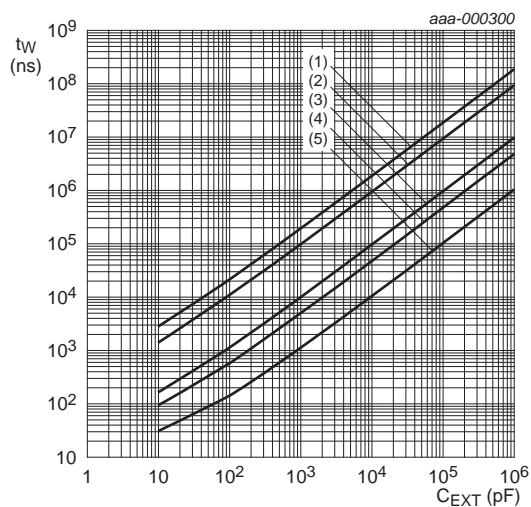
Fig 12. Typical output pulse width as a function of the external capacitor value



$V_{CC} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

- (1) $R_{EXT} = 200\text{ k}\Omega$
- (2) $R_{EXT} = 100\text{ k}\Omega$
- (3) $R_{EXT} = 10\text{ k}\Omega$
- (4) $R_{EXT} = 5\text{ k}\Omega$
- (5) $R_{EXT} = 1\text{ k}\Omega$

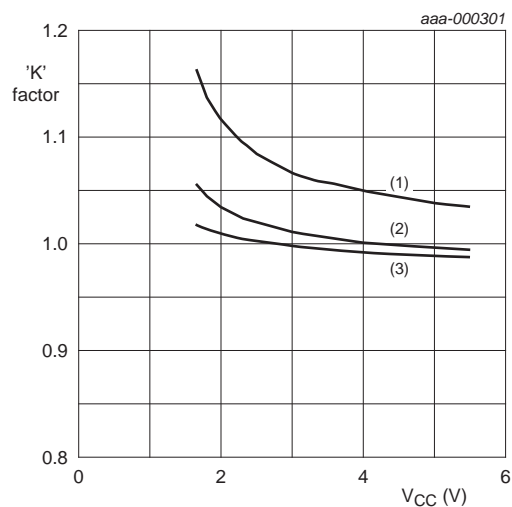
Fig 13. Typical output pulse width as a function of the external capacitor value



$V_{CC} = 5.0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

- (1) $R_{EXT} = 200 \text{ k}\Omega$
- (2) $R_{EXT} = 100 \text{ k}\Omega$
- (3) $R_{EXT} = 10 \text{ k}\Omega$
- (4) $R_{EXT} = 5 \text{ k}\Omega$
- (5) $R_{EXT} = 1 \text{ k}\Omega$

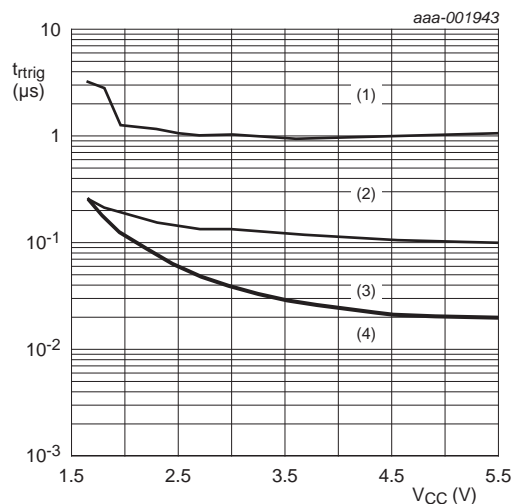
Fig 14. Typical output pulse width as a function of the external capacitor value



$R_{EXT} = 10 \text{ k}\Omega$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

- (1) $C_{EXT} = 1000 \text{ pF}$
- (2) $C_{EXT} = 0.01 \text{ }\mu\text{F}$
- (3) $C_{EXT} = 0.1 \text{ }\mu\text{F}$

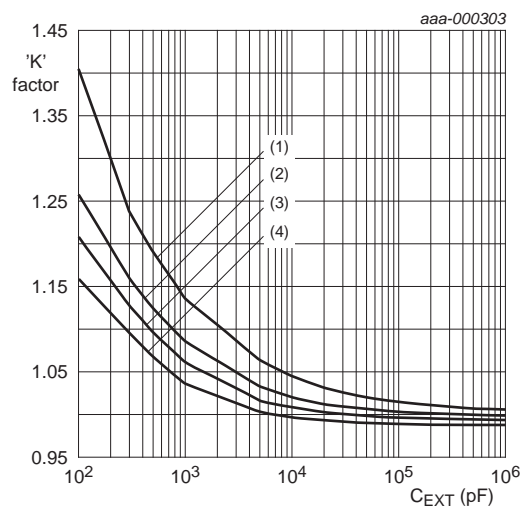
Fig 15. Typical 'K' factor as function of V_{CC}



$T_{amb} = 25 \text{ }^{\circ}\text{C}$.

- (1) $C_{EXT} = 0.01 \text{ }\mu\text{F}$
- (2) $C_{EXT} = 1000 \text{ pF}$
- (3) $C_{EXT} = 100 \text{ pF}$
- (4) $C_{EXT} = 10 \text{ pF}$

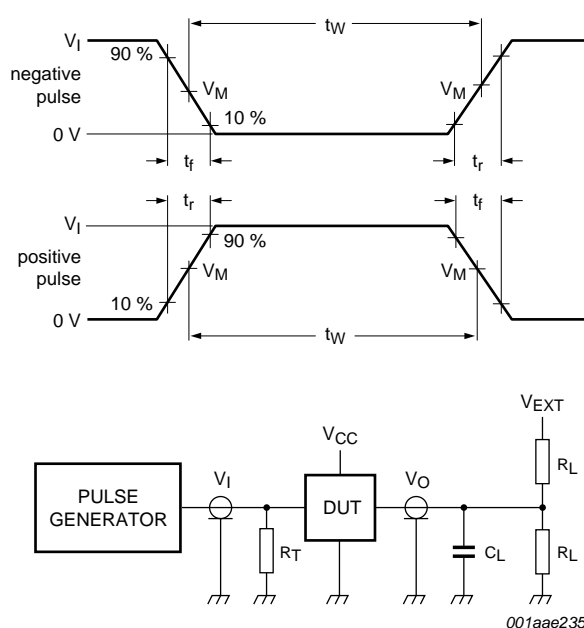
Fig 16. Minimum retrigger time as function of the supply voltage



$R_{EXT} = 10 \text{ k}\Omega$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

- (1) $V_{CC} = 1.8 \text{ V}$
- (2) $V_{CC} = 2.5 \text{ V}$
- (3) $V_{CC} = 3.3 \text{ V}$
- (4) $V_{CC} = 5.0 \text{ V}$

Fig 17. Typical 'K' factor as function of C_{EXT}



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	15 pF	1 M Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	15 pF	1 M Ω	open
2.7 V	2.7 V	≤ 2.5 ns	15 pF	1 M Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF	1 M Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	15 pF	1 M Ω	open
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

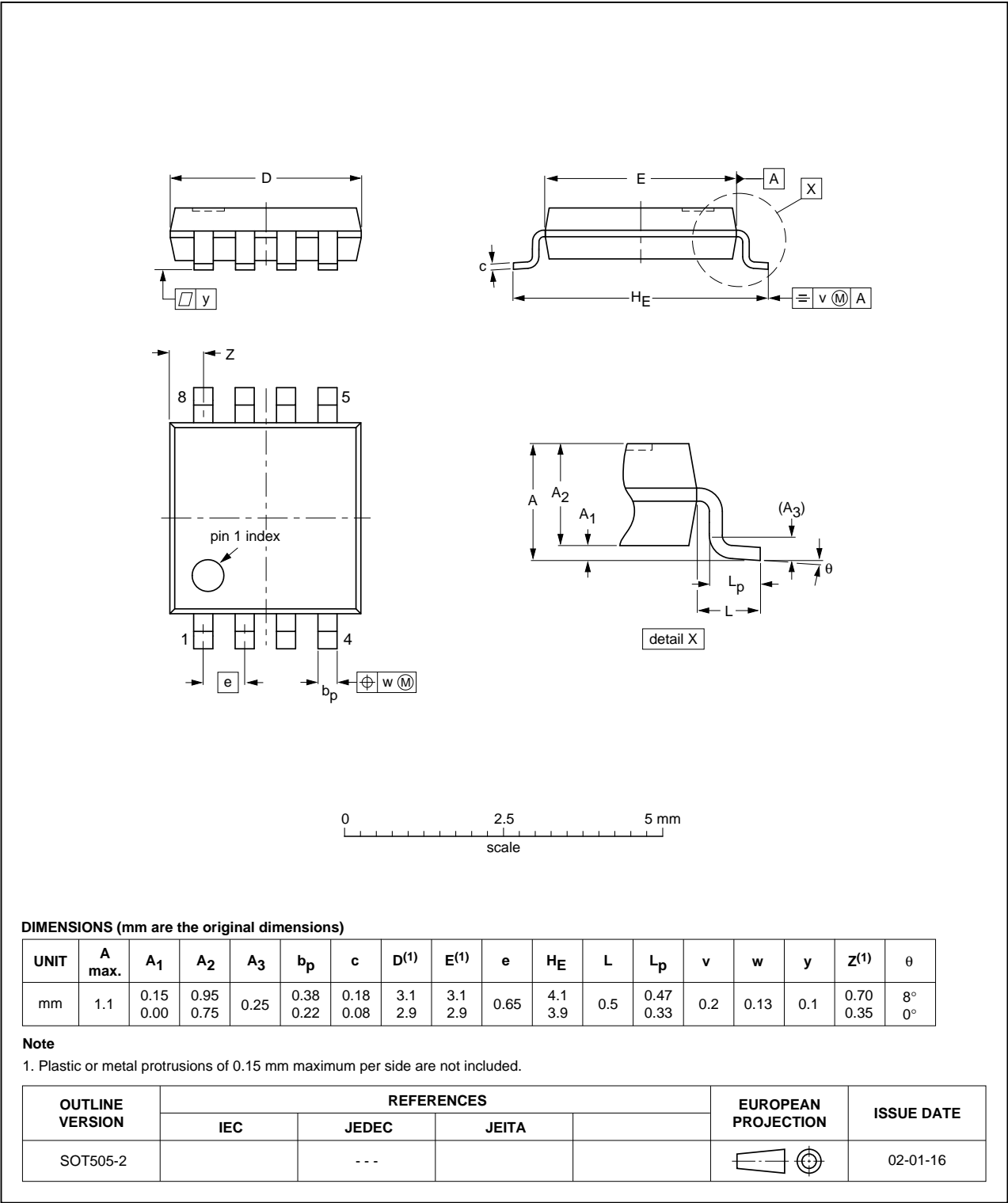


Fig 19. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

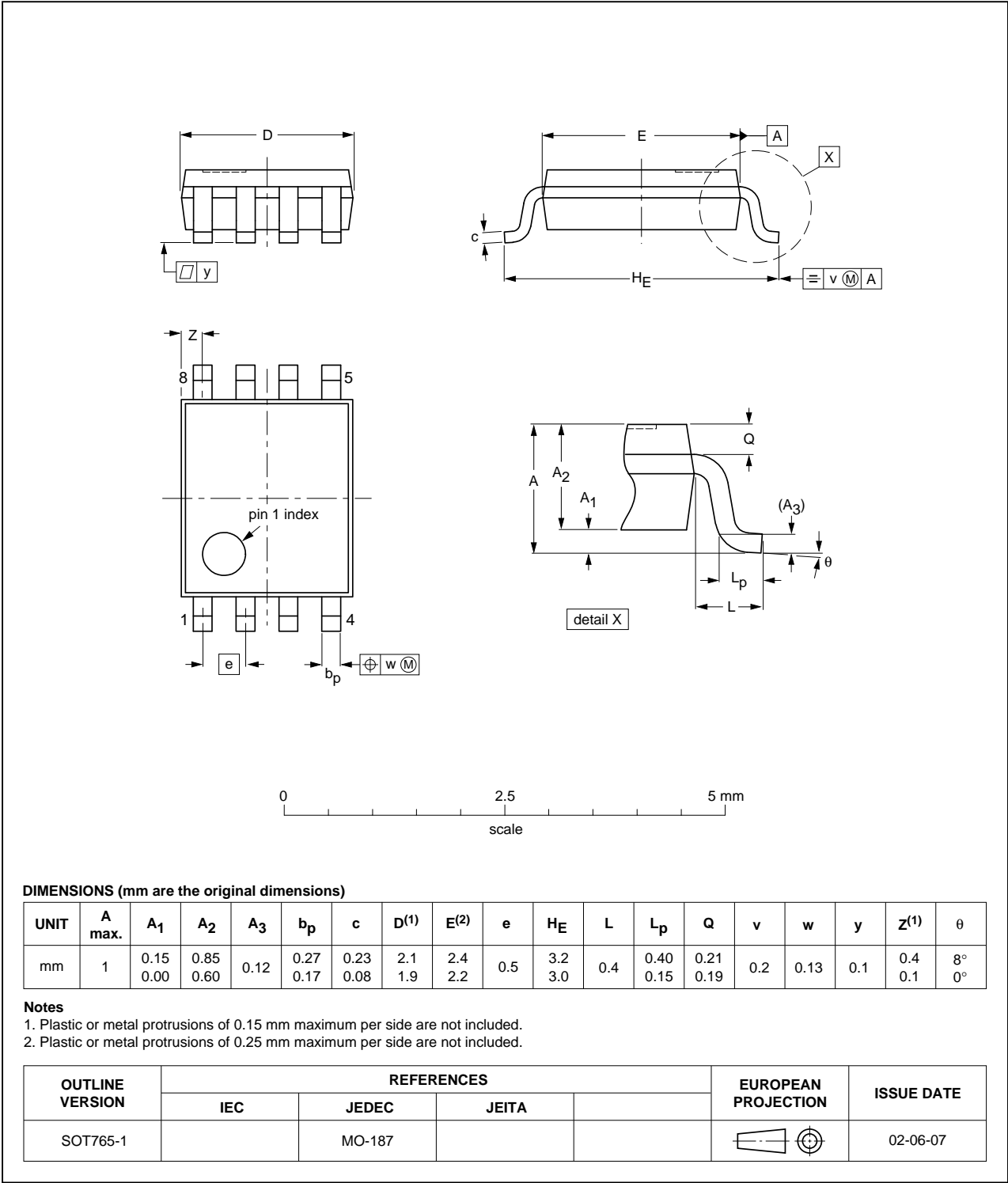


Fig 20. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

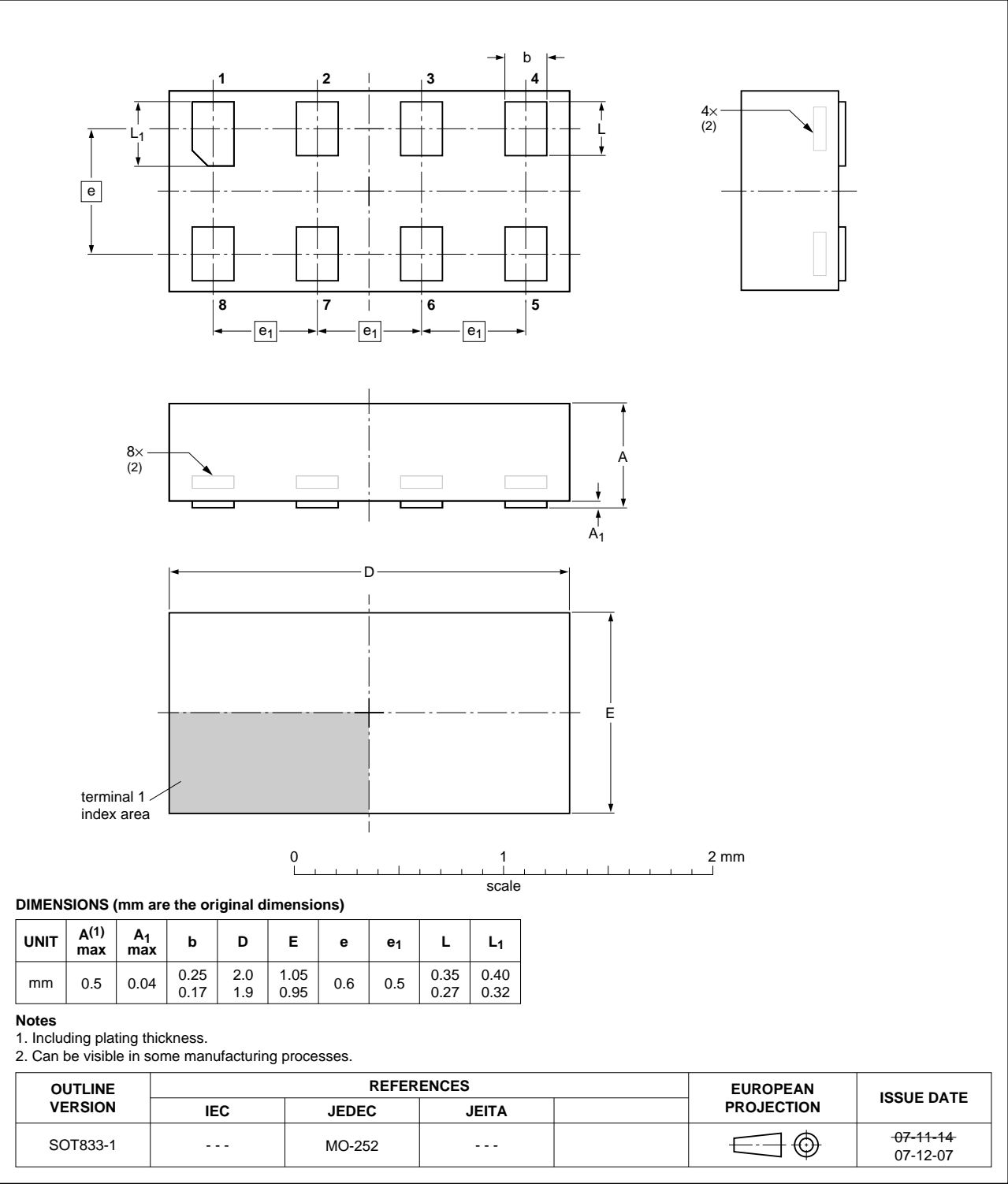


Fig 21. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

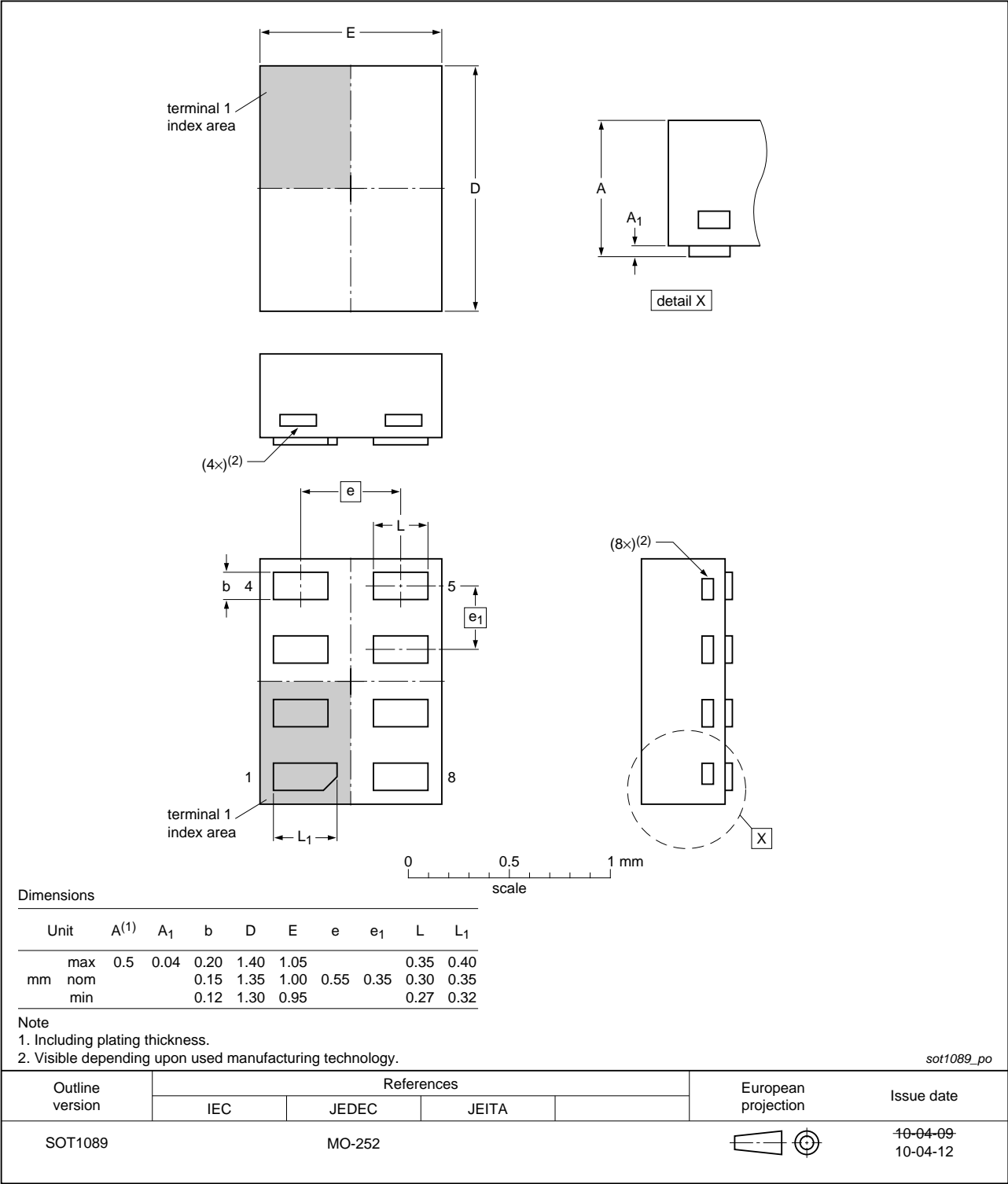


Fig 22. Package outline SOT1089 (XSON8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

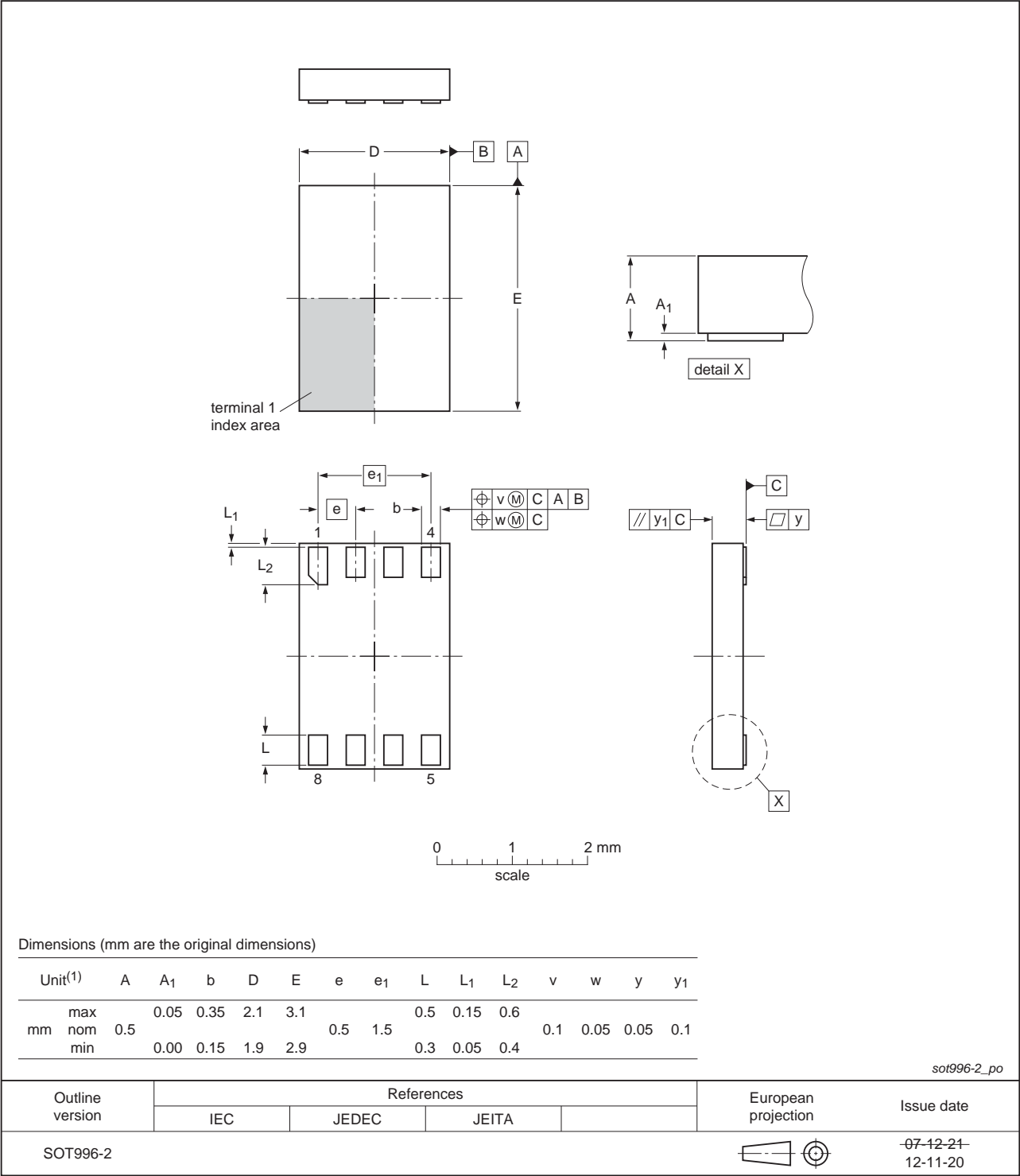


Fig 23. Package outline SOT996-2 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

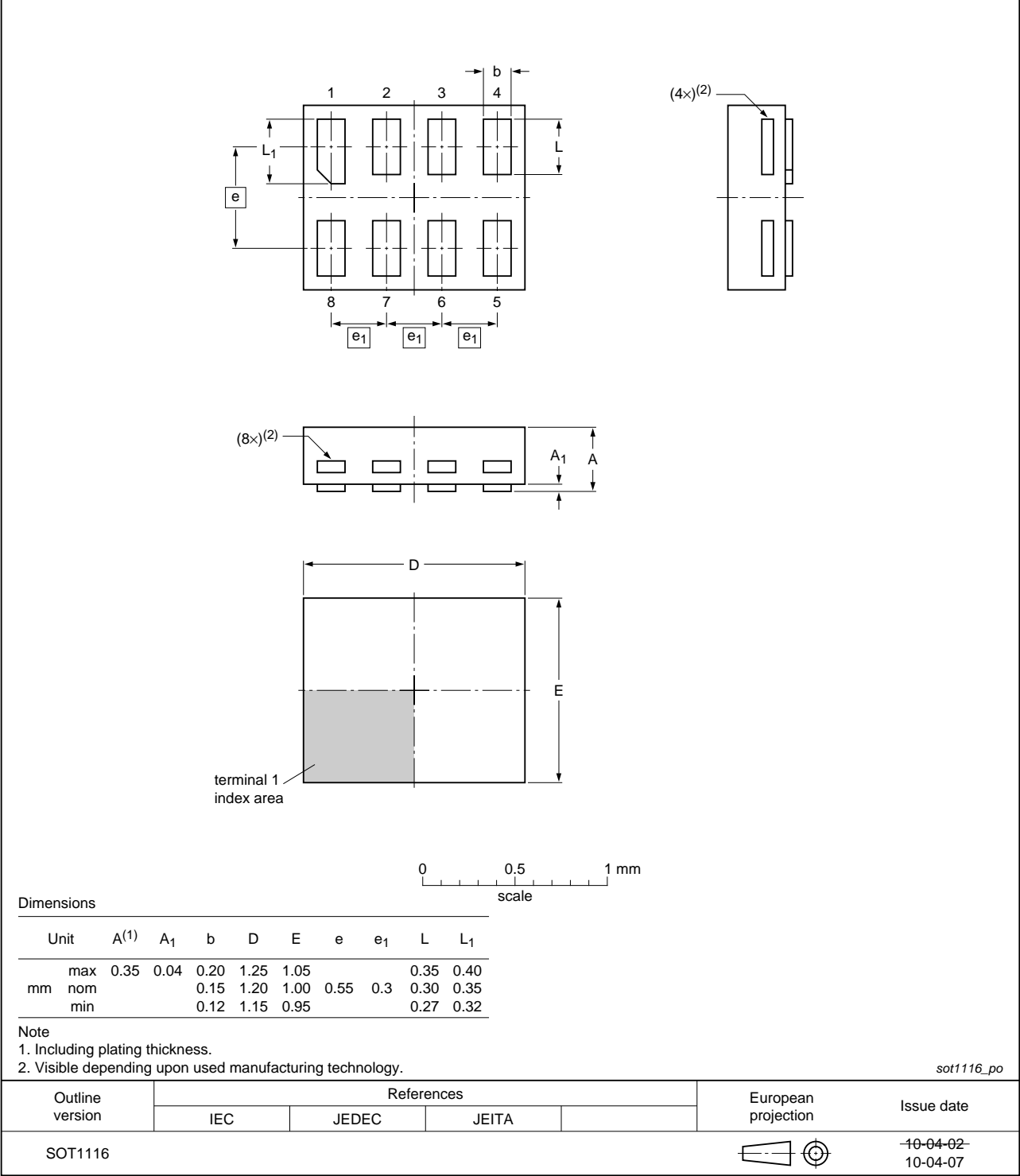


Fig 24. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

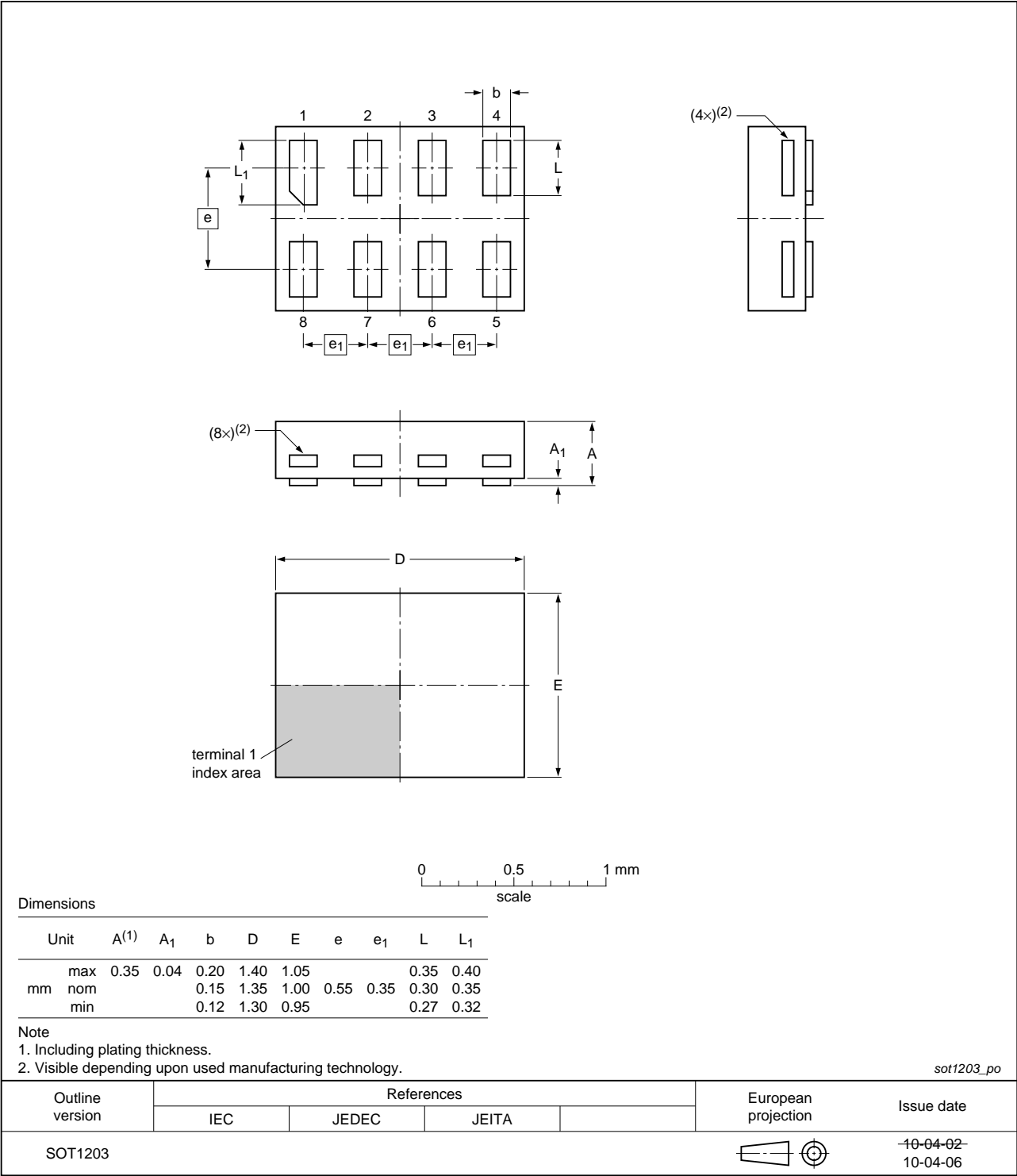


Fig 25. Package outline SOT1203 (XSON8)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G123 v.4	20131127	Product data sheet	-	74LVC1G123 v.3
Modifications:	• 74LVC1G123GM (XQFN8) removed.			
74LVC1G123 v.3	20130329	Product data sheet	-	74LVC1G123 v.2
Modifications:	• For type number 74LVC1G123GD XSON8U has changed to XSON8.			
74LVC1G123 v.2	20120801	Product data sheet	-	74LVC1G123 v.1
Modifications:	• V_{HYS} conditions and limits corrected (errata).			
74LVC1G123 v.1	20120123	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 27 November 2013

Document identifier: 74LVC1G123