# 74LVC1G97

## Low-power configurable multiple function gate

Rev. 3 — 7 December 2011 Product data sheet

## 1. General description

The 74LVC1G97 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to $V_{CC}$ or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power-down applications using $I_{OFF}$.
The $I_{OFF}$ circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive ($V_{CC}$ = 3.0 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC1G97GW | −40 °C to +125 °C | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |
| 74LVC1G97GV | −40 °C to +125 °C | SC-74 | plastic surface mounted package; 6 leads | SOT457 |
| 74LVC1G97GM | −40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886 |
| 74LVC1G97GF | −40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm | SOT891 |
| 74LVC1G97GN | −40 °C to +125 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm | SOT1115 |
| 74LVC1G97GS | −40 °C to +125 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm | SOT1202 |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code[1] |
|---|---|
| 74LVC1G97GW | YV |
| 74LVC1G97GV | Y97 |
| 74LVC1G97GM | YV |
| 74LVC1G97GF | YV |
| 74LVC1G97GN | YV |
| 74LVC1G97GS | YV |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

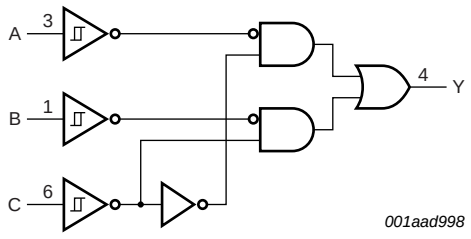



**Fig 1. Logic symbol**

# 6. Pinning information

## 6.1 Pinning

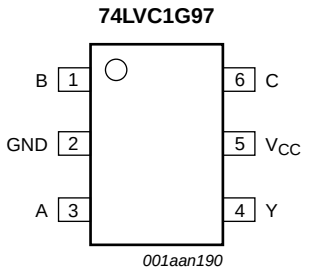



Fig 2. Pin configuration SOT363 and SOT457

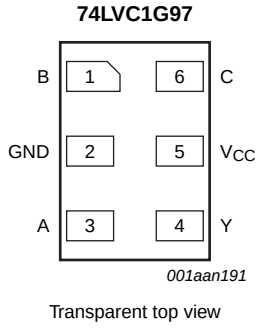



Fig 3. Pin configuration SOT886

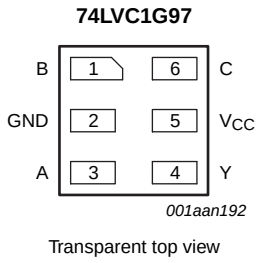



Fig 4. Pin configuration SOT891, SOT1115 and SOT1202

## 6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|---|---|---|
| B | 1 | data input |
| GND | 2 | ground (0 V) |
| A | 3 | data input |
| Y | 4 | data output |
| $V_{CC}$ | 5 | supply voltage |
| C | 6 | data input |

# 7. Functional description

Table 4. Function table[1]

| Input | | | Output |
|---|---|---|---|
| **C** | **B** | **A** | **Y** |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

[1] H = HIGH voltage level; L = LOW voltage level.

## 7.1 Logic configurations

**Table 5. Function selection table**

| Logic function | Figure |
|---|---|
| 2-input MUX | see Figure 5 |
| 2-input AND | see Figure 6 |
| 2-input OR with one input inverted | see Figure 7 |
| 2-input NAND with one input inverted | see Figure 7 |
| 2-input AND with one input inverted | see Figure 8 |
| 2-input NOR with one input inverted | see Figure 8 |
| 2-input OR | see Figure 9 |
| Inverter | see Figure 10 |
| Buffer | see Figure 11 |

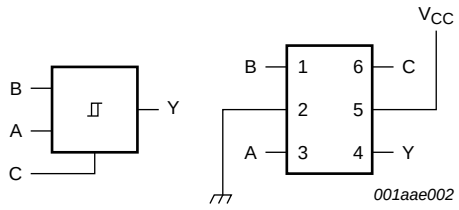



**Fig 5. 2-input MUX**

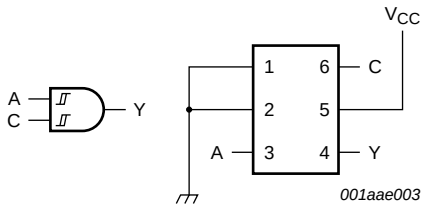



**Fig 6. 2-input AND gate**

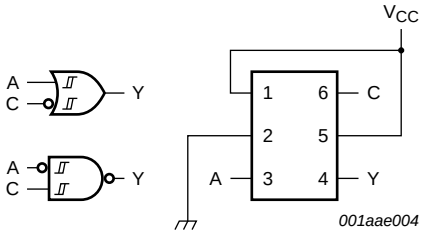



**Fig 7. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted**

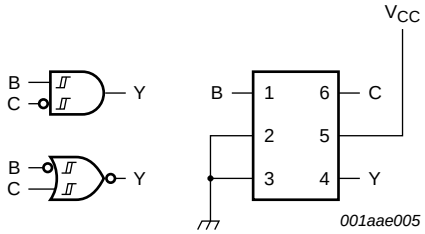



**Fig 8. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted**

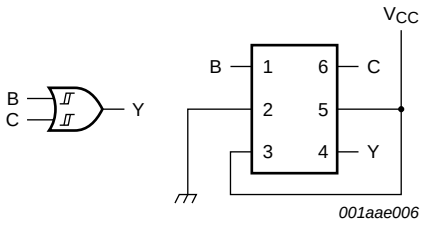



**Fig 9. 2-input OR gate**

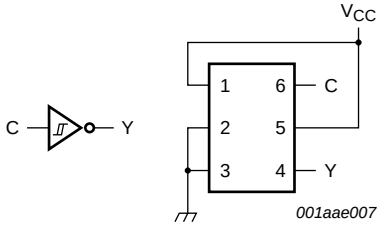



**Fig 10. Inverter**

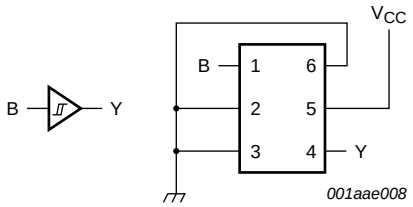



**Fig 11. Buffer**

## 8. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | −50 | - | mA |
| $V_I$ | input voltage | | [1] | −0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | Active mode | [1][2] | −0.5 | +6.5 | V |
| | | Power-down mode | [1][2] | −0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | +100 | mA |
| $I_{GND}$ | ground current | | | −100 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | [3] | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC}$ = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-88 and SC-74 packages: above 87.5 °C the value of $P_{tot}$ derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of $P_{tot}$ derates linearly with 7.8 mW/K.

## 9. Recommended operating conditions

**Table 7. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | Active mode | 0 | - | $V_{CC}$ | V |
| | | $V_{CC}$ = 0 V; Power-down mode | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | | −40 | - | +125 | °C |

## 10. Static characteristics

**Table 8. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{CC}$ or GND | | | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.65 V to 5.5 V | - | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.7 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.3 | - | 0.45 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| | | $I_O$ = 32 mA; $V_{CC}$ = 4.5 V | - | - | 0.55 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{CC}$ or GND | | | | | | |
| | | $I_O$ = −100 μA; $V_{CC}$ = 1.65 V to 5.5 V | $V_{CC}$ − 0.1 | - | - | $V_{CC}$ − 0.1 | - | V |
| | | $I_O$ = −4 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 0.95 | - | V |
| | | $I_O$ = −8 mA; $V_{CC}$ = 2.3 V | 1.9 | - | - | 1.7 | - | V |
| | | $I_O$ = −12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 1.9 | - | V |
| | | $I_O$ = −24 mA; $V_{CC}$ = 3.0 V | 2.3 | - | - | 2.0 | - | V |
| | | $I_O$ = −32 mA; $V_{CC}$ = 4.5 V | 3.8 | - | - | 3.4 | - | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | ±0.1 | ±5 | - | ±100 | μA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0 V | - | ±0.1 | ±10 | - | ±200 | μA |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $I_O$ = 0 A; $V_{CC}$ = 1.65 V to 5.5 V | - | 0.1 | 10 | - | 200 | μA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.3 V to 5.5 V | - | 5 | 500 | - | 5000 | μA |
| $C_I$ | input capacitance | | - | 2.5 | - | - | - | pF |

[1] Typical values are measured at maximum $V_{CC}$ and $T_{amb}$ = 25 °C.

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.*

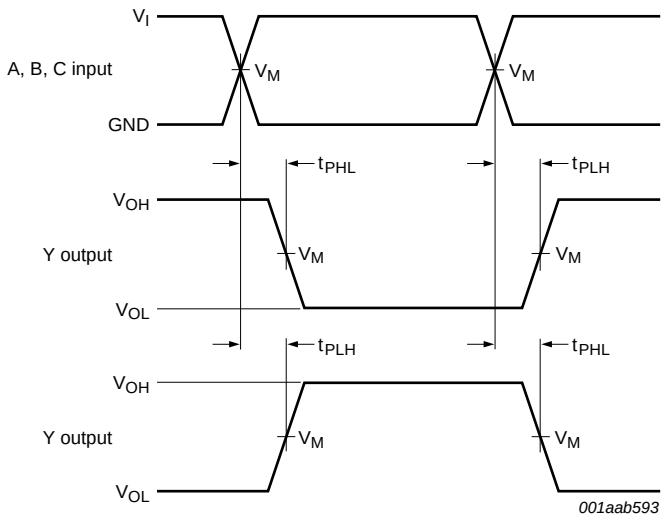
| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | A, B, C to Y; see Figure 12 | [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.0 | 6.0 | 14.4 | 1.0 | 18.0 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.5 | 3.5 | 8.3 | 0.5 | 10.4 | ns |
| | | $V_{CC}$ = 2.7 V | | 0.5 | 4.2 | 8.5 | 0.5 | 10.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 0.5 | 3.8 | 6.3 | 0.5 | 7.9 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.5 | 3.0 | 5.1 | 0.5 | 6.4 | ns |
| $C_{PD}$ | power dissipation capacitance | $V_{CC}$ = 3.3 V; $V_I$ = GND to $V_{CC}$ | [3] | - | 22 | - | - | - | pF |

[1] Typical values are measured at nominal $V_{CC}$ and at $T_{amb}$ = 25 °C.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## 12. Waveforms



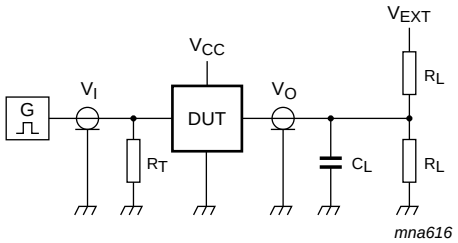

Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 12. Input A, B and C to output Y propagation delay times**

**Table 10. Measurement points**

| Supply voltage | Input | | Output |
|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_I$ | $V_M$ |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $V_{CC}$ | $0.5V_{CC}$ |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V | 1.5 V | 2.7 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 2.7 V | 1.5 V |
| 4.5 V to 5.5 V | $0.5V_{CC}$ | $V_{CC}$ | $0.5V_{CC}$ |




Measurement points are given in Table 11.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 13. Test circuit for measuring switching times**

**Table 11. Measurement points**

| Supply voltage | Input | | Load | | $V_{EXT}$ |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r = t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open |
| 2.3 to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open |

## 13. Transfer characteristics

**Table 12. Transfer characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{T+}$ | positive-going threshold voltage | see Figure 14, Figure 15, Figure 16 and Figure 17 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.70 | 1.02 | 1.20 | 0.67 | 1.20 | V |
| | | $V_{CC}$ = 2.3 V | 1.11 | 1.42 | 1.60 | 1.08 | 1.60 | V |
| | | $V_{CC}$ = 3.0 V | 1.50 | 1.79 | 2.00 | 1.47 | 2.00 | V |
| | | $V_{CC}$ = 4.5 V | 2.16 | 2.52 | 2.74 | 2.13 | 2.74 | V |
| | | $V_{CC}$ = 5.5 V | 2.61 | 2.99 | 3.33 | 2.58 | 3.33 | V |
| $V_{T-}$ | negative-going threshold voltage | see Figure 14, Figure 15, Figure 16 and Figure 17 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.30 | 0.53 | 0.72 | 0.30 | 0.75 | V |
| | | $V_{CC}$ = 2.3 V | 0.58 | 0.77 | 1.00 | 0.58 | 1.03 | V |
| | | $V_{CC}$ = 3.0 V | 0.80 | 1.04 | 1.30 | 0.80 | 1.33 | V |
| | | $V_{CC}$ = 4.5 V | 1.21 | 1.55 | 1.90 | 1.21 | 1.93 | V |
| | | $V_{CC}$ = 5.5 V | 1.45 | 1.86 | 2.29 | 1.45 | 2.32 | V |
| $V_H$ | hysteresis voltage | ($V_{T+} - V_{T-}$). See Figure 14, Figure 15, Figure 16 and Figure 17 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.30 | 0.48 | 0.62 | 0.23 | 0.62 | V |
| | | $V_{CC}$ = 2.3 V | 0.40 | 0.64 | 0.80 | 0.34 | 0.80 | V |
| | | $V_{CC}$ = 3.0 V | 0.50 | 0.75 | 1.00 | 0.44 | 1.00 | V |
| | | $V_{CC}$ = 4.5 V | 0.71 | 0.97 | 1.20 | 0.65 | 1.20 | V |
| | | $V_{CC}$ = 5.5 V | 0.71 | 1.13 | 1.40 | 0.65 | 1.40 | V |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

## 14. Waveforms transfer characteristics

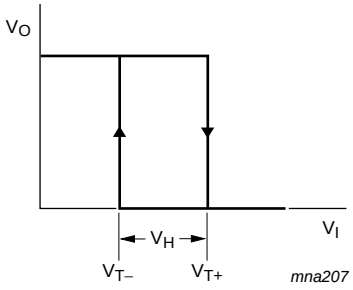
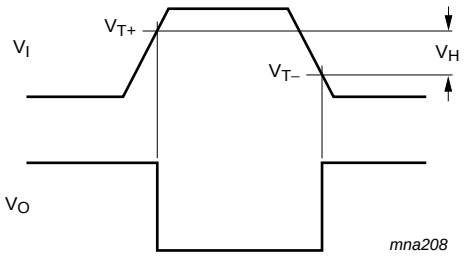



**Fig 14. Transfer characteristic**




$V_{T+}$ and $V_{T-}$ limits are at 70 % and 20 %.

**Fig 15. Definition of $V_{T+}$, $V_{T-}$ and $V_H$**

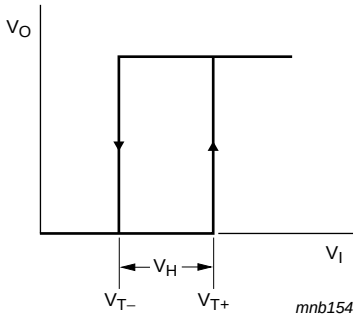
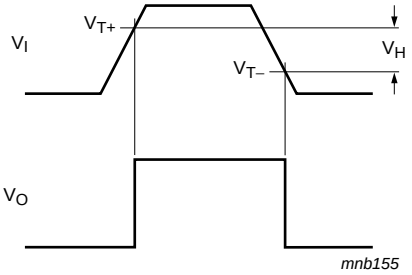



Fig 16. Transfer characteristic




$V_{T+}$ and $V_{T-}$ limits are at 70 % and 20 %.

Fig 17. Definition of $V_{T+}$, $V_{T-}$ and $V_H$

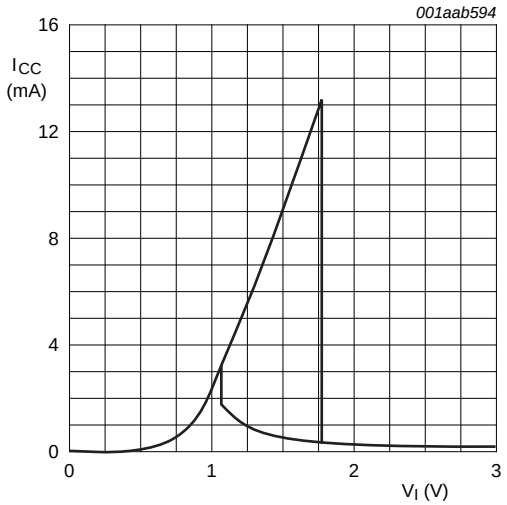
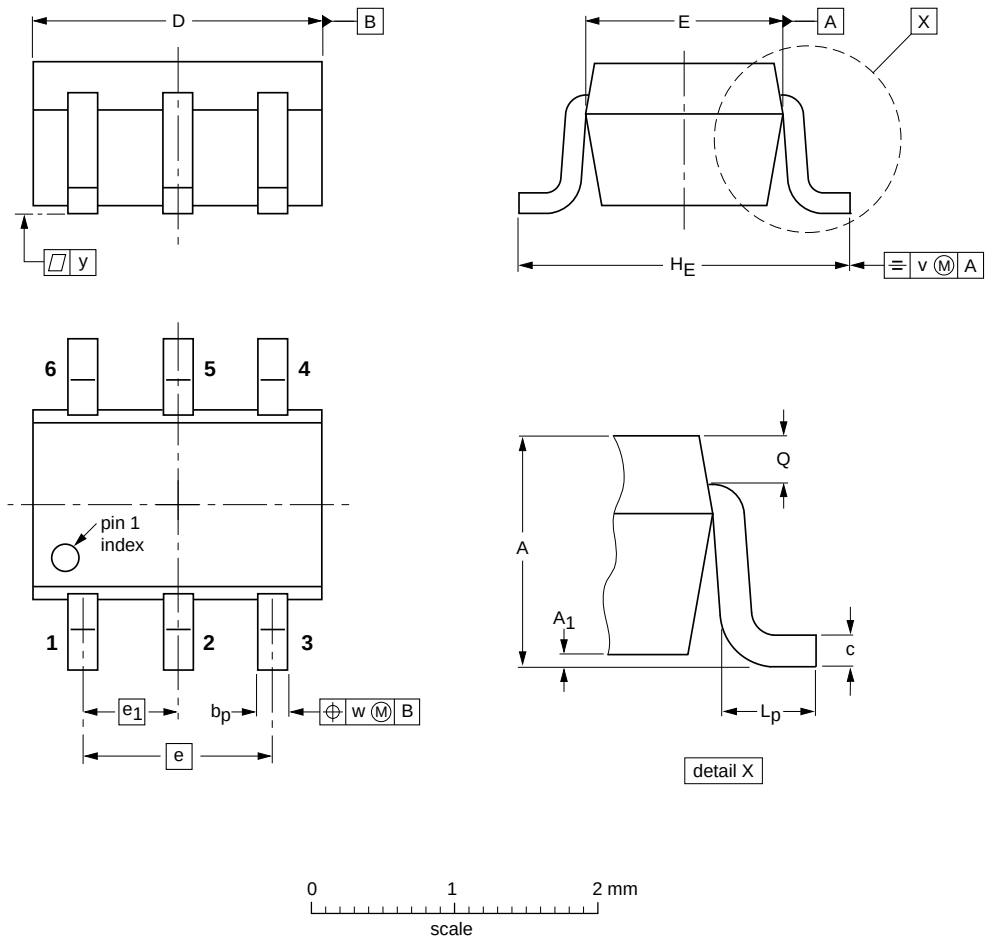



Fig 18. Typical 74LVC1G97 transfer characteristic; $V_{CC}$ = 3.0 V

## 15. Package outline

**Plastic surface-mounted package; 6 leads** **SOT363**



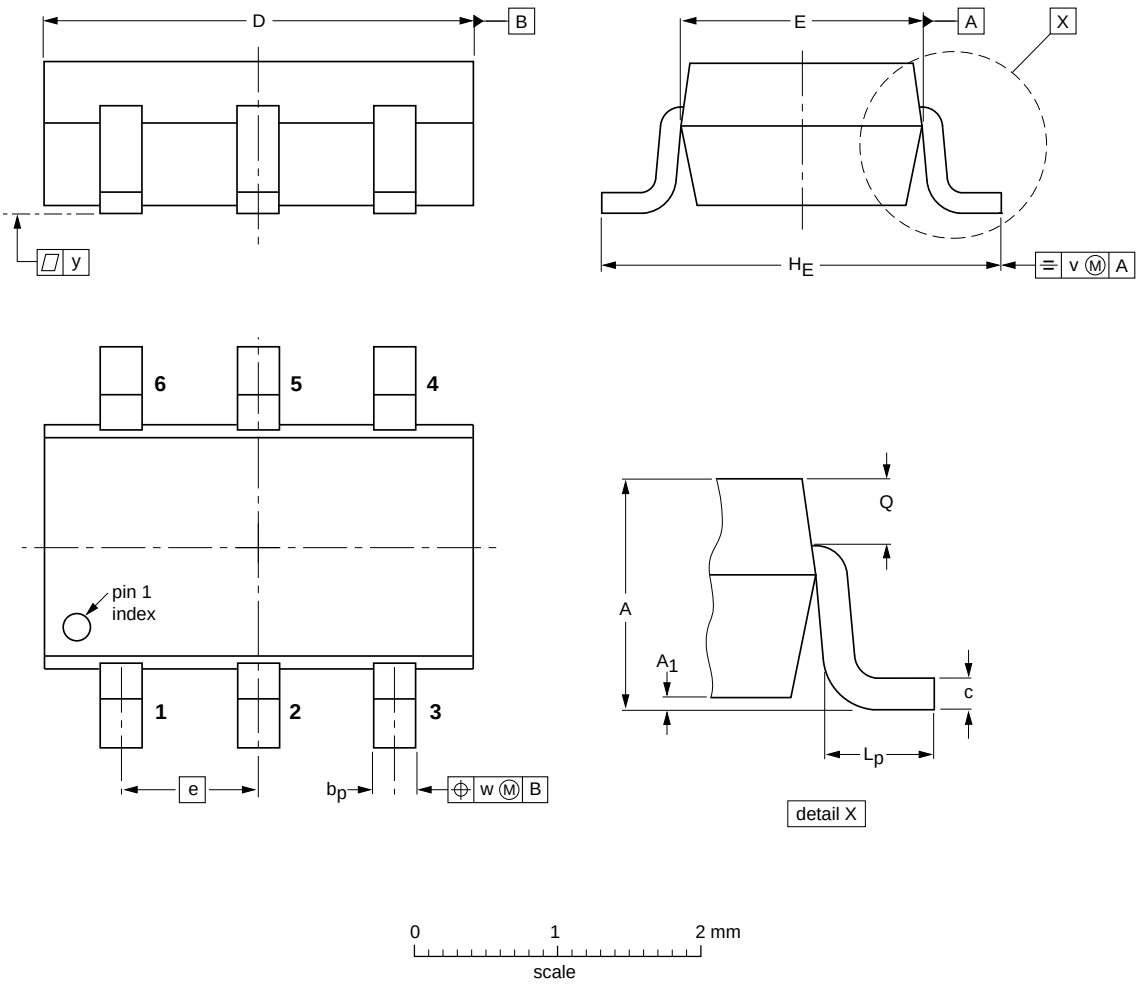

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.8 | 0.1 | 0.30<br>0.20 | 0.25<br>0.10 | 2.2<br>1.8 | 1.35<br>1.15 | 1.3 | 0.65 | 2.2<br>2.0 | 0.45<br>0.15 | 0.25<br>0.15 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT363 | | | SC-88 | | | ~~04-11-08~~<br>06-03-16 |

**Fig 19. Package outline SOT363 (SC-88)**

**Plastic surface-mounted package (TSOP6); 6 leads** **SOT457**



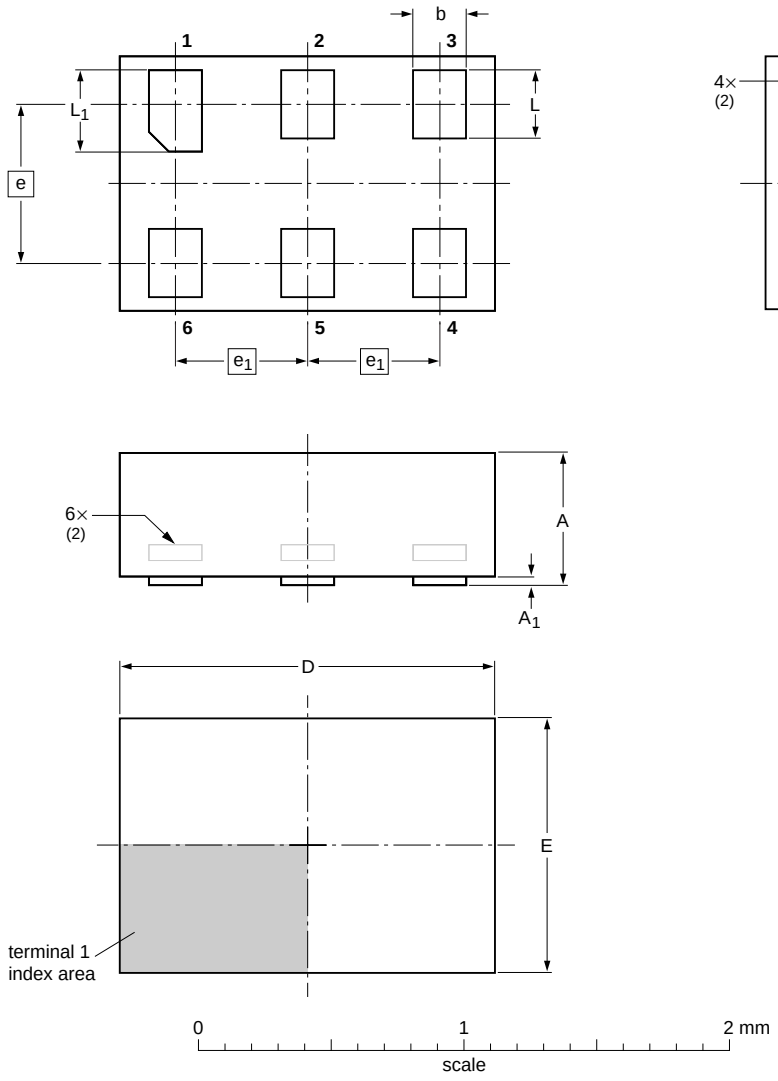

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT457 | | | SC-74 | | | ~~05-11-07~~<br>06-03-16 |

**Fig 20. Package outline SOT457 (SC-74)**

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm** **SOT886**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | A1 max | b | D | E | e | e1 | L | L1 |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 1.5<br>1.4 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

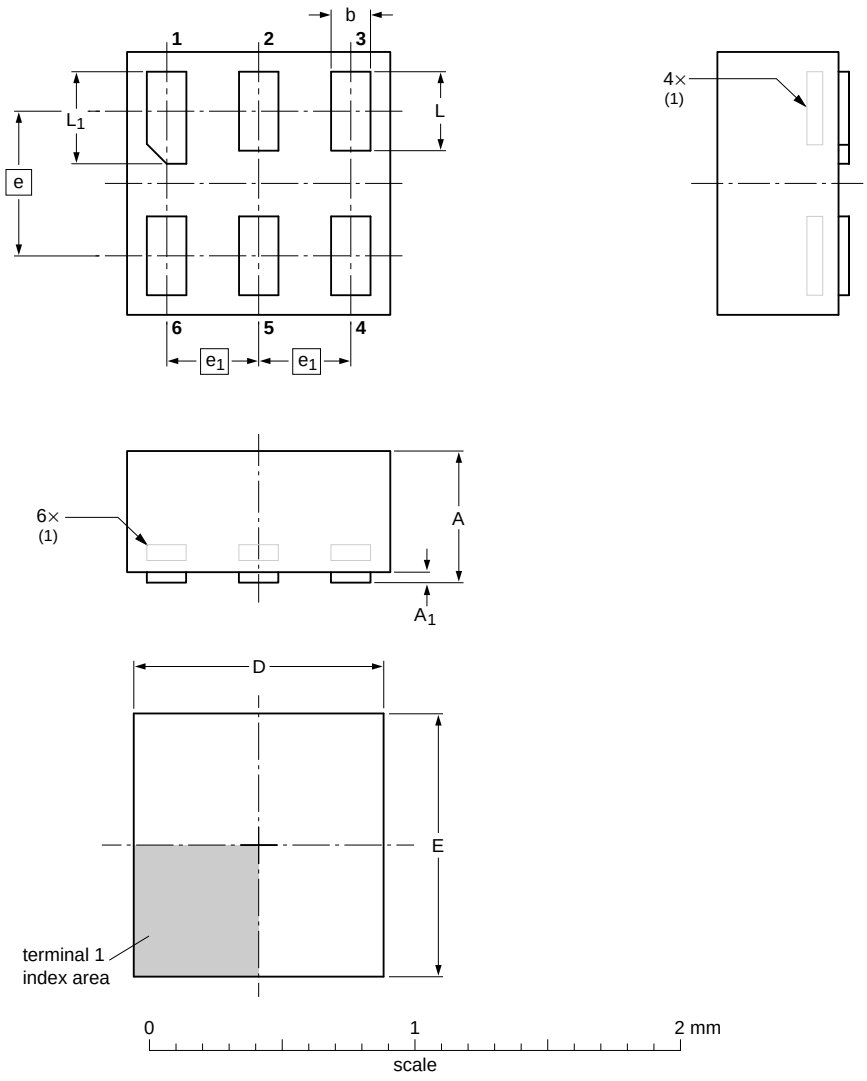
**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | | | ~~04-07-15~~<br>04-07-22 |

**Fig 21. Package outline SOT886 (XSON6)**

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm** **SOT891**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.20<br>0.12 | 1.05<br>0.95 | 1.05<br>0.95 | 0.55 | 0.35 | 0.35<br>0.27 | 0.40<br>0.32 |

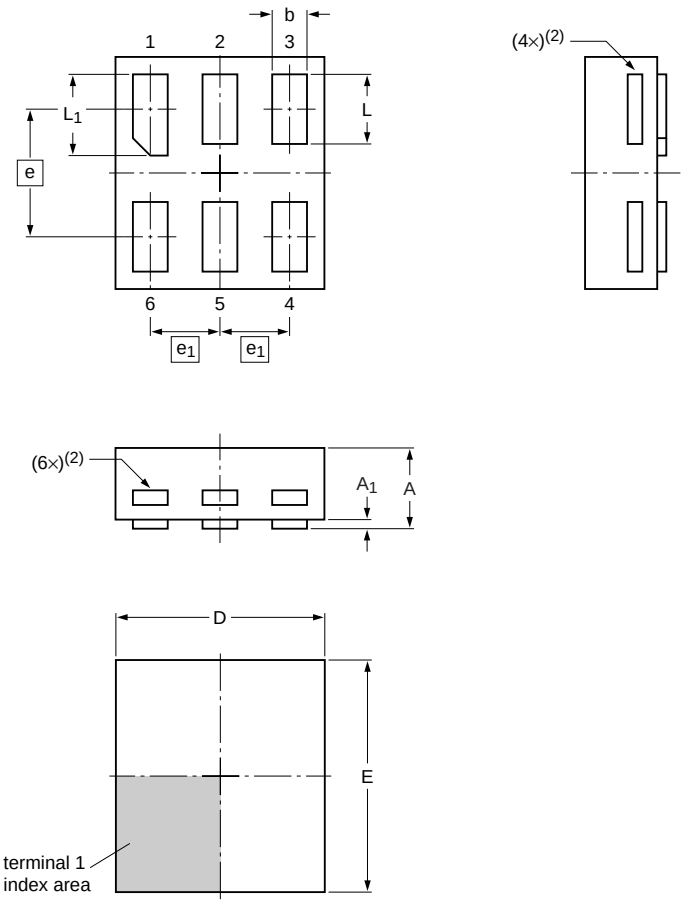
**Note**

1. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT891 | | | | | | ~~05-04-06~~<br>07-05-15 |

**Fig 22. Package outline SOT891 (XSON6)**

**XSON6: extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm** **SOT1115**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 0.95 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 0.90 | 1.00 | 0.55 | 0.3 | 0.30 | 0.35 |
| | min | | | 0.12 | 0.85 | 0.95 | | | 0.27 | 0.32 |

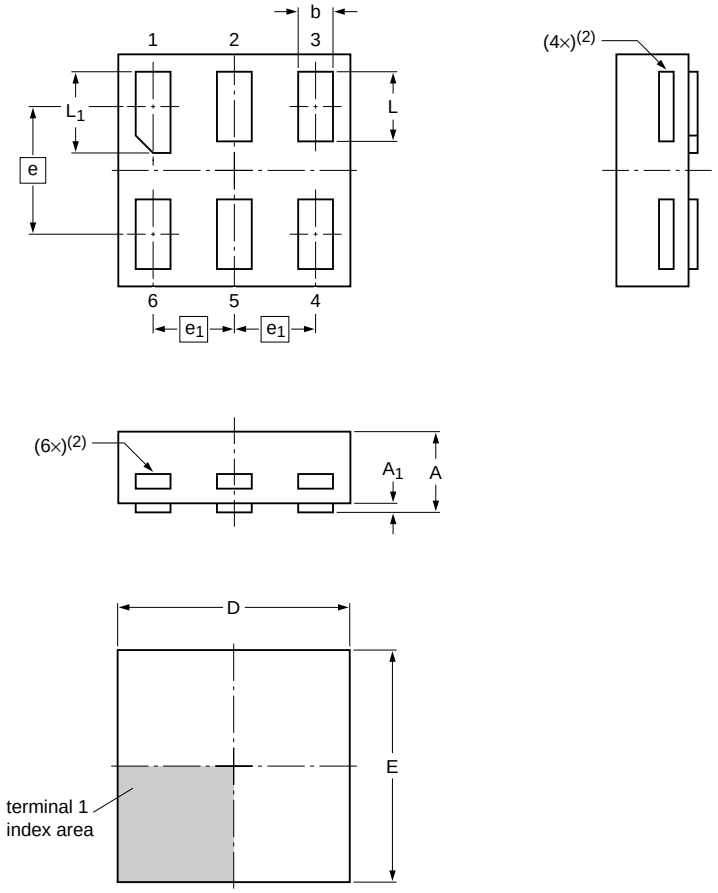
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1115_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1115 | | | | | | ~~10-04-02~~ 10-04-07 |

**Fig 23. Package outline SOT1115 (XSON6)**

**XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm** **SOT1202**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.05 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.00 | 1.00 | 0.55 | 0.35 | 0.30 | 0.35 |
| | min | | | 0.12 | 0.95 | 0.95 | | | 0.27 | 0.32 |

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1202_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1202 | | | | | | ~~10-04-02~~ 10-04-06 |

**Fig 24. Package outline SOT1202 (XSON6)**

## 16. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| TTL | Transistor-Transistor Logic |
| HBM | Human Body Model |
| ESD | ElectroStatic Discharge |
| MM | Machine Model |
| DUT | Device Under Test |

## 17. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC1G97 v.3 | 20111207 | Product data sheet | - | 74LVC1G97 v.2 |
| Modifications: | • Legal pages updated. | | | |
| 74LVC1G97 v.2 | 20110309 | Product data sheet | - | 74LVC1G97 v.1 |
| 74LVC1G97 v.1 | 20101221 | Product data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 18.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 18.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

### 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 20. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 7 December 2011**
**Document identifier: 74LVC1G97**