BLF8G38LS-75V

Power LDMOS transistor

Rev. 1 — 4 November 2013 Objective data sheet

1. Product profile

1.1 General description

75 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 3400 MHz to 3800 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	3400 to 3800	600	30	20	15.5	26	–30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

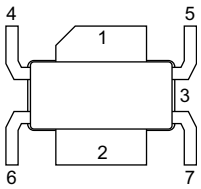
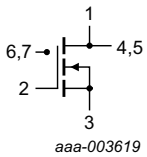
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth
- Designed for broadband operation (3400 MHz to 3800 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 3400 MHz to 3800 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G38LS-75V	-	earless flanged LDMOST ceramic package; 6 leads	SOT1239B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 20 W	0.48	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 153 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 600 mA	1.7	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	19.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 153 mA	-	0.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.35 A	-	0.1	-	Ω

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA, 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on the CCDF; f_1 = 3400 MHz; f_2 = 3500 MHz; f_3 = 3600 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 600 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 20 W	14.3	15.5	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 20 W	21	26	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 20 W	-	−10	−6	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 20 W	-	−30	−25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G38LS-75V is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 600 mA; P_L = 75 W; f = 3400 MHz.

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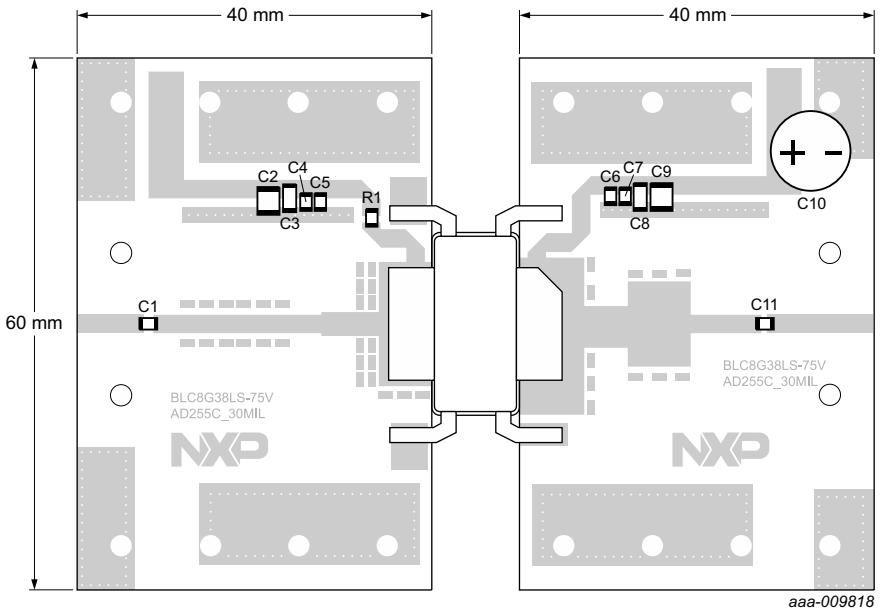
7.2 Test circuit



Printed-Circuit Board (PCB): Arlon AD255C; ε_r = 2.55; thickness = 0.762 mm.

See Table 8 for list of components.

Fig 1. Component layout for test circuit

Table 8. List of components

For test circuit, see Figure 1.

Component	Description	Value	Remarks
C1, C5, C6, C11	multilayer ceramic chip capacitor	20 pF	ATC600F
C2, C9	multilayer ceramic chip capacitor	10 μF	Murata
C3, C8	multilayer ceramic chip capacitor	0.1 μF	Murata
C4, C7	multilayer ceramic chip capacitor	0.01 μF	Murata
C10	electrolytic capacitor	1000 μF, 100 V	
R1	chip resistor	5.1 Ω	Vishay Dale SMD 0805

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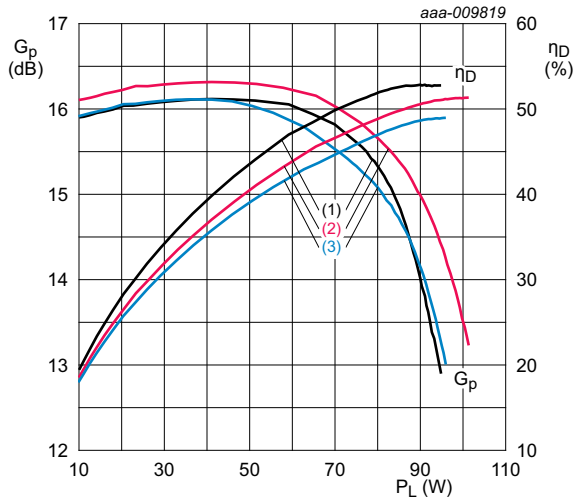
7.3 Graphical data

7.3.1 Pulsed CW



V_{DS} = 30 V; I_{Dq} = 600 mA.

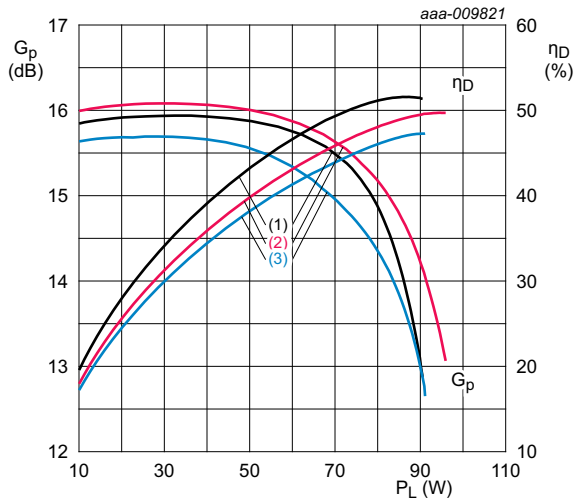
(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 2. Power gain and drain efficiency as function of output power; typical values

7.3.2 CW



V_{DS} = 30 V; I_{Dq} = 600 mA.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

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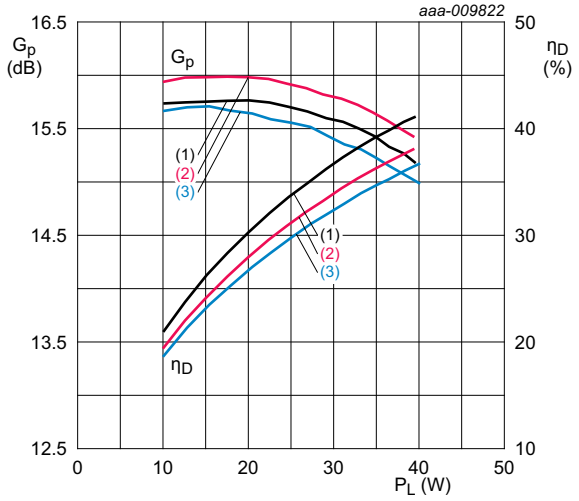
7.3.3 1-Carrier W-CDMA



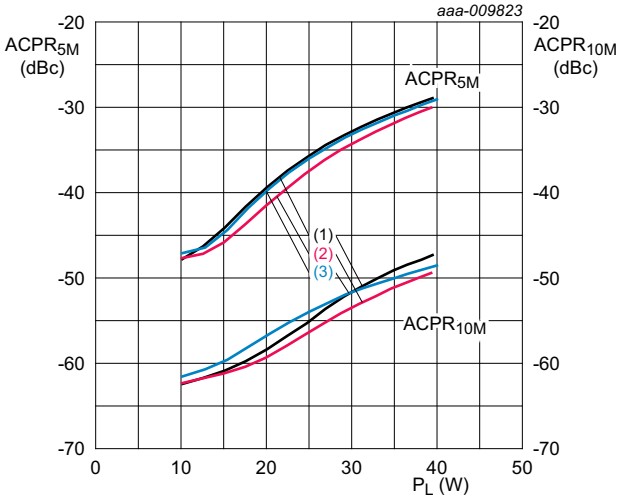
V_{DS} = 30 V; I_{Dq} = 600 mA.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 600 mA.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 5. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values

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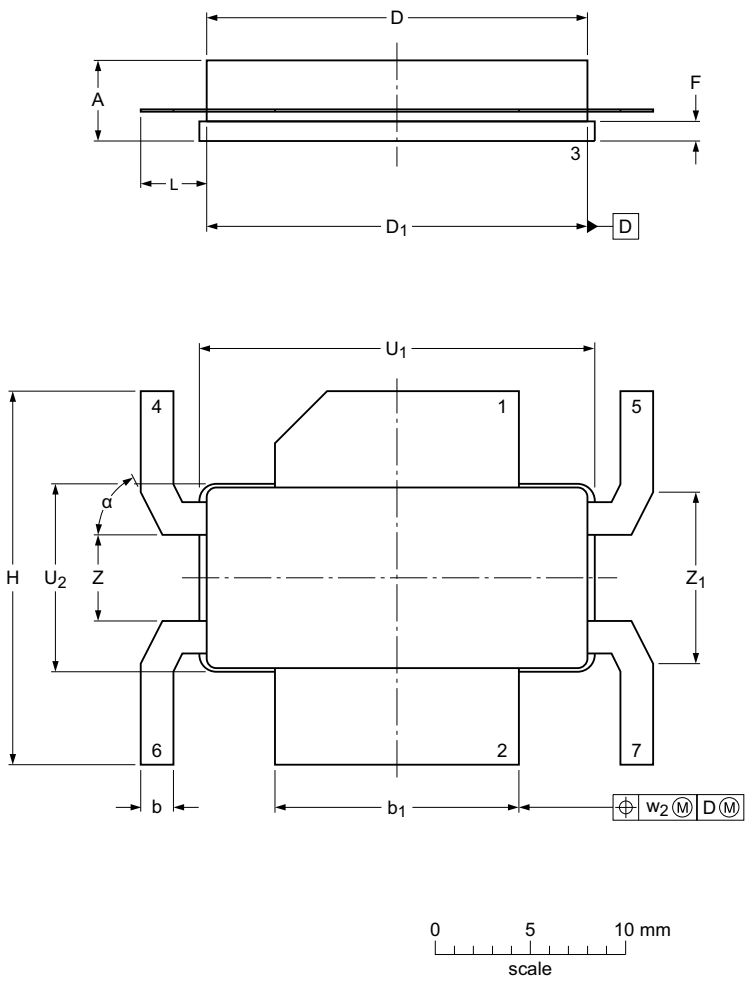
8. Package outline

Earless flanged LDMOST ceramic package; 6 leads **SOT1239B**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2	Z	Z_1	α
mm	max	4.75	1.83	12.83	0.20	20.02	19.96	9.53	9.53	1.14	19.94	3.56	1.70	20.70	9.91		4.60	9.53	64°
	nom															0.51			
	min	3.45	1.57	12.57	0.12	19.61	19.66	9.27	9.25	0.89	18.92	3.30	1.45	20.45	9.65		4.32	8.71	60°
inches	max	0.187	0.072	0.505	0.008	0.788	0.786	0.375	0.375	0.045	0.785	0.140	0.067	0.815	0.390		0.181	0.375	64°
	nom															0.02			
	min	0.136	0.062	0.495	0.005	0.772	0.774	0.365	0.364	0.035	0.745	0.130	0.057	0.805	0.380		0.170	0.343	60°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1239b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1239B						~~13-07-09~~ 13-10-28

Fig 6. Package outline SOT1239B

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9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G38LS-75V v.1	20131104	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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