BLM7G1822S-40PB; BLM7G1822S-40PBG

LDMOS 2-stage power MMIC

Rev. 1 — 9 October 2013 Objective data sheet

1. Product profile

1.1 General description

The BLM7G1822S-40PB(G) is a dual path, 2-stage power MMIC using NXP's state of the art GEN7 LDMOS technology. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 1805 MHz to 2170 MHz. Available in gull wing or straight lead outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq1} = <tbd>; I_{Dq2} = <tbd>.
Test signal: 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; per section unless otherwise specified in a class-AB production circuit.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	2140	28	1.1	31.5	12	<tbd>

1.2 Features and benefits

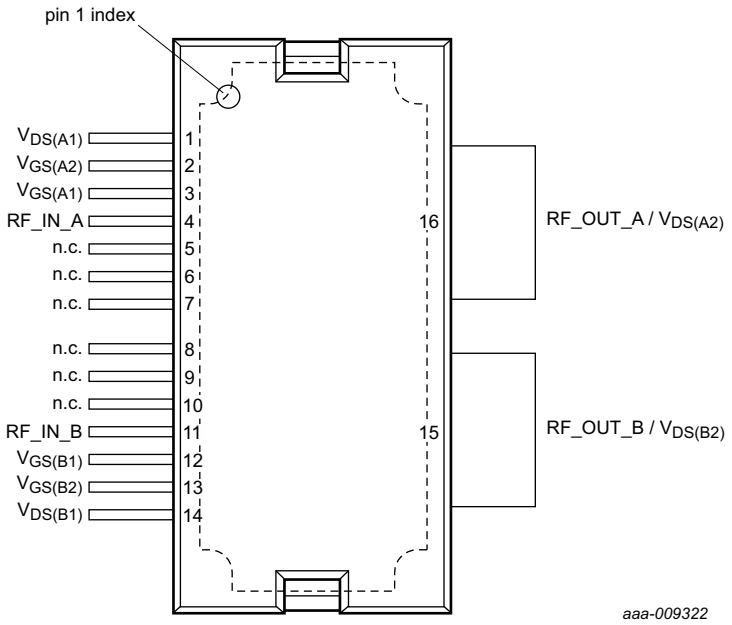
- Designed for broadband operation (frequency 1805 MHz to 2170 MHz)
- High path-to-path isolation enabling multiple combinations
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power MMIC for W-CDMA base stations in the 1805 MHz to 2170 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
  - Dual path or single ended
  - Doherty
  - Quadrature combined
  - Push-pull

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of stage A1
$V_{GS(A2)}$	2	gate-source voltage of stage A2
$V_{GS(A1)}$	3	gate-source voltage of stage A1
RF_IN_A	4	RF input path A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input path of B
$V_{GS(B1)}$	12	gate-source voltage of stage B1
$V_{GS(B2)}$	13	gate-source voltage of stage B2
$V_{DS(B1)}$	14	drain-source voltage of stage B1

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_B/$V_{DS(B2)}$	15	RF output path B / drain-source voltage of stage B2
RF_OUT_A/$V_{DS(A2)}$	16	RF output path A / drain-source voltage of stage A2
GND [1]	flange	RF ground

[1] Flange = RF_GROUND.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G1822S-40PB	HSOP16F	plastic, heatsink small outline package; 16 leads (flat)	SOT1211-1
BLM7G1822S-40PBG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-1

4. Block diagram

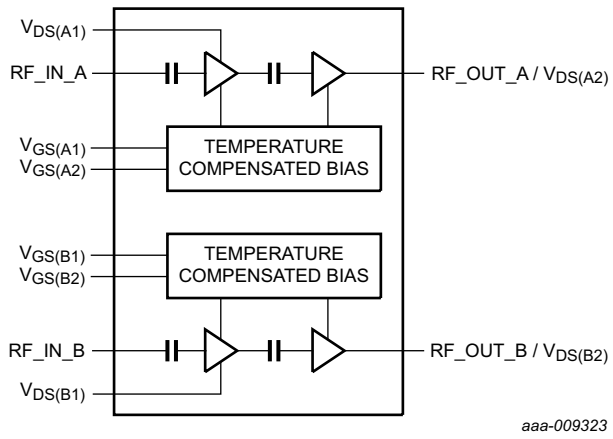


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; T_{case} = 90 °C; P_L = <tbd>	[1]	<tbd>	K/W
		driver stage; T_{case} = 90 °C; P_L = <tbd>	[1]	<tbd>	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Final stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = <tbd>	<tbd>	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = <tbd>	<tbd>	<tbd>	<tbd>	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = <tbd>	<tbd>	<tbd>	<tbd>	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	<tbd>	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	<tbd>	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	<tbd>	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = <tbd>	-	<tbd>	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = <tbd>	-	<tbd>	-	mΩ
I_{Dq}	quiescent drain current	V_{DS} = 28 V	<tbd>	<tbd>	<tbd>	mA
Driver stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = <tbd>	<tbd>	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = <tbd>	<tbd>	<tbd>	<tbd>	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = <tbd>	<tbd>	<tbd>	<tbd>	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	<tbd>	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	<tbd>	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	<tbd>	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = <tbd>	-	<tbd>	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = <tbd>	-	<tbd>	-	mΩ
I_{Dq}	quiescent drain current	V_{DS} = 28 V	<tbd>	<tbd>	<tbd>	mA

Table 7. RF Characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = <tbd>; I_{Dq2} = <tbd>. Test signal: 2-carrier W-CDMA; 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; f = 2140 MHz; per section unless otherwise specified, measured in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 1.1 W	<tbd>	31.5	<tbd>	dB
η_D	drain efficiency	$P_{L(AV)}$ = 1.1 W	<tbd>	12	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 1.1 W	-	−15	<tbd>	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 1.1 W	-	<tbd>	<tbd>	dBc

8. Application information

8.1 Possible circuit topologies

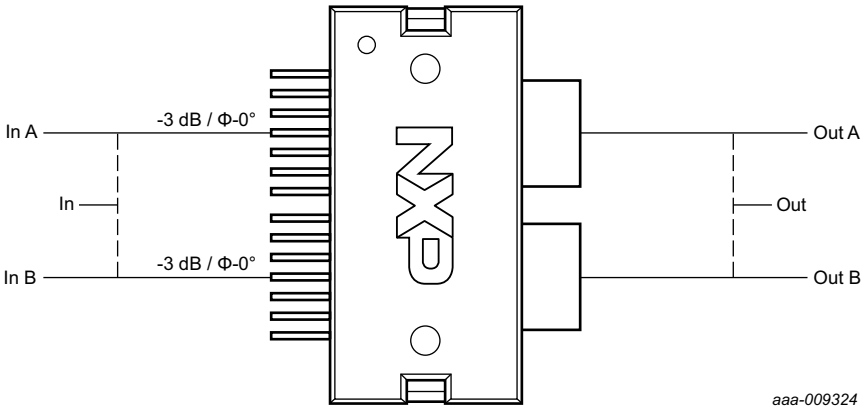


Fig 3. Dual path or single ended

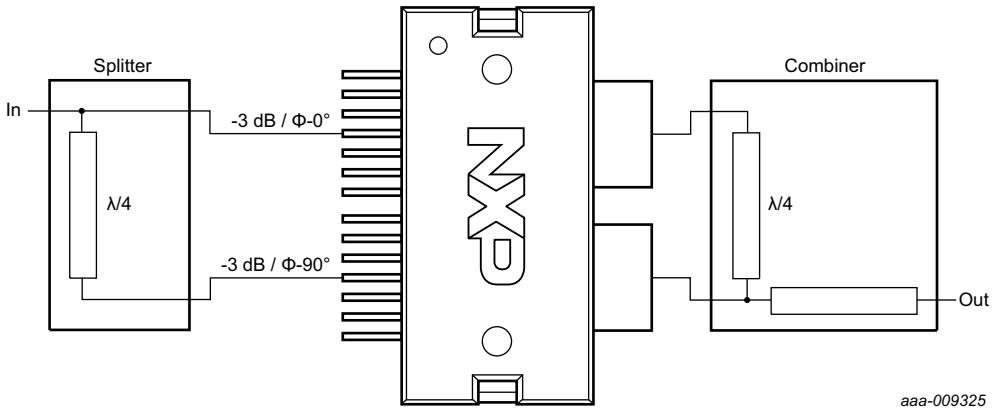


Fig 4. Doherty

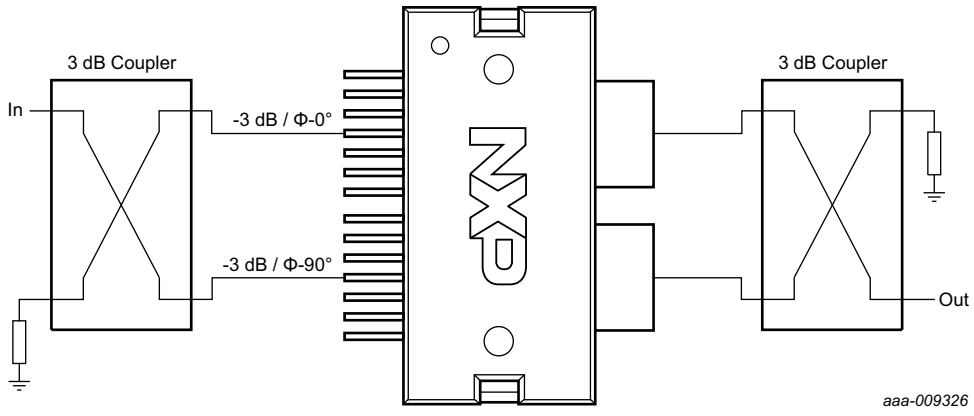


Fig 5. Quadrature combined

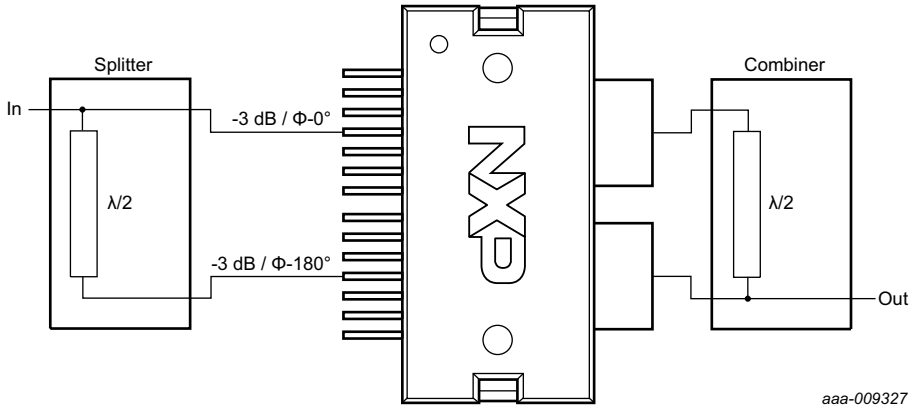
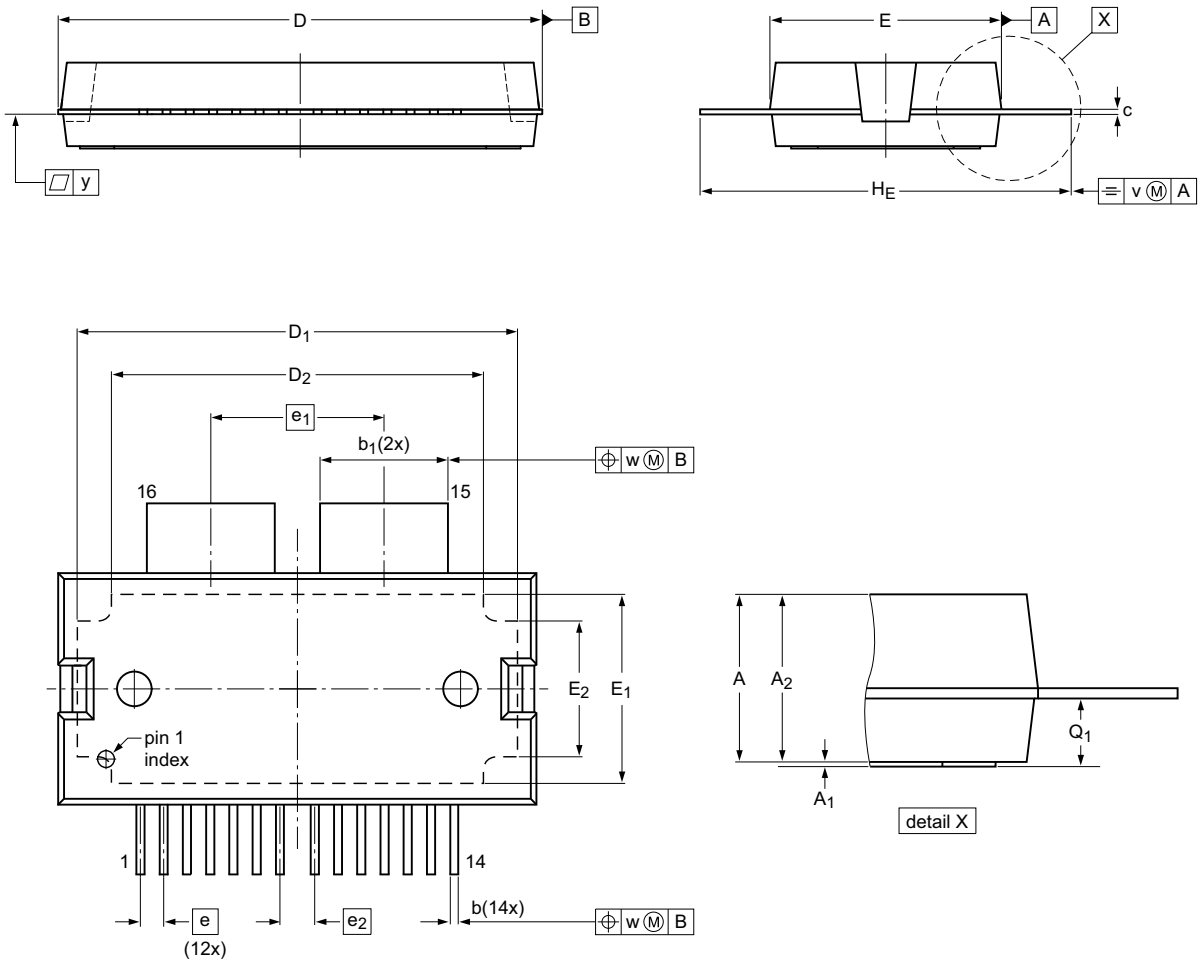


Fig 6. Push-pull

9. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat) **SOT1211-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	b_1	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	e_1	e_2	H_E	Q_1	v	w	y
mm	max	3.9	0.2	3.65	0.40	5.55	0.27	20.62	19.00	16.05	10.01	8.18	5.89				16.16	1.62			
	nom		0.1	3.60	0.35	5.50	0.22	20.57	18.95	16.00	9.96	8.13	5.84	1.0	7.45	1.5	15.96	1.57	0.25	0.25	0.1
	min		0	3.55	0.30	5.45	0.17	20.52	18.90	15.95	9.91	8.08	5.79				15.76	1.52			

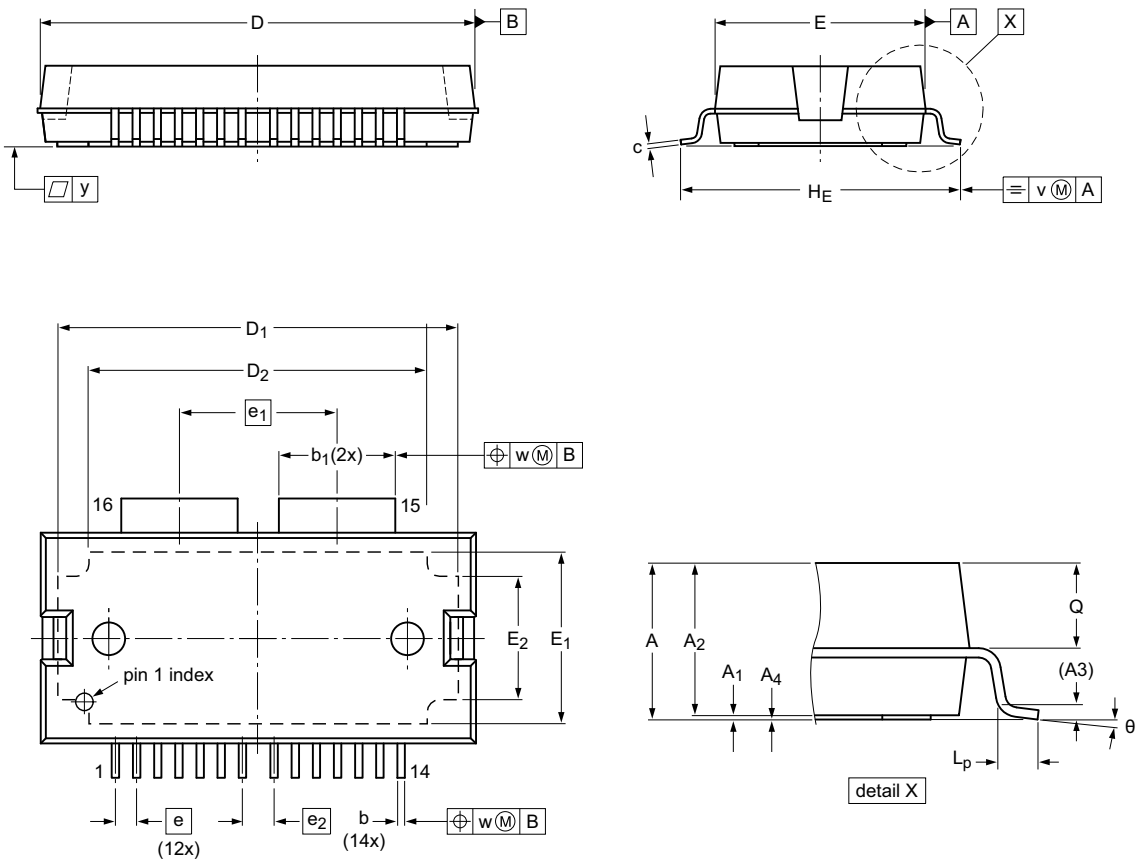
Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1211-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1211-1						~~12-03-06~~ 13-06-24

Fig 7. Package outline SOT1211-1 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads **SOT1212-1**



w	y	θ
0.25	0.1	7° / 3° / 0°

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	A_4	b	b_1	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	e_1	e_2	H_E	L_p	Q	v
mm	max	3.9	0.2	3.65		0.06	0.40	5.55	0.27	20.62	19.00	16.05	10.01	8.18	5.89				13.5	1.10	2.07	
	nom		0.1	3.60	0.35	0	0.35	5.50	0.22	20.57	18.95	16.00	9.96	8.13	5.84	1.0	7.45	1.5	13.2	0.95	2.02	0.25
	min		0	3.55		-0.02	0.30	5.45	0.17	20.52	18.90	15.95	9.91	8.08	5.79				12.9	0.80	1.97	

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1212-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1212-1						~~12-05-14~~ 12-05-21

Fig 8. Package outline SOT1212-1 (HSOP16)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 8. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN7	Seventh Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G1822S-40PB_S-40PBG v.1	20131009	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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