

BLM7G22S-60PB; BLM7G22S-60PBG

LDMOS 2-stage power MMIC

Rev. 1 — 11 December 2012

Product data sheet

1. Product profile

1.1 General description

The BLM7G22S-60PB(G) is a dual path, 2-stage power MMIC using NXP's state of the art GEN7 LDMOS technology. This device is perfectly suited as general purpose driver in the frequency range from 2100 MHz to 2200 MHz. Available in gull wing or flat lead outline.

Table 1. Application performance

Typical RF performance at $T_{case} = 25\text{ °C}$; $I_{Dq1} = 75\text{ mA}$; $I_{Dq2} = 233\text{ mA}$.

Test signal: 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; per section unless otherwise specified in a class-AB production circuit.

Test signal	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR (dBc)
2-carrier W-CDMA	2140	28	1.6	31.5	11.3	-43

1.2 Features and benefits

- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated current sense
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use (input matched to 50 Ω; output partially matched)
- Designed for broadband operation (frequency 2100 MHz to 2200 MHz)
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

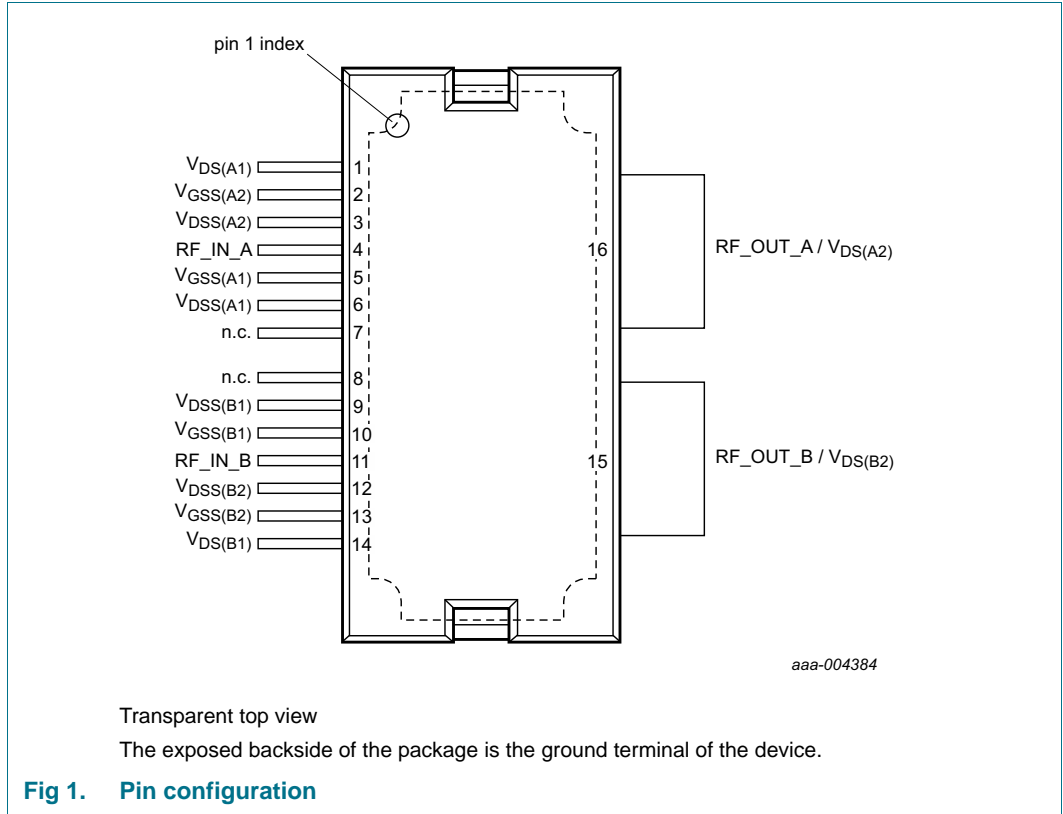
1.3 Applications

RF power MMIC for W-CDMA base stations in the 2100 MHz to 2200 MHz frequency range.



2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of stage A1
$V_{GSS(A2)}$	2	gate sense FET and gate source voltage of stage A2
$V_{DSS(A2)}$	3	drain sense FET source voltage of stage A2
RF_IN_A	4	RF input path A
$V_{GSS(A1)}$	5	gate sense FET and gate source voltage of stage A1
$V_{DSS(A1)}$	6	drain sense FET source voltage of stage A1
n.c.	7	not connected
n.c.	8	not connected
$V_{DSS(B1)}$	9	drain sense FET source voltage of stage B1
$V_{GSS(B1)}$	10	gate sense FET and gate source voltage of stage B1
RF_IN_B	11	RF input path of B
$V_{DSS(B2)}$	12	drain sense FET source voltage of stage B2
$V_{GSS(B2)}$	13	gate sense FET and gate source voltage of stage B2
$V_{DS(B1)}$	14	drain-source voltage of stage B1

Table 2. Pin description ...continued

Symbol	Pin	Description
RF_OUT_A/ $V_{DS(A2)}$	15	RF output path A / drain source voltage of stage A2
RF_OUT_B/ $V_{DS(B2)}$	16	RF output path B / drain source voltage of stage B2
GND [1]	flange	RF ground

[1] Flange = RF_GROUND.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G22S-60PB	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-1
BLM7G22S-60PBG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-1

4. Block diagram

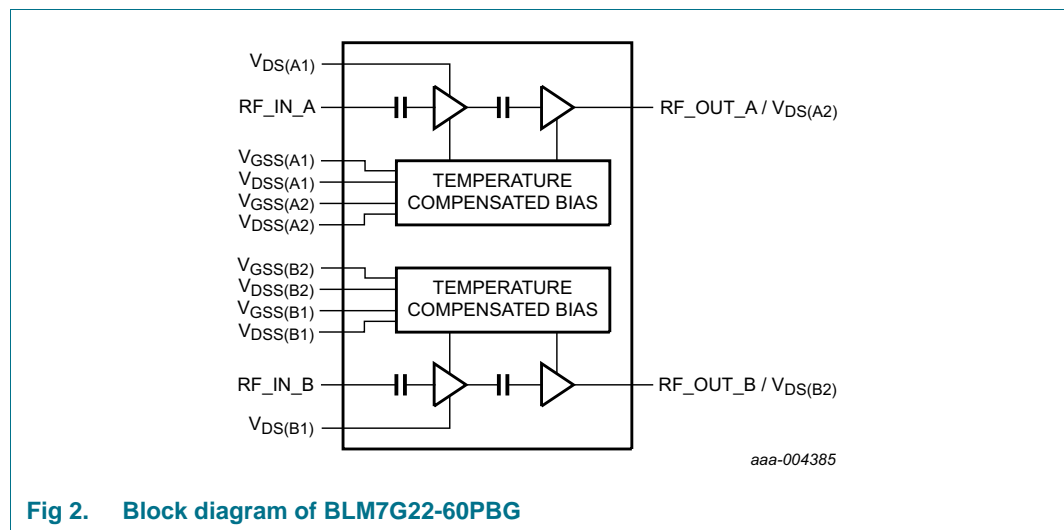


Fig 2. Block diagram of BLM7G22-60PBG

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
$V_{GS(sense)}$	sense gate-source voltage		-0.5	+9	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; $T_{case} = 90\text{ °C}$; $P_L = 3.2\text{ W}$	[1] 1.1	K/W
		driver stage; $T_{case} = 90\text{ °C}$; $P_L = 3.2\text{ W}$	[1] 3.2	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

$T_{case} = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Final stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.422\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 42\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 253\text{ mA}$	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	7.8	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 1478\text{ mA}$	-	2.85	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 1.48\text{ A}$	-	350	-	$\text{m}\Omega$
I_{Dq}	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$; $V_{DS} = 28\text{ V}$	208	233	257	mA
Driver stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.116\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 11.6\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 69.6\text{ mA}$	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	2.2	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 406\text{ mA}$	-	0.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 0.4\text{ A}$	-	2350	-	$\text{m}\Omega$
I_{Dq}	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$; $V_{DS} = 28\text{ V}$	67	75	83	mA

Table 7. RF Characteristics

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{Dq1} = 75\text{ mA}$; $I_{Dq2} = 233\text{ mA}$. Test signal: 2-carrier W-CDMA; 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; $f = 2140\text{ MHz}$; per section unless otherwise specified, measured in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 1.6\text{ W}$	29.5	31.5	33.5	dB
η_D	drain efficiency	$P_{L(AV)} = 1.6\text{ W}$	10	11.3	-	%
RL_{in}	input return loss	$P_{L(AV)} = 1.6\text{ W}$	-	-17	-10	dB
ACPR	adjacent channel power ratio	$P_{L(AV)} = 1.6\text{ W}$	-	-43	-40	dBc

8. Application information

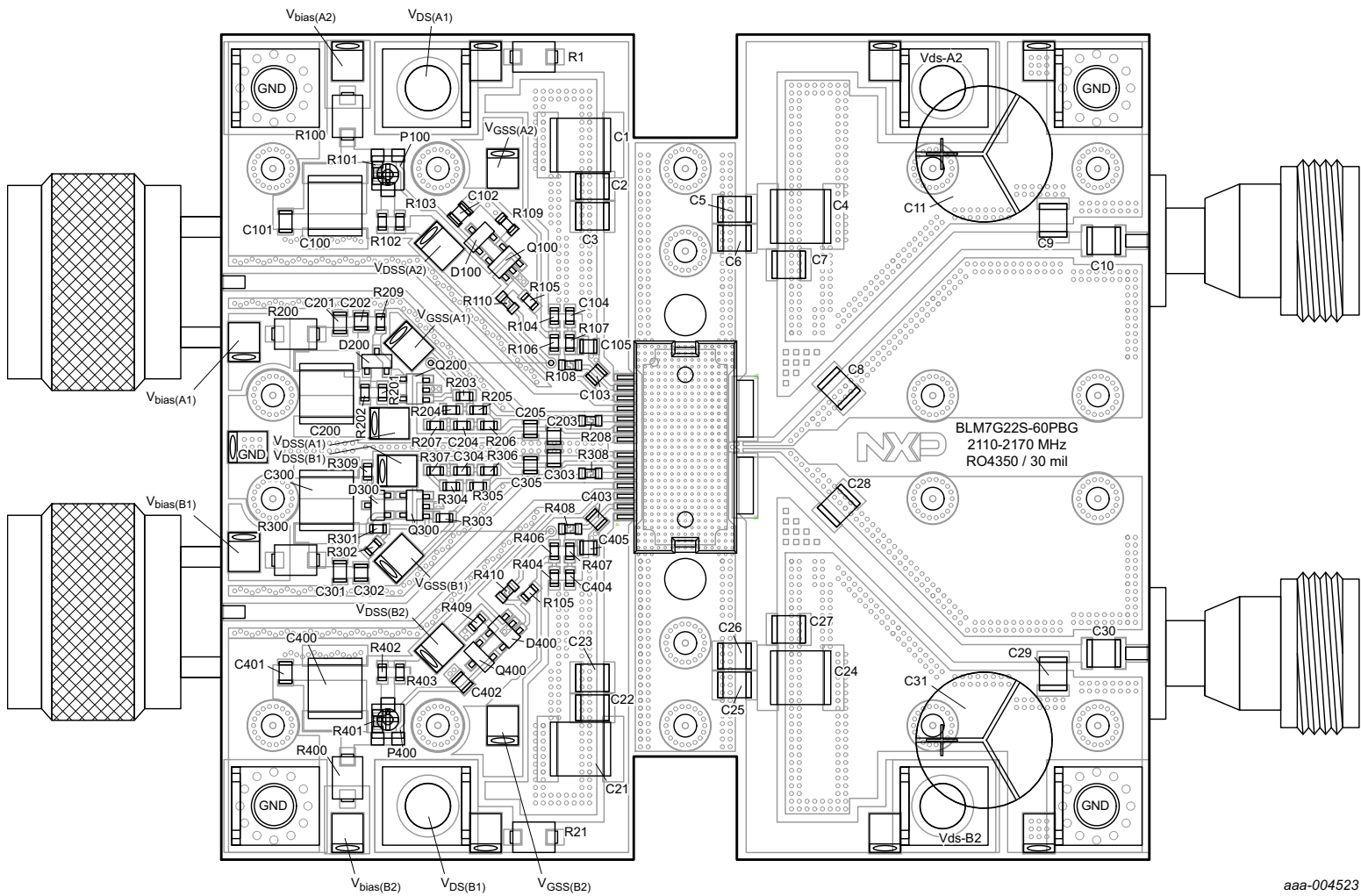
Table 8. List of components

For test circuit see [Figure 3](#).

Component	Description	Value	Remarks
C1, C4, C21, C24, C100, C200, C300, C400	capacitor	10 μF	
C2, C5, C6, C22, C25, C26	capacitor	1 μF	
C3, C7, C10, C23, C27, C30	capacitor	8.2 pF	[1]
C8, C28	capacitor	1.6 pF	[1]
C9, C29	capacitor	0.4 pF	[1]
C11, C31	electrolytic capacitor	470 μF	
C101, C201, C301, C401	capacitor	100 nF	
C102, C103, C105, C202, C203, C205, C302, C303, C305, C402, C403, C405	capacitor	12 pF	[2]
C104, C204, C304, C404	capacitor	4.7 μF	
D100, D200, D300, D400	IC: LM4051	-	
P100, P400	potentiometer	-	do not populate
Q100, Q200, Q300, Q400	IC	-	LM7341
R1, R21	ferrite bead	-	
R100, R200, R300, R400	resistor	4.7 Ω	
R101, R108, R208, R308, R401, R408	resistor	0 Ω	
R102, R402	resistor	360 Ω	1% tolerance
R103, R403	resistor	330 Ω	1% tolerance
R104, R203, R303, R404	resistor	68 k Ω	
R105, R405	resistor	10 k Ω	
R106, R205, R305, R406	resistor	820 Ω	
R107, R206, R306, R407	resistor	47 Ω	
R109, R209, R309, R409	resistor	300 k Ω	
R201, R301	resistor	180 Ω	1% tolerance
R202, R302	resistor	3.6 k Ω	1% tolerance
R204, R304	resistor	9.1 k Ω	
R207, R307	resistor	1 k Ω	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.



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Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.762 mm.

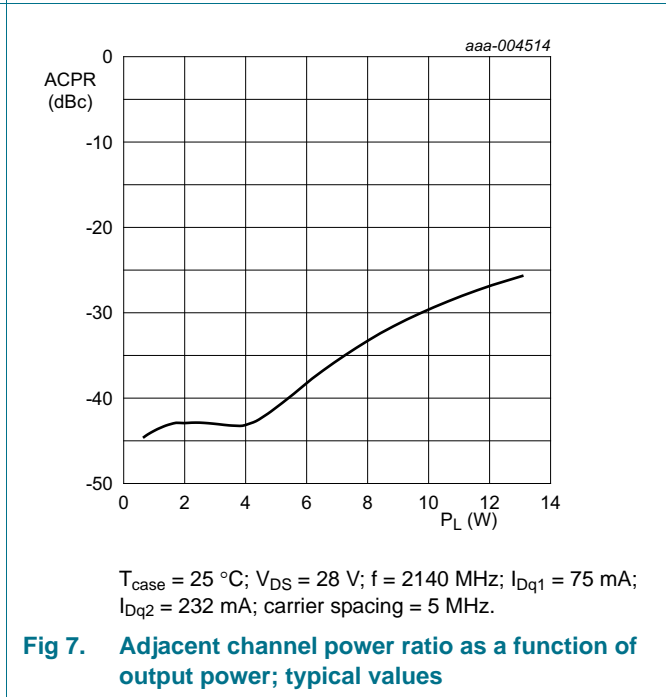
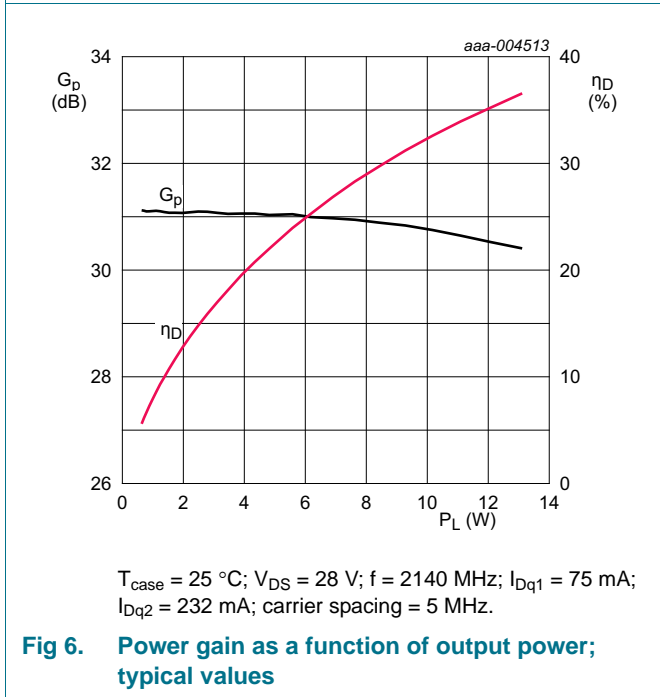
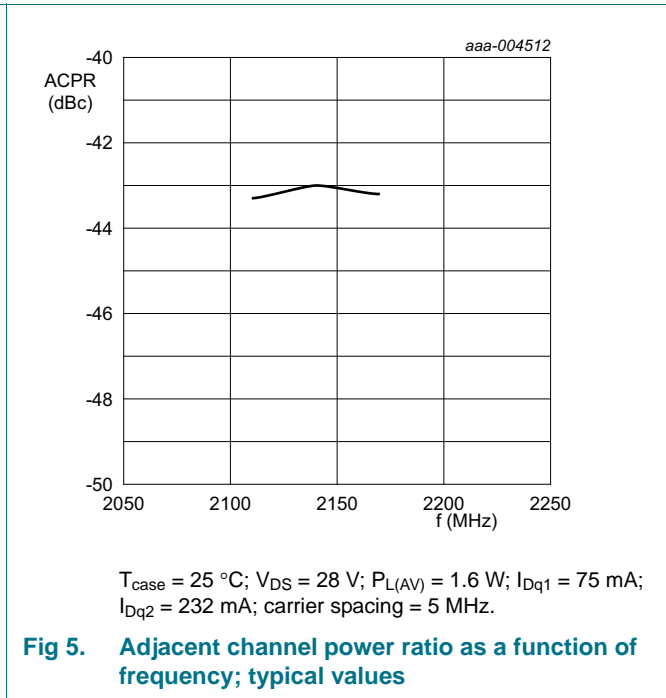
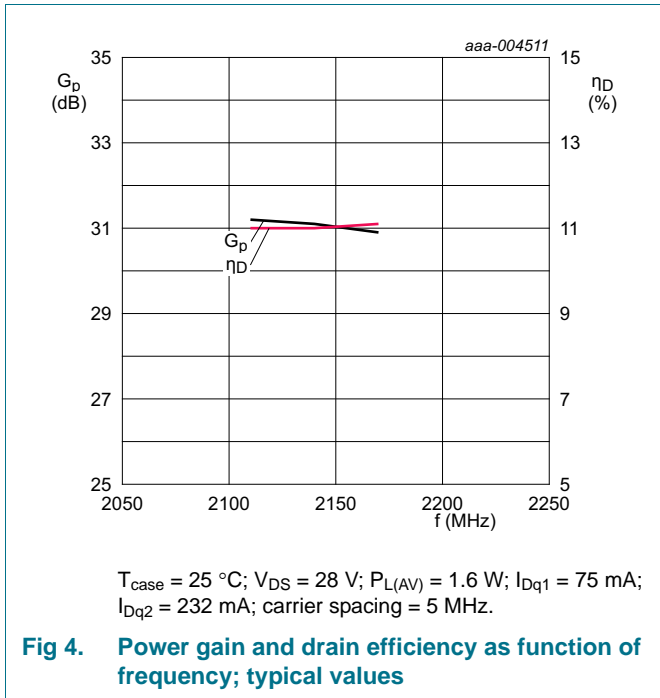
See [Table 8](#) for a list of components.

Fig 3. Component layout for class-AB application circuit with auto-bias

8.1 Performance curves

Performance curves are measured per section in a class-AB BLM7G22S-60PBG application circuit with auto-bias.

8.1.1 W-CDMA



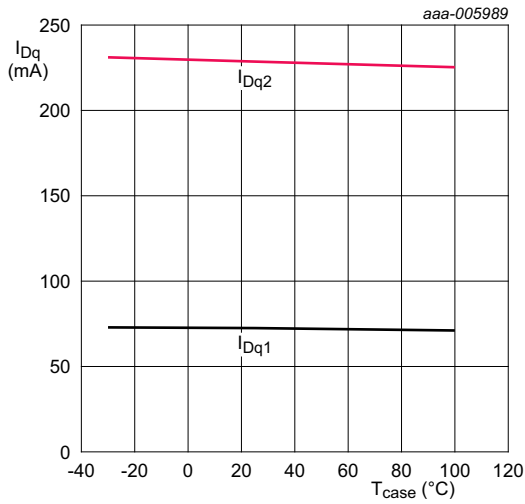
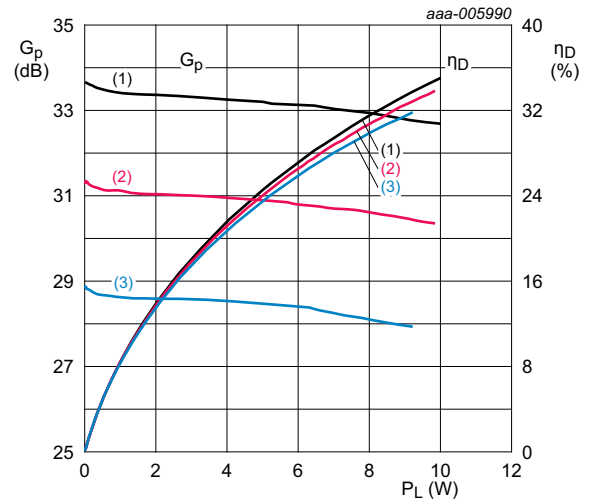


Fig 8. Quiescent drain current as a function of case temperature; typical values

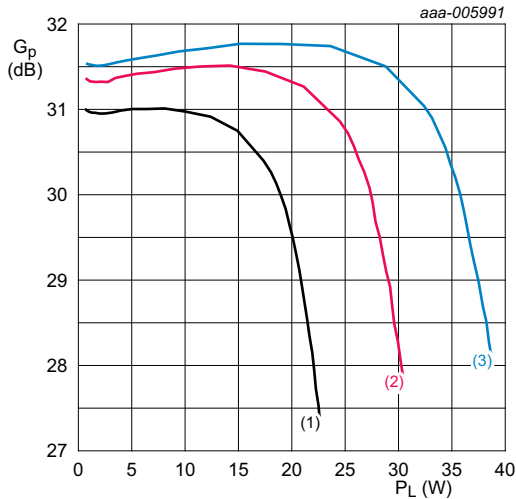


V_{DS} = 28 V; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

- (1) T_{case} = -30 °C
- (2) T_{case} = +25 °C
- (3) T_{case} = +100 °C

Fig 9. Power gain and drain efficiency as function of output power; typical values

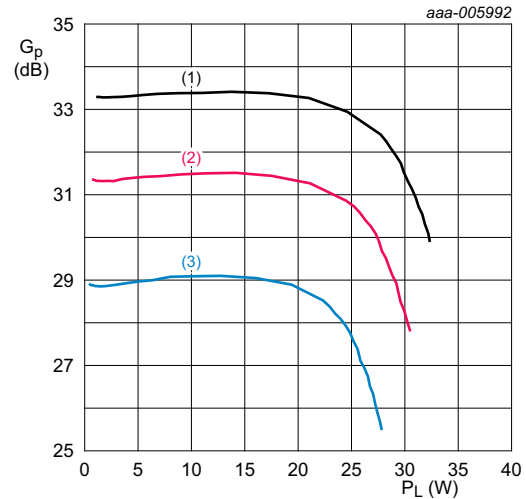
8.1.2 1-Tone pulsed CW



T_{case} = 25 °C; V_{DS} = 28 V; P_{L(AV)} = 1.6 W; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; δ = 10 %; t_p = 100 μs.

- (1) V_{DD} = 24 V
- (2) V_{DD} = 28 V
- (3) V_{DD} = 32 V

Fig 10. Power gain as a function of output power; typical values

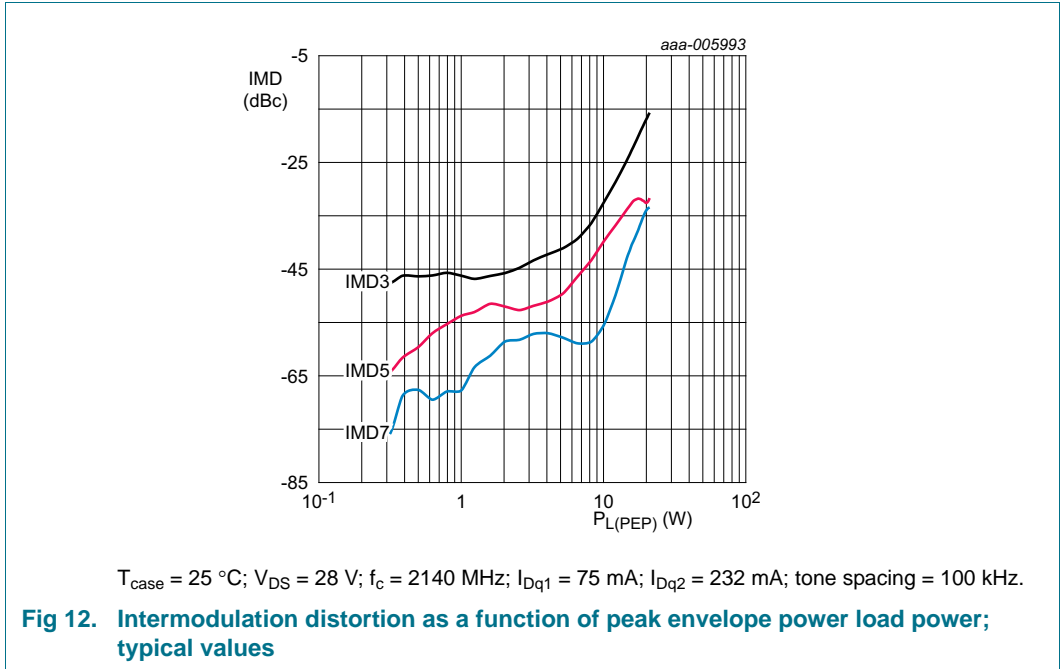


V_{DS} = 28 V; P_{L(AV)} = 1.6 W; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; δ = 10 %; t_p = 100 μs.

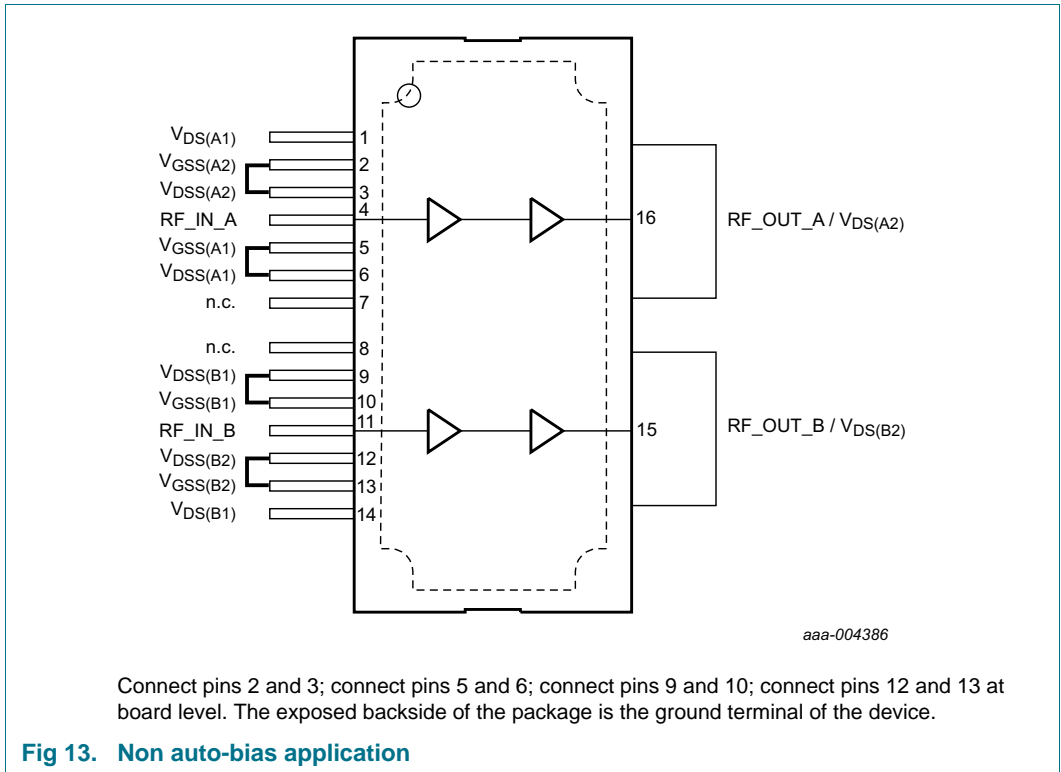
- (1) T_{case} = -30 °C
- (2) T_{case} = +25 °C
- (3) T_{case} = +100 °C

Fig 11. Power gain as a function of output power; typical values

8.1.3 2-Tone CW



8.2 Application without auto-bias



9. Test information

9.1 Ruggedness

The BLM7G22S-60PB and BLM7G22S-60PBG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq1} = 75\text{ mA}$; $I_{Dq2} = 233\text{ mA}$; $P_L = 27\text{ W}$ (W-CDMA); $f = 2140\text{ MHz}$.

9.2 Impedance information

Table 9. Typical impedance

Measured load-pull data. Typical values per section unless otherwise specified.

f MHz	Z_S [1] Ω	Z_L [1] Ω
BLM7G22S-60PB		
2050	58.86 + j21.82	10.54 – j3.20
2110	58.70 + j29.76	10.23 – j2.72
2140	51.80 + j41.56	9.56 – j2.90
2170	47.31 + j44.60	9.10 – j2.80
2230	38.35 + j46.53	8.41 – j2.05
BLM7G22S-60PBG		
2080	55.62 + j18.89	15.89 – j2.28
2110	55.61 + j19.04	14.74 – j2.59
2140	55.60 + j19.12	13.56 – j2.75
2170	55.57 + j19.25	12.38 – j2.75
2200	55.53 + j19.39	11.20 – j2.61
2230	55.48 + j19.55	10.05 – j2.34

[1] Z_S and Z_L defined in [Figure 14](#).

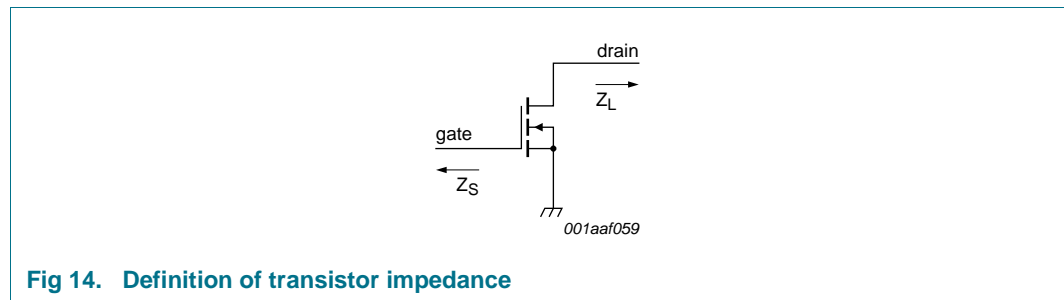
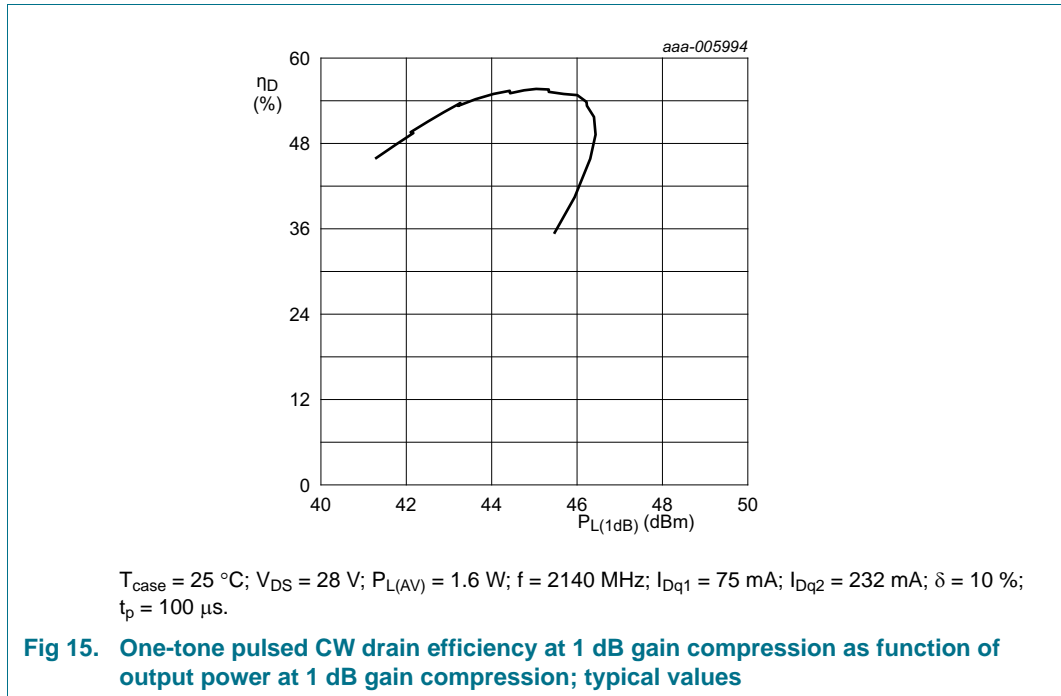


Fig 14. Definition of transistor impedance

9.3 Performance curves

Performance curves are measured per section.



10. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat)

SOT1211-1

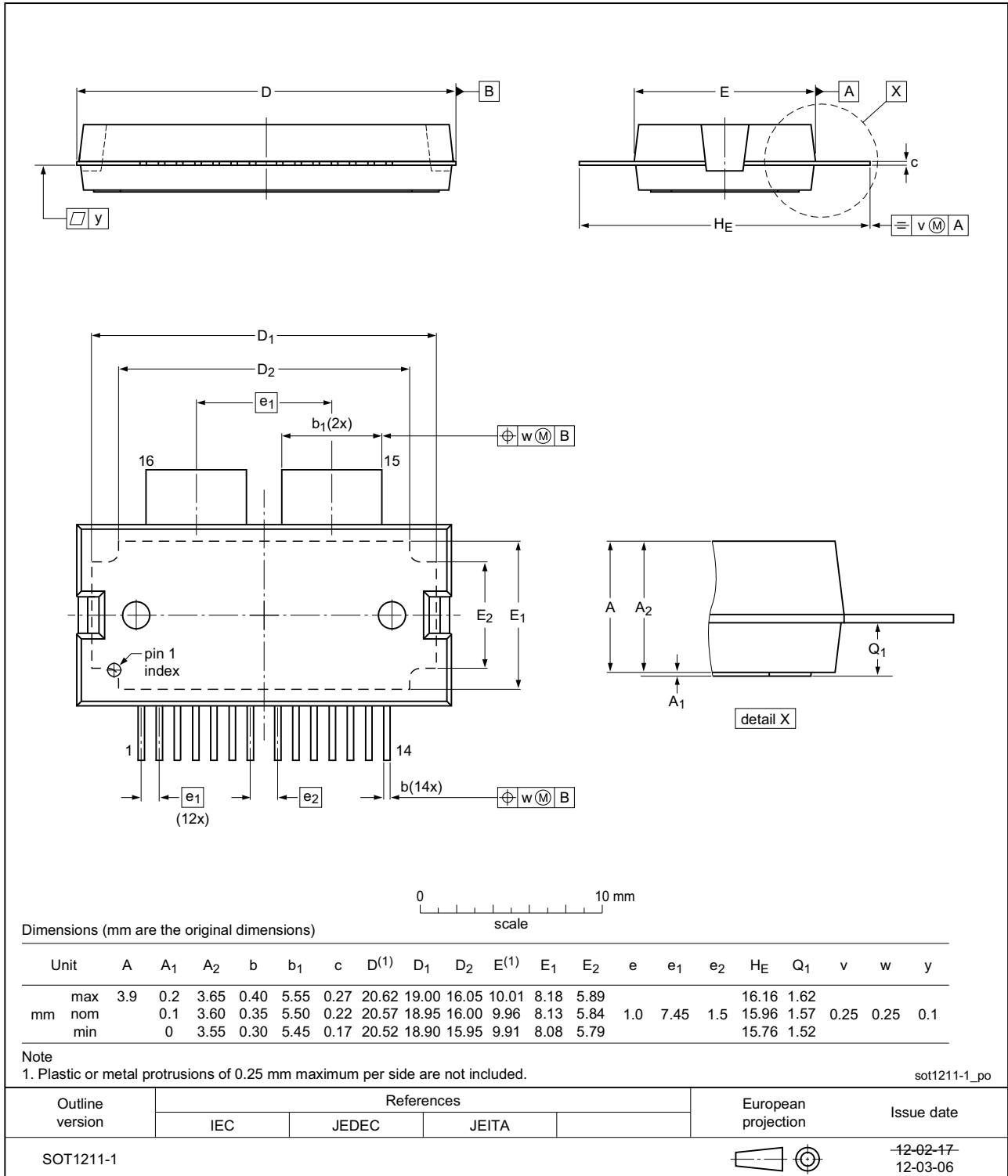


Fig 16. Package outline SOT1211-1 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads

SOT1212-1

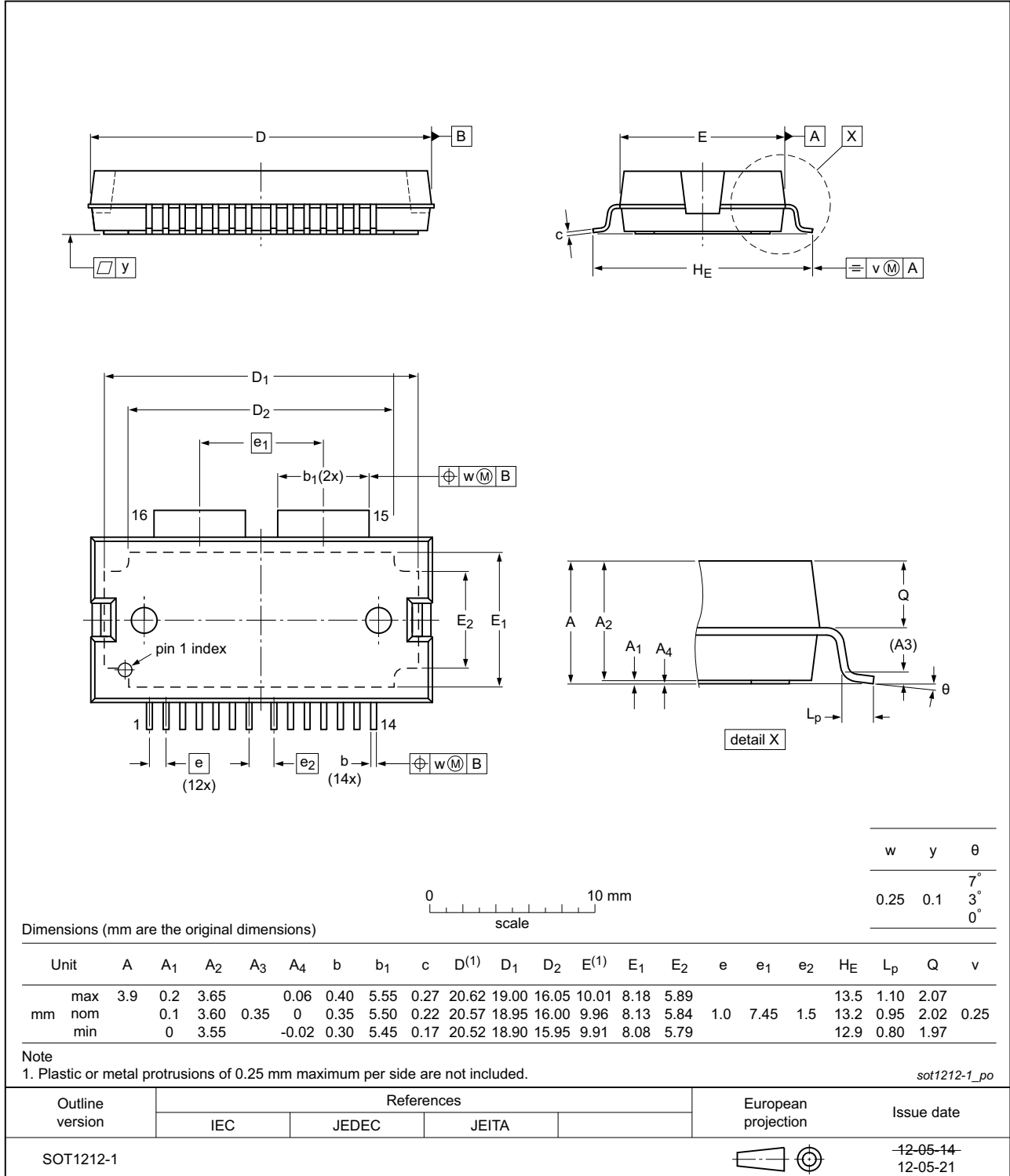


Fig 17. Package outline SOT1212-1 (HSOP16)

11. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Waveform
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GEN7	Seventh Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G22S-60PB_7G22S-60PBG v.1	20121211	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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