

# BLM7G24S-30BG

LDMOS 2-stage power MMIC

Rev. 1 — 4 November 2013

Product data sheet

## 1. Product profile

### 1.1 General description

The BLM7G24S-30BG is a 2-stage power MMIC using NXP's state of the art Gen7 LDMOS technology. This device is perfectly suited as general purpose driver in the frequency range from 2100 MHz to 2400 MHz. Available in gull wing.

**Table 1. Application performance**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  $I_{Dq1} = 75\text{ mA}$ ;  $I_{Dq2} = 233\text{ mA}$ .

Test signal: 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; unless otherwise specified in a class-AB application circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L(AV)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	ACPR (dBc)
2-carrier W-CDMA	2140	28	1.6	31.5	11.3	-43
2-carrier W-CDMA	2350	28	1.6	29.3	10.7	-42

### 1.2 Features and benefits

- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated current sense
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use (input matched to 50 Ω; output partially matched)
- Designed for broadband operation (frequency 2100 MHz to 2400 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

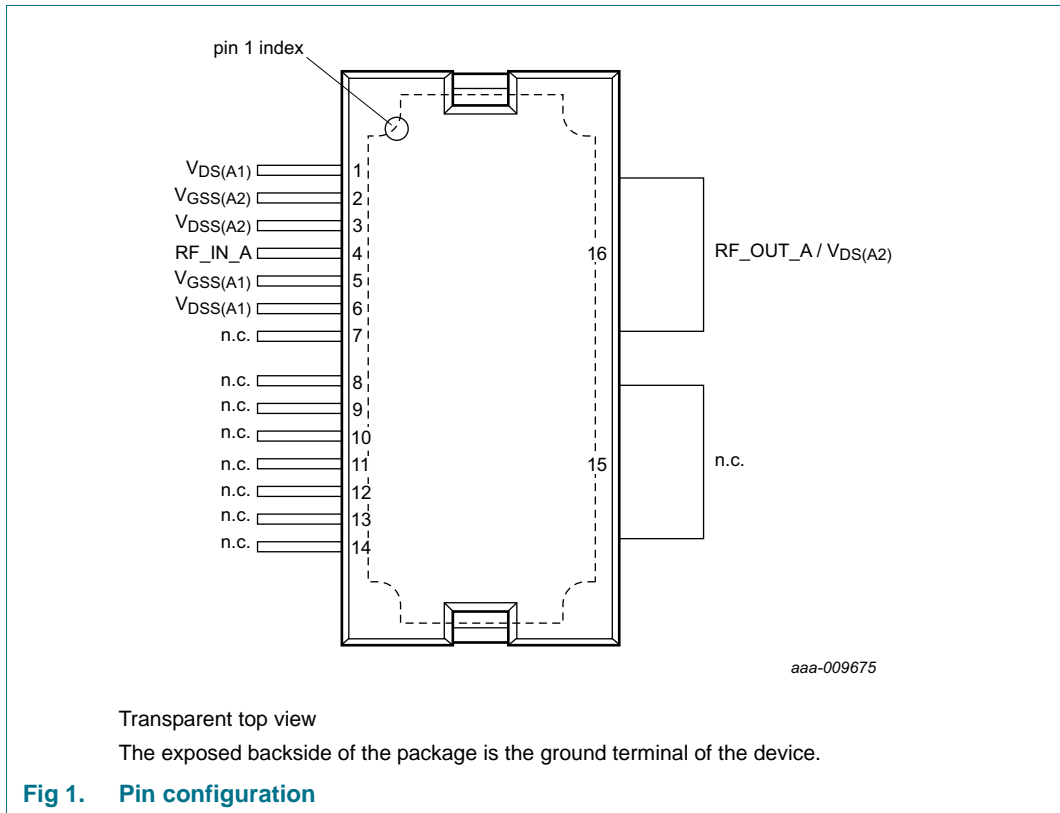
### 1.3 Applications

RF power MMIC for W-CDMA base stations in the 2100 MHz to 2400 MHz frequency range.



## 2. Pinning information

### 2.1 Pinning



### 2.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of stage A1
$V_{GSS(A2)}$	2	gate sense FET and gate source voltage of stage A2
$V_{DSS(A2)}$	3	drain sense FET source voltage of stage A2
RF_IN_A	4	RF input path A
$V_{GSS(A1)}$	5	gate sense FET and gate source voltage of stage A1
$V_{DSS(A1)}$	6	drain sense FET source voltage of stage A1
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected

**Table 2. Pin description ...continued**

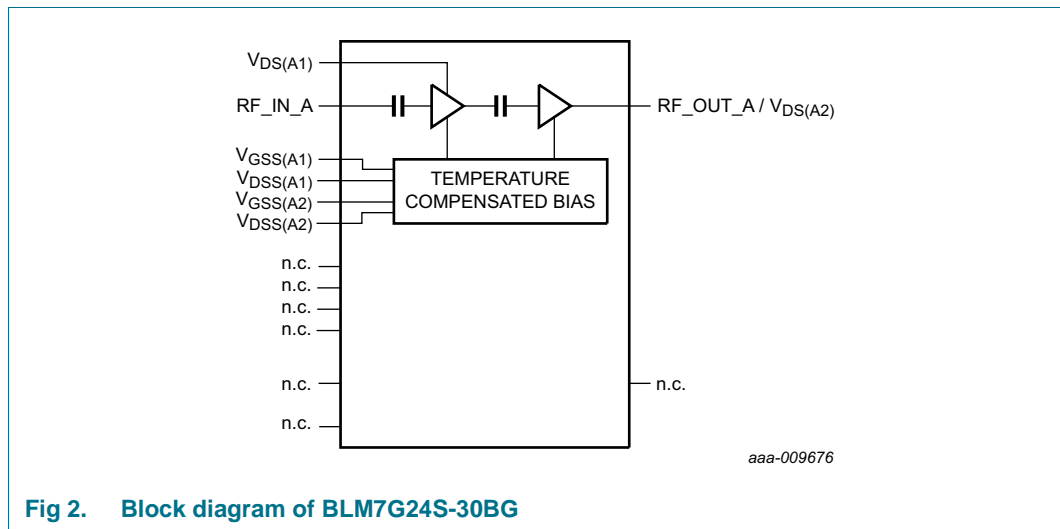
Symbol	Pin	Description
n.c.	15	not connected
RF_OUT_A/V <sub>DS(A2)</sub>	16	RF output path A / drain source voltage of stage A2
GND	flange	RF ground

### 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BLM7G24S-30BG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-1

### 4. Block diagram



**Fig 2. Block diagram of BLM7G24S-30BG**

### 5. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage		-	65	V
V <sub>GS</sub>	gate-source voltage		-0.5	+13	V
V <sub>GS(sense)</sub>	sense gate-source voltage		-0.5	+9	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[1]	225	°C
T <sub>case</sub>	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

## 6. Thermal characteristics

**Table 5. Thermal characteristics**

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; $T_{case} = 90\text{ °C}$ ; $P_L = 1.6\text{ W}$	[1] 2.2	K/W
		driver stage; $T_{case} = 90\text{ °C}$ ; $P_L = 1.6\text{ W}$	[1] 6.4	K/W

[1] When operated with a CW signal.

## 7. Characteristics

**Table 6. DC characteristics**

$T_{case} = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Final stage</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.422\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 42\text{ mA}$	1.5	1.9	2.3	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$ ; $I_D = 253\text{ mA}$	1.7	2.1	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	7.8	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 1478\text{ mA}$	-	2.85	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 1.48\text{ A}$	-	350	-	$\text{m}\Omega$
$I_{Dq}$	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$ ; $V_{DS} = 28\text{ V}$	208	233	257	mA
<b>Driver stage</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.116\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 11.6\text{ mA}$	1.5	1.9	2.3	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$ ; $I_D = 69.6\text{ mA}$	1.7	2.1	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	2.2	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 406\text{ mA}$	-	0.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 0.4\text{ A}$	-	2350	-	$\text{m}\Omega$
$I_{Dq}$	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$ ; $V_{DS} = 28\text{ V}$	67	75	83	mA

**Table 7. RF Characteristics**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq1} = 75\text{ mA}$ ;  $I_{Dq2} = 233\text{ mA}$ . Test signal: 2-carrier W-CDMA; 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz;  $f_1 = 2112.5\text{ MHz}$ ;  $f_2 = 2117.5\text{ MHz}$ ;  $f_3 = 2162.5\text{ MHz}$ ;  $f_4 = 2167.5\text{ MHz}$ ; unless otherwise specified measured in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 1.6\text{ W}$	29.5	31.5	33.5	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 1.6\text{ W}$	10	11.3	-	%
$RL_{in}$	input return loss	$P_{L(AV)} = 1.6\text{ W}$	-	-17	-10	dB
ACPR	adjacent channel power ratio	$P_{L(AV)} = 1.6\text{ W}$	-	-43	-40	dBc

## 8. Application information

### 8.1 Circuit information for application circuit (2.1 GHz to 2.2 GHz)

**Table 8. List of components**

For test circuit see [Figure 3](#).

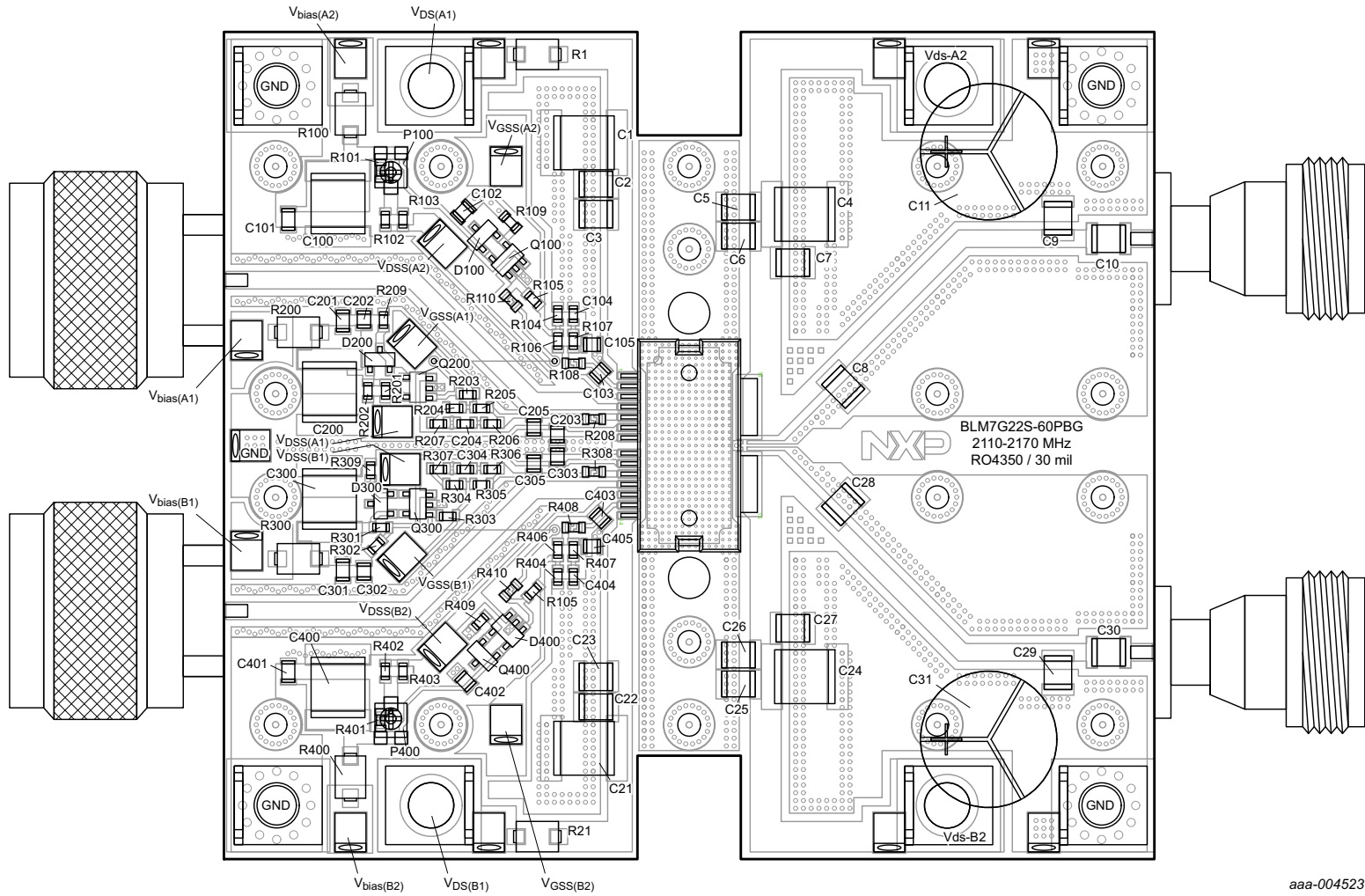
Component	Description	Value	Remarks
C1, C4, C100, C200	capacitor	10 $\mu\text{F}$	
C2, C5, C6,	capacitor	1 $\mu\text{F}$	
C3, C7, C10	capacitor	8.2 pF	<a href="#">[1]</a>
C8	capacitor	1.6 pF	<a href="#">[1]</a>
C9	capacitor	0.4 pF	<a href="#">[1]</a>
C11	electrolytic capacitor	470 $\mu\text{F}$	
C101, C201	capacitor	100 nF	
C102, C103, C105, C202, C203, C205	capacitor	12 pF	<a href="#">[2]</a>
C104, C204	capacitor	4.7 $\mu\text{F}$	
C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C300, C301, C302, C303, C304, C305, C400, C401, C402, C403, C404, C405	capacitor	-	not mounted
D100, D200	IC: LM4051	-	
D300, D400	IC	-	not mounted
P100	potentiometer	-	do not populate
P400	potentiometer	-	not mounted
Q100, Q200	IC	-	LM7341
Q300, Q400	IC	-	not mounted
R1	ferrite bead	-	
R100, R200	resistor	4.7 $\Omega$	
R101, R108, R110, R208	resistor	0 $\Omega$	
R102	resistor	360 $\Omega$	1% tolerance
R103	resistor	330 $\Omega$	1% tolerance
R104, R203	resistor	68 k $\Omega$	
R105	resistor	10 k $\Omega$	

**Table 8.** List of components ...continued  
For test circuit see [Figure 3](#).

Component	Description	Value	Remarks
R106, R205	resistor	820 $\Omega$	
R107, R206	resistor	47 $\Omega$	
R109, R209	resistor	300 k $\Omega$	
R201	resistor	180 $\Omega$	1% tolerance
R202	resistor	3.6 k $\Omega$	1% tolerance
R204	resistor	9.1 k $\Omega$	
R207	resistor	1 k $\Omega$	
R21, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409	resistor	-	not mounted

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.



aaa-004523

Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.762 mm.

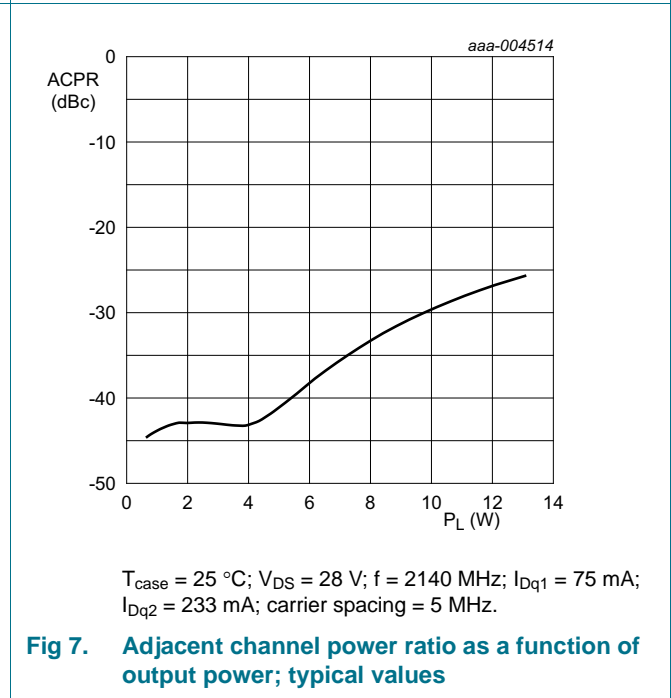
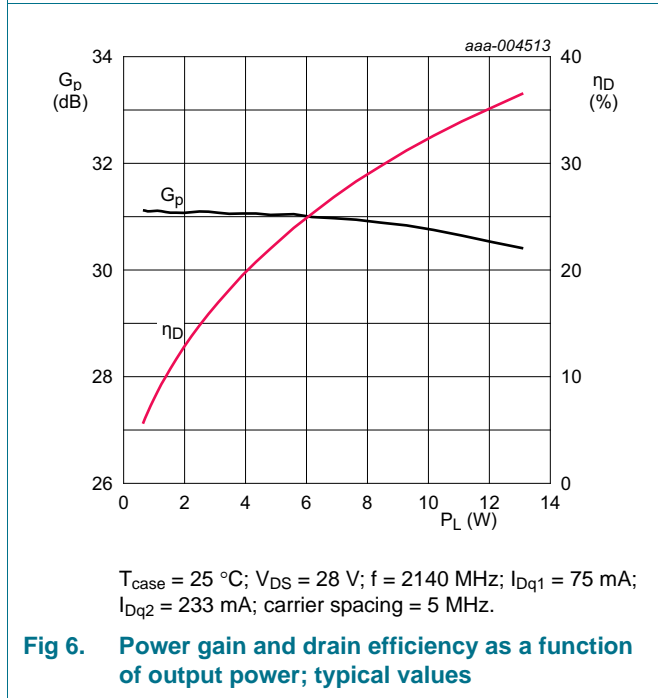
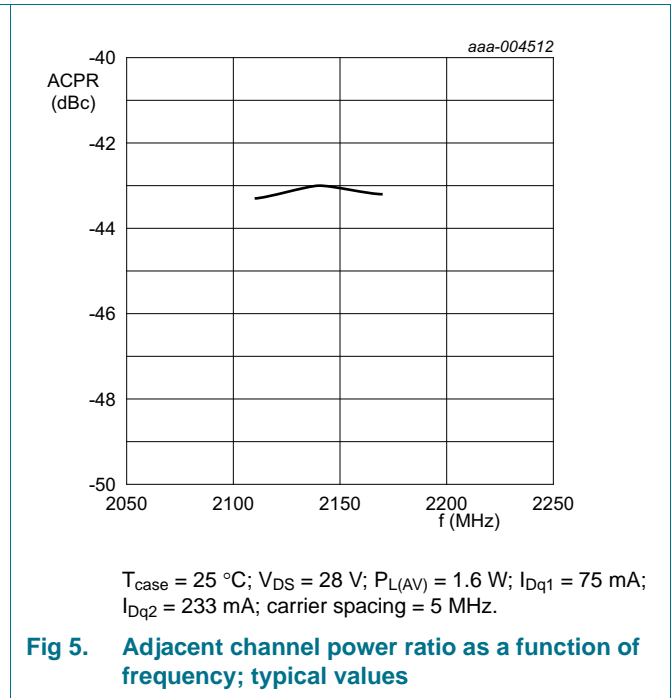
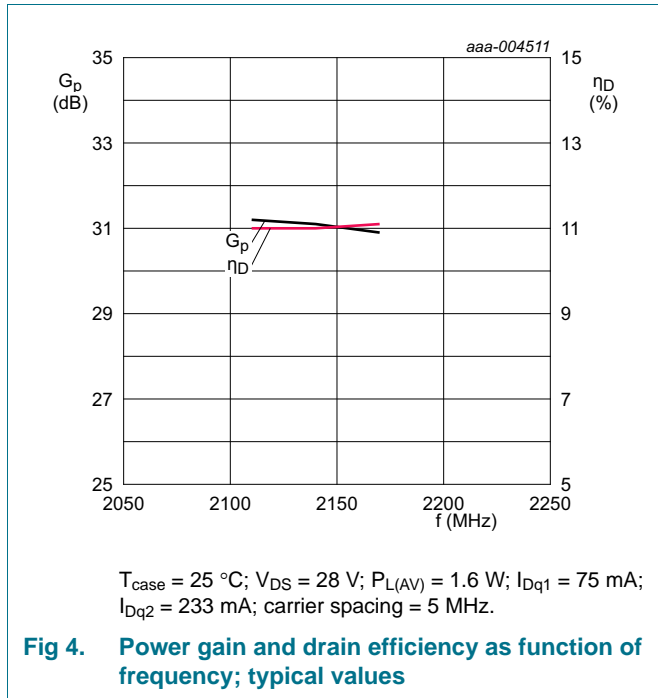
See [Table 8](#) for a list of components.

**Fig 3. Component layout for class-AB application circuit with auto-bias (a half section of the BLM7G22S-60PBG [section A] is used for characterization)**

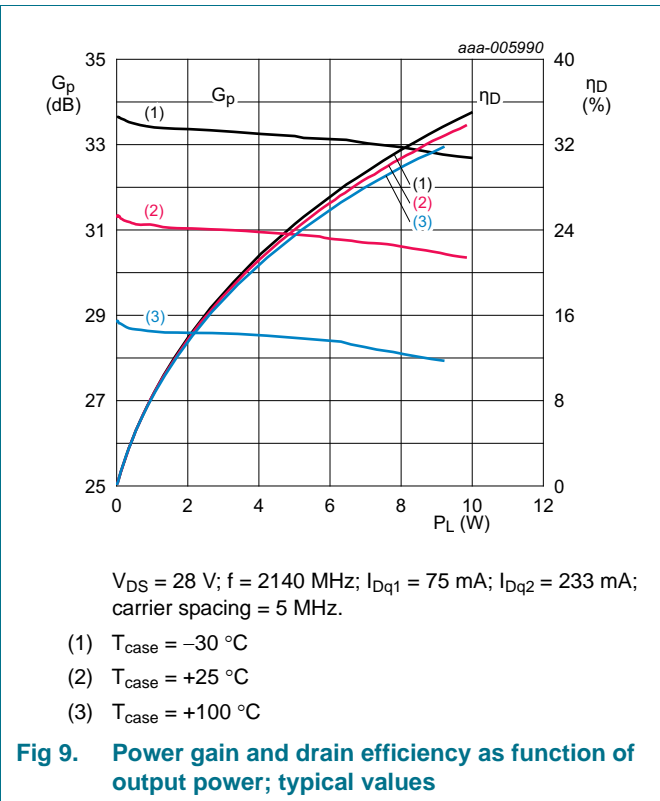
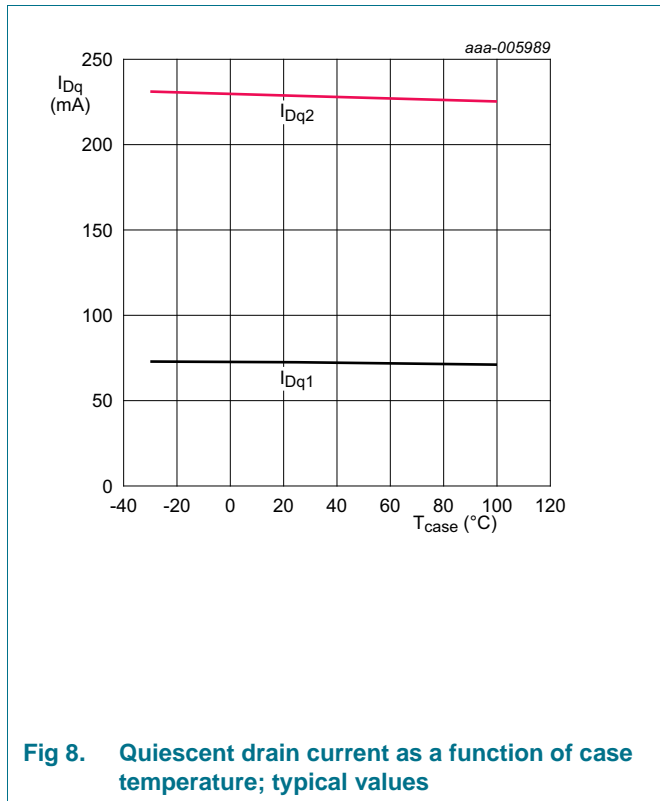
8.2 Performance curves (2.1 GHz to 2.2 GHz)

Performance curves are measured in a class-AB dedicated application circuit with auto-bias from 2.1 GHz to 2.2 GHz, see [Table 8](#) and [Figure 3](#).

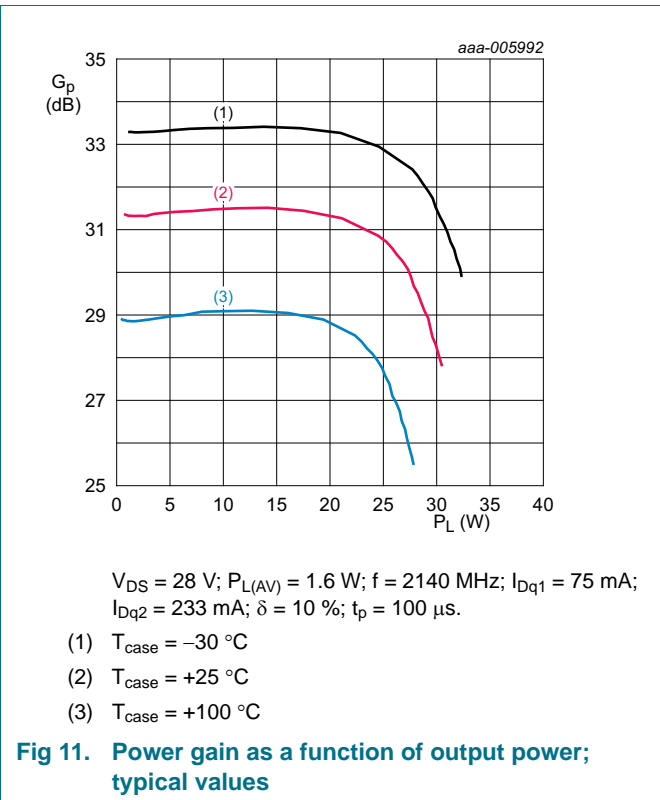
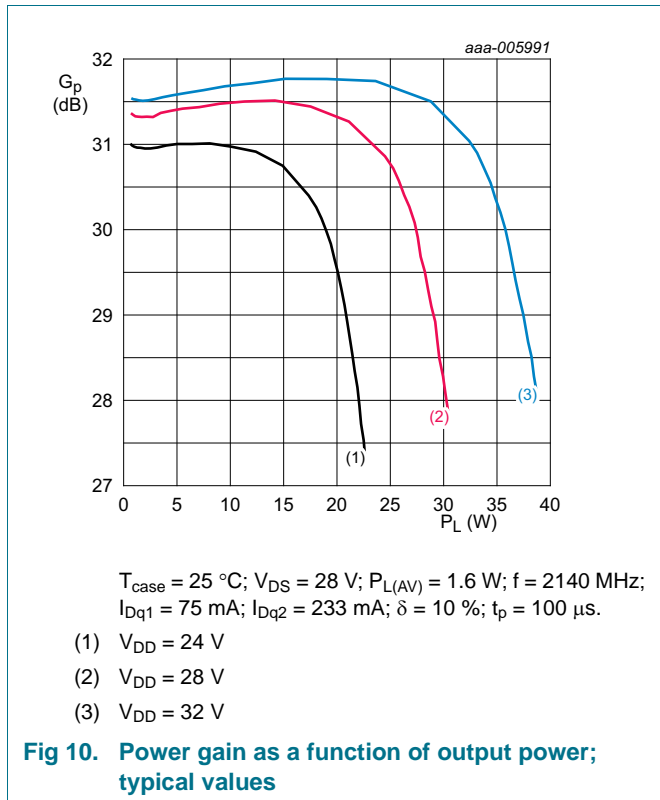
8.2.1 W-CDMA



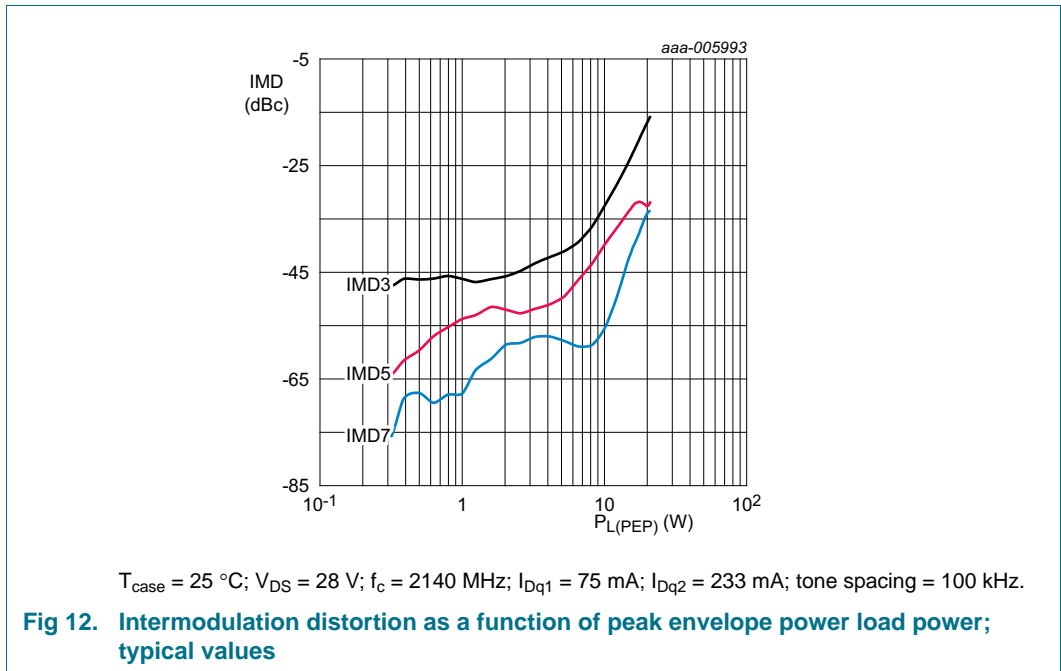




8.2.2 1-Tone pulsed CW



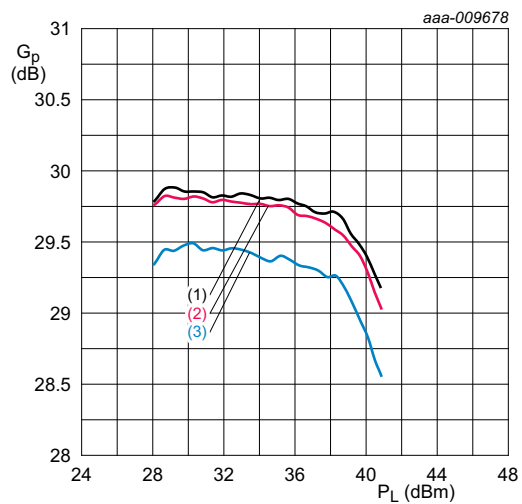
8.2.3 2-Tone CW



### 8.3 Performance curves (2.3 GHz to 2.4 GHz)

Performance curves are measured in a class-AB dedicated application circuit with auto-bias from 2.3 GHz to 2.4 GHz.

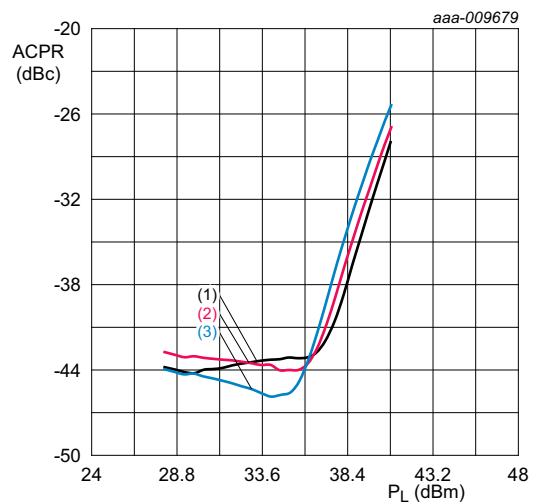
#### 8.3.1 2-Carrier W-CDMA



$V_{DS} = 28\text{ V}$ ;  $I_{Dq1} = 220\text{ mA}$ ;  $I_{Dq2} = 75\text{ mA}$ ; carrier spacing = 5MHz.

- (1)  $f = 2300\text{ MHz}$
- (2)  $f = 2350\text{ MHz}$
- (3)  $f = 2400\text{ MHz}$

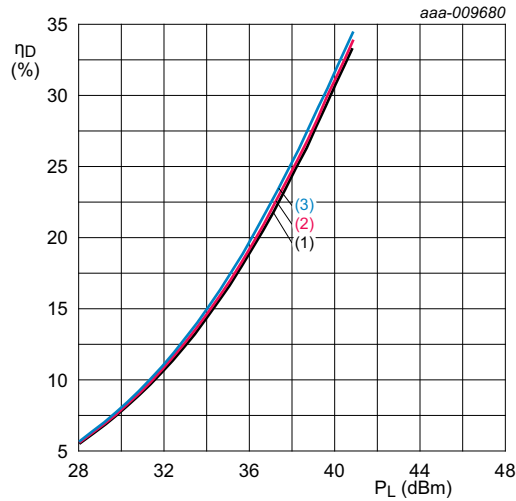
**Fig 13. Power gain as a function of output power; typical values**



$V_{DS} = 28\text{ V}$ ;  $I_{Dq1} = 220\text{ mA}$ ;  $I_{Dq2} = 75\text{ mA}$ ; carrier spacing = 5MHz.

- (1)  $f = 2300\text{ MHz}$
- (2)  $f = 2350\text{ MHz}$
- (3)  $f = 2400\text{ MHz}$

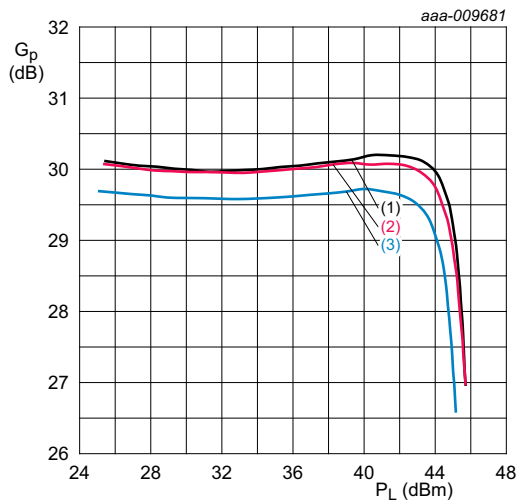
**Fig 14. Adjacent channel power ratio as a function of output power; typical values**



$V_{DS} = 28\text{ V}$ ;  $I_{DQ1} = 220\text{ mA}$ ;  $I_{DQ2} = 75\text{ mA}$ ; carrier spacing = 5MHz.  
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

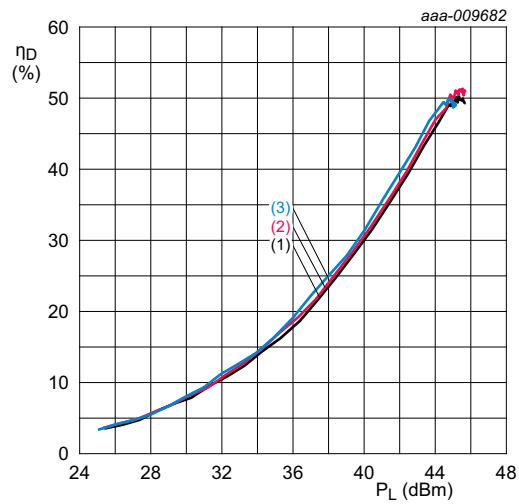
**Fig 15. Drain efficiency as a function of output power; typical values**

**8.3.2 Pulsed CW**



$V_{DS} = 28\text{ V}$ ;  $I_{DQ1} = 220\text{ mA}$ ;  $I_{DQ2} = 75\text{ mA}$ ;  $\delta = 10\%$ ;  
 $t_p = 100\ \mu\text{s}$ .  
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

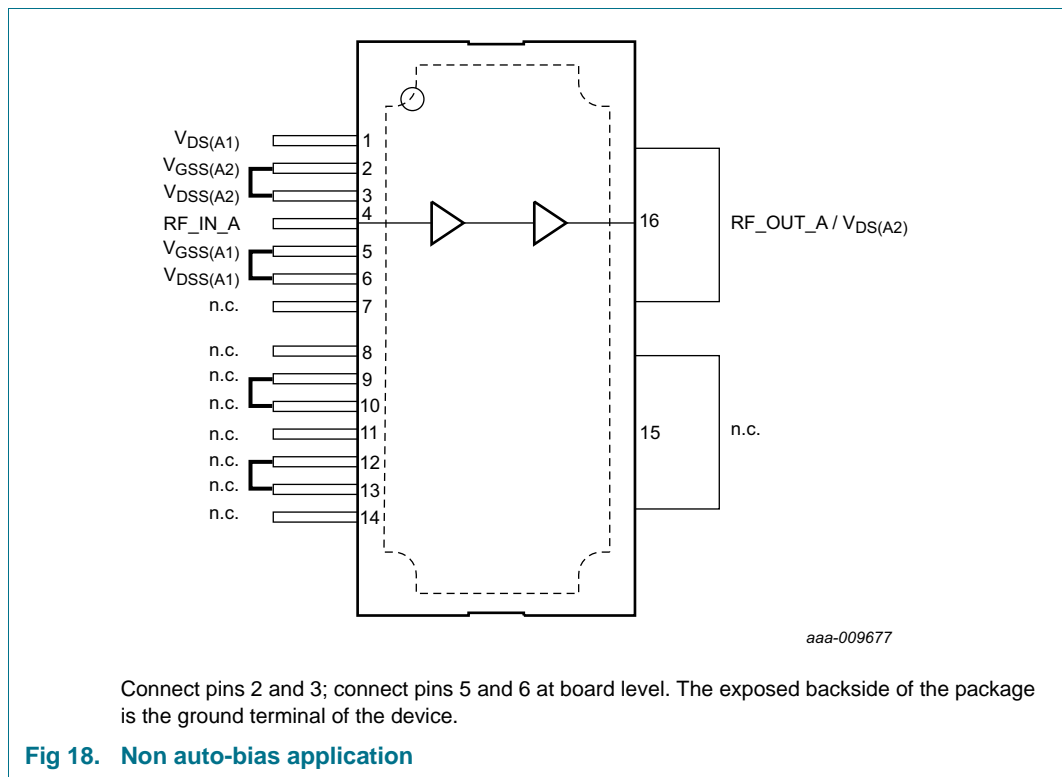
**Fig 16. Power gain as a function of output power; typical values**



$V_{DS} = 28\text{ V}$ ;  $I_{DQ1} = 220\text{ mA}$ ;  $I_{DQ2} = 75\text{ mA}$ ;  $\delta = 10\%$ ;  
 $t_p = 100\ \mu\text{s}$ .  
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

**Fig 17. Efficiency as a function of output power; typical values**

### 8.4 Application without auto-bias



## 9. Test information

### 9.1 Ruggedness

The BLM7G24S-30BG is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq1} = 75\text{ mA}$ ;  $I_{Dq2} = 233\text{ mA}$ ;  $P_L = 27\text{ W}$  (W-CDMA);  $f = 2140\text{ MHz}$ .

### 9.2 Impedance information

**Table 9. Typical impedance**

Measured load-pull data. Typical values per section unless otherwise specified.

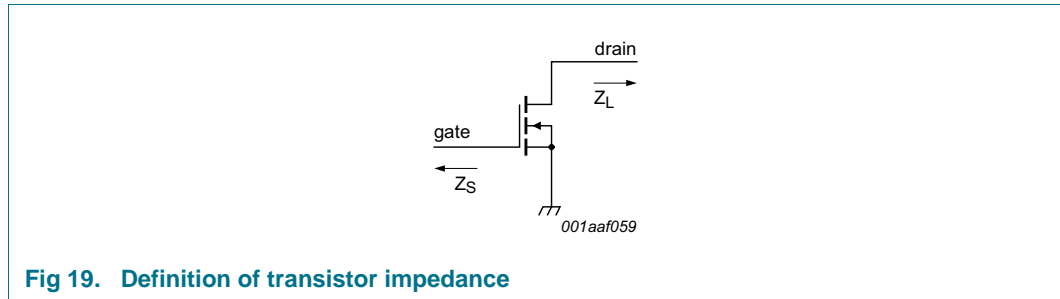
f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)
2080	55.62 + j18.89	15.89 – j2.28
2110	55.61 + j19.04	14.74 – j2.59
2140	55.60 + j19.12	13.56 – j2.75
2170	55.57 + j19.25	12.38 – j2.75
2200	55.53 + j19.39	11.20 – j2.61
2230	55.48 + j19.55	10.05 – j2.34
2300	34.51 + j41.45	7.06 – j6.36

**Table 9. Typical impedance ...continued**

Measured load-pull data. Typical values per section unless otherwise specified.

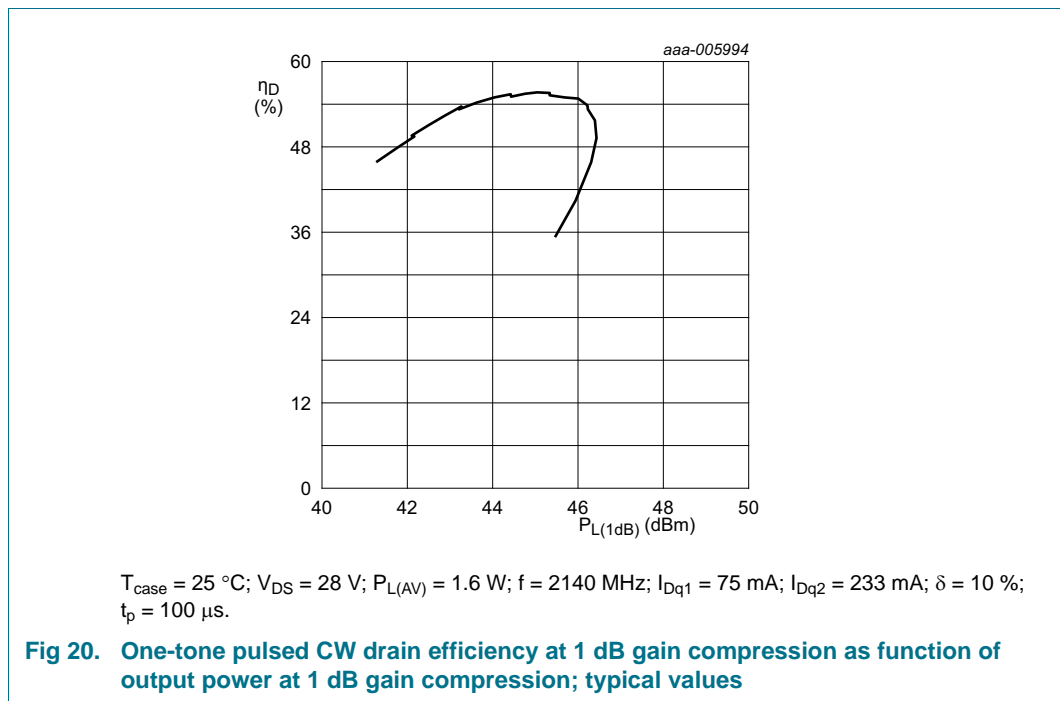
f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)
2350	29.26 + j36.91	6.35 – j6.24
2400	22.86 + j32.52	5.65 – j6.15

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 19](#).



**Fig 19. Definition of transistor impedance**

### 9.3 Performance curves



**Fig 20. One-tone pulsed CW drain efficiency at 1 dB gain compression as function of output power at 1 dB gain compression; typical values**

10. Package outline

HSOP16: plastic, heatsink small outline package; 16 leads

SOT1212-1

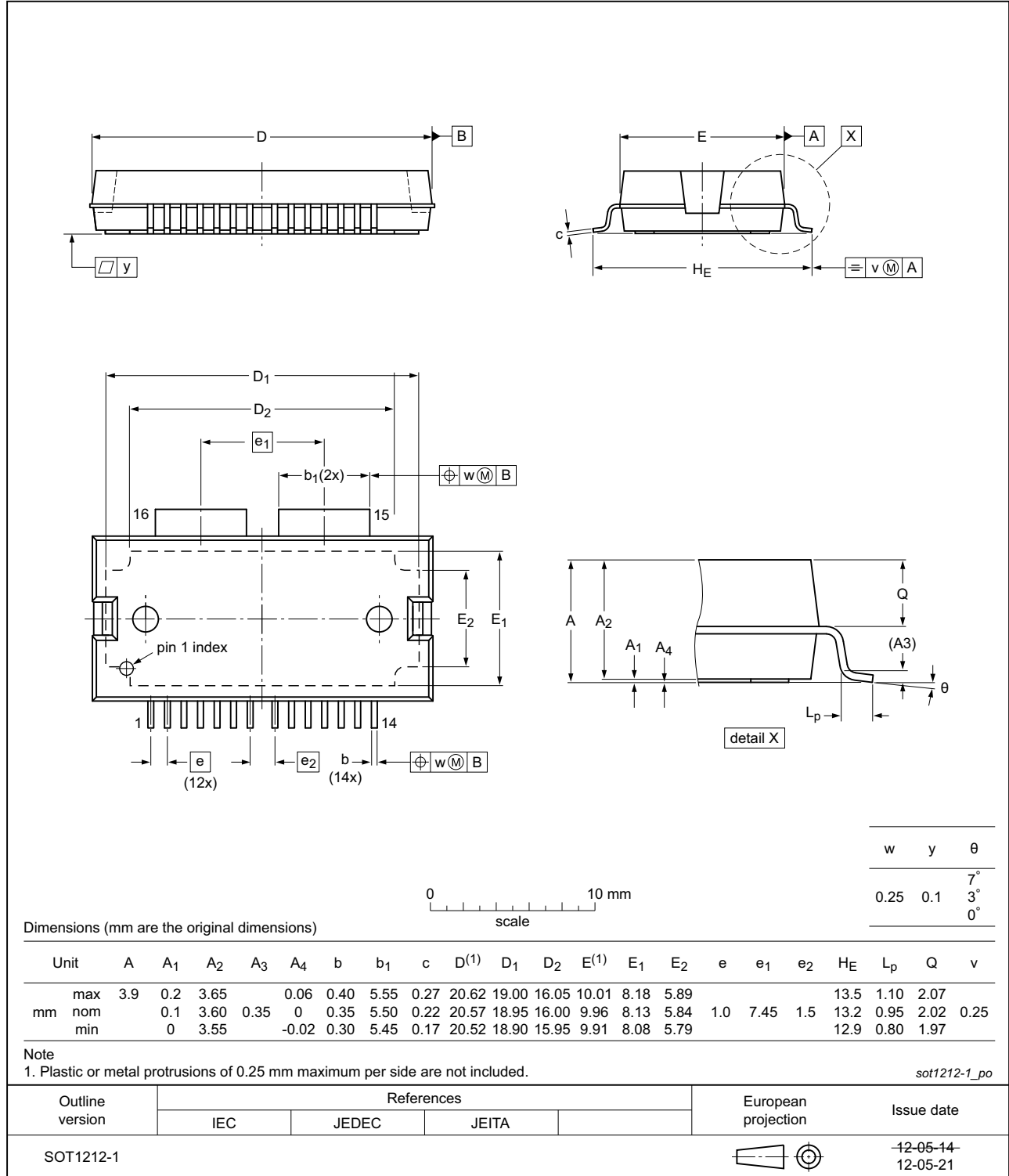


Fig 21. Package outline SOT1212-1 (HSOP16)

## 11. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Waveform
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
Gen7	Seventh-Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G24S-30BG v.1	20131104	Product data sheet	-	-



## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 16. Contents

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<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features and benefits .....	1
1.3	Applications .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>2</b>
2.1	Pinning .....	2
2.2	Pin description .....	2
<b>3</b>	<b>Ordering information</b> .....	<b>3</b>
<b>4</b>	<b>Block diagram</b> .....	<b>3</b>
<b>5</b>	<b>Limiting values</b> .....	<b>3</b>
<b>6</b>	<b>Thermal characteristics</b> .....	<b>4</b>
<b>7</b>	<b>Characteristics</b> .....	<b>4</b>
<b>8</b>	<b>Application information</b> .....	<b>5</b>
8.1	Circuit information for application circuit (2.1 GHz to 2.2 GHz) .....	5
8.2	Performance curves (2.1 GHz to 2.2 GHz) . . .	8
8.2.1	W-CDMA .....	8
8.2.2	1-Tone pulsed CW .....	9
8.2.3	2-Tone CW .....	10
8.3	Performance curves (2.3 GHz to 2.4 GHz) . . .	11
8.3.1	2-Carrier W-CDMA .....	11
8.3.2	Pulsed CW .....	12
8.4	Application without auto-bias .....	13
<b>9</b>	<b>Test information</b> .....	<b>13</b>
9.1	Ruggedness .....	13
9.2	Impedance information .....	13
9.3	Performance curves .....	14
<b>10</b>	<b>Package outline</b> .....	<b>15</b>
<b>11</b>	<b>Handling information</b> .....	<b>16</b>
<b>12</b>	<b>Abbreviations</b> .....	<b>16</b>
<b>13</b>	<b>Revision history</b> .....	<b>16</b>
<b>14</b>	<b>Legal information</b> .....	<b>17</b>
14.1	Data sheet status .....	17
14.2	Definitions .....	17
14.3	Disclaimers .....	17
14.4	Trademarks .....	18
<b>15</b>	<b>Contact information</b> .....	<b>18</b>
<b>16</b>	<b>Contents</b> .....	<b>19</b>

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