BUK9609-75A

N-channel TrenchMOS logic level FET

Rev. 4 — 30 August 2011 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

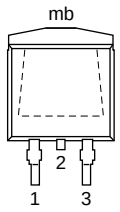
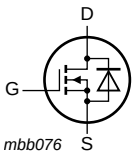
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	75	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; see Figure 3; see Figure 1	[1]	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	230	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 25$ A; $T_j = 25$ °C		-	-	9.95	mΩ
		$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C		-	7.23	8.5	mΩ
		$V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 13; see Figure 14		-	7.6	9	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75$ A; $V_{sup} \leq 75$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped		-	-	562	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9609-75A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

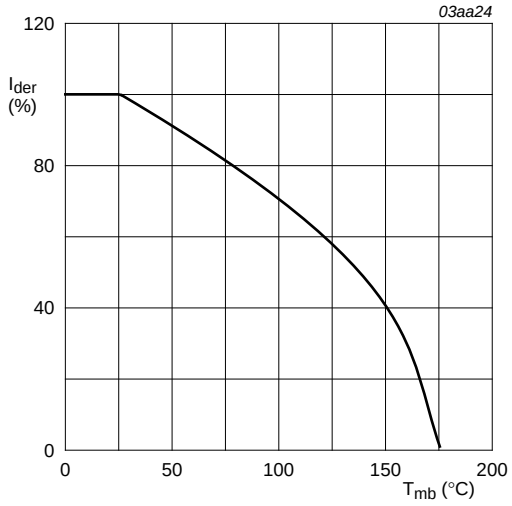
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

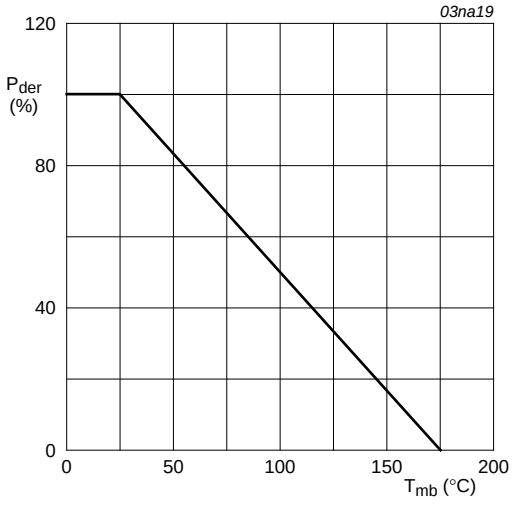
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	75	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	75	V
V_{GS}	gate-source voltage			-10	10	V
I_D	drain current	T_{mb} = 100 °C; V_{GS} = 5 V; see Figure 1	[1]	-	75	A
		T_{mb} = 25 °C; V_{GS} = 5 V; see Figure 3; see Figure 1	[1]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; see Figure 3		-	440	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	230	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50$ µs		-15	15	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	440	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \leq 75$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	562	mJ

[1] Continuous current is limited by package.



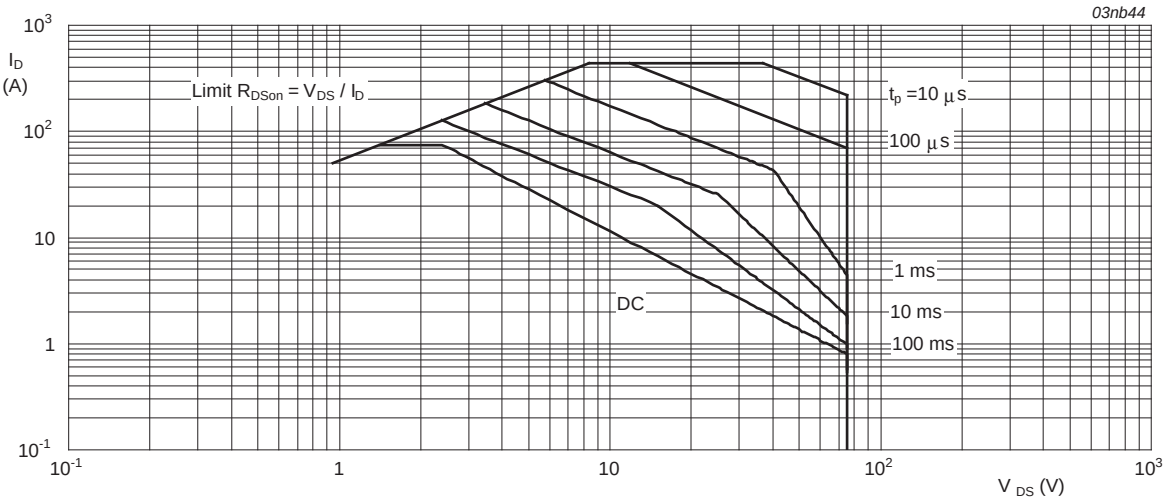
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.65	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

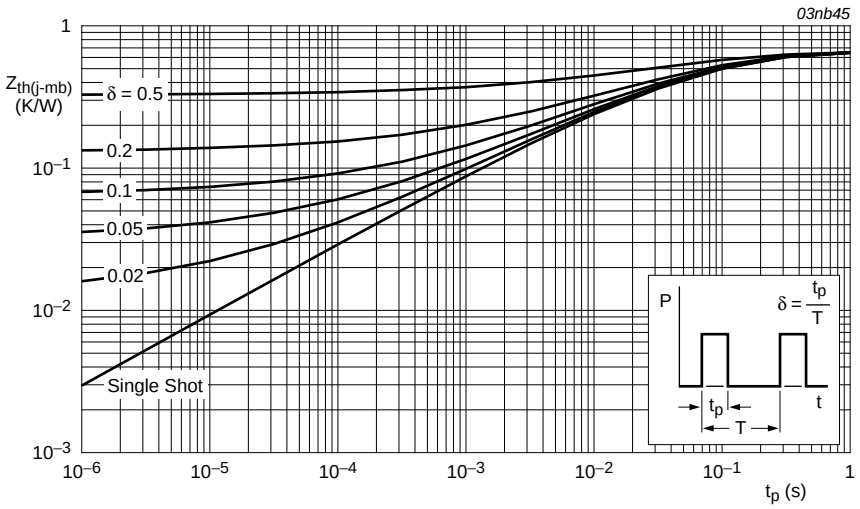
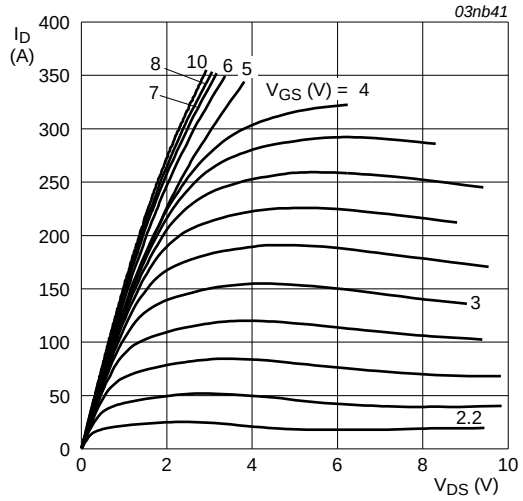


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

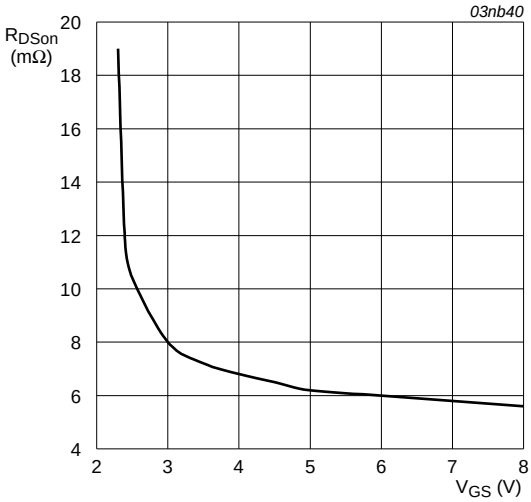
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	75	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	70	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 12	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 12	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 12	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C	-	-	9.95	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 13; see Figure 14	-	-	18.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	7.23	8.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 13; see Figure 14	-	7.6	9	mΩ
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 8	-	6631	8840	pF
C_{oss}	output capacitance		-	905	1090	pF
C_{rss}	reverse transfer capacitance		-	610	840	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	47	-	ns
t_r	rise time		-	185	-	ns
$t_{d(off)}$	turn-off delay time		-	424	-	ns
t_f	fall time		-	226	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die ; T_j = 25 °C	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die ; T_j = 25 °C	-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	70.3	-	ns
Q_r	recovered charge		-	213	-	nC



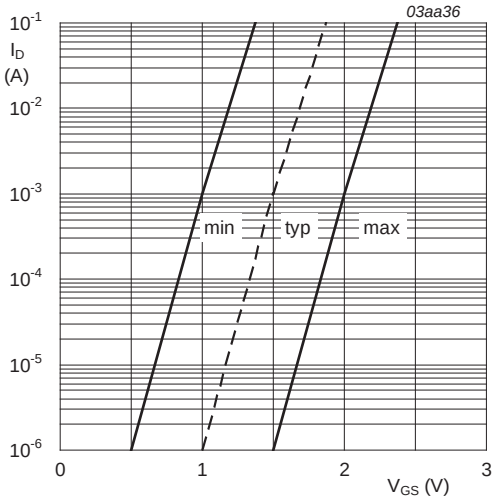
$T_j = 25°C; t_p = 300\mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



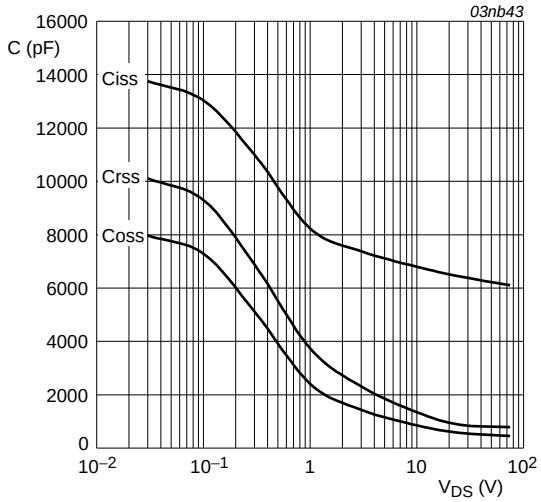
$T_j = 25°C; I_D = 25A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



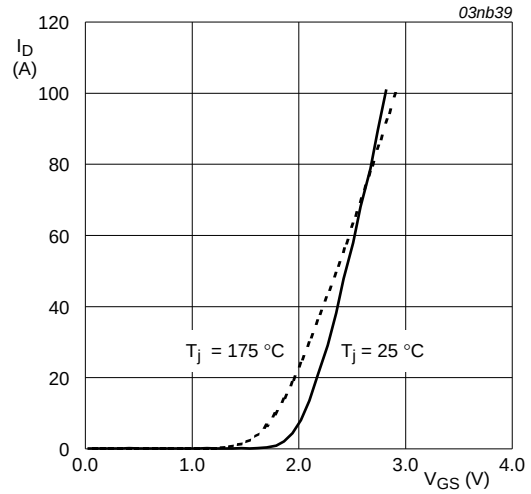
$T_j = 25°C; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



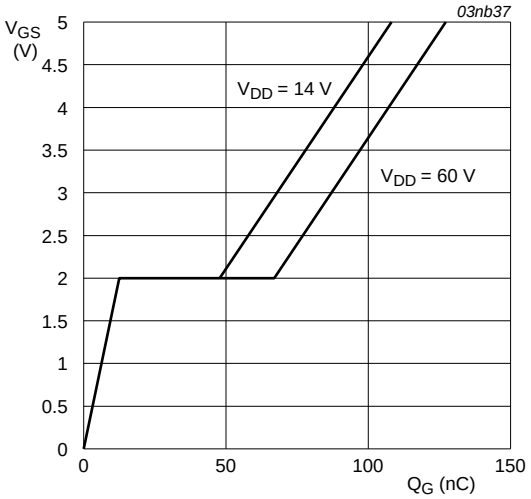
$V_{GS} = 0V; f = 1MHz$

Fig 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



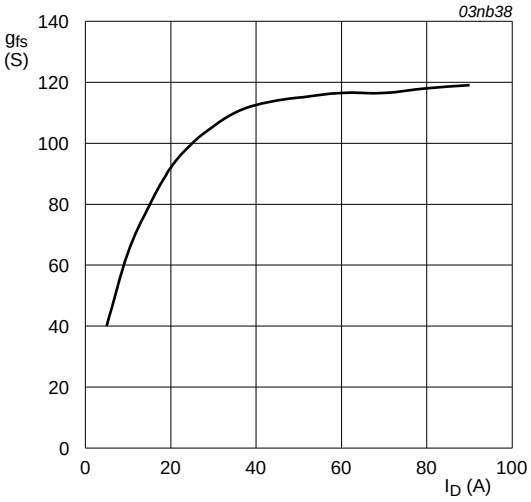
$V_{DS} = 25V$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



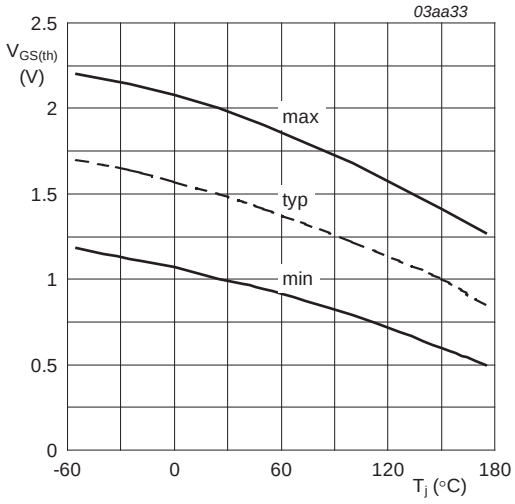
$T_j = 25°C; I_D = 25A$

Fig 10. Gate-source voltage as a function of gate charge; typical values



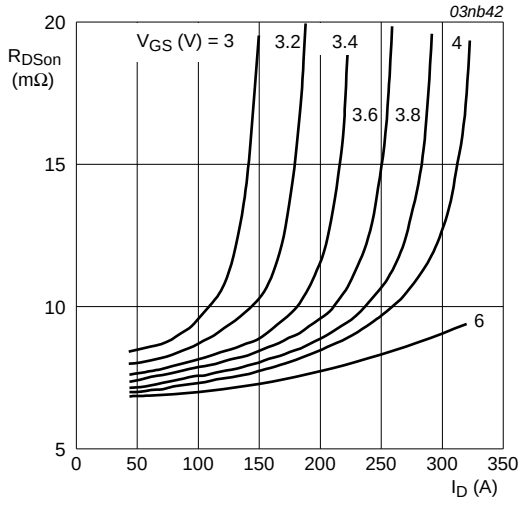
$T_j = 25°C; V_{DS} = 25V$

Fig 11. Forward transconductance as a function of drain current; typical values



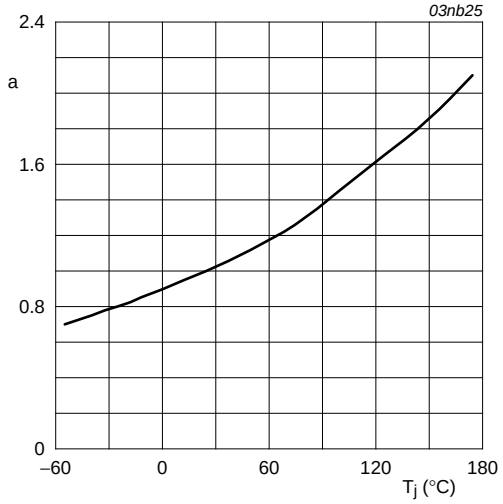
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



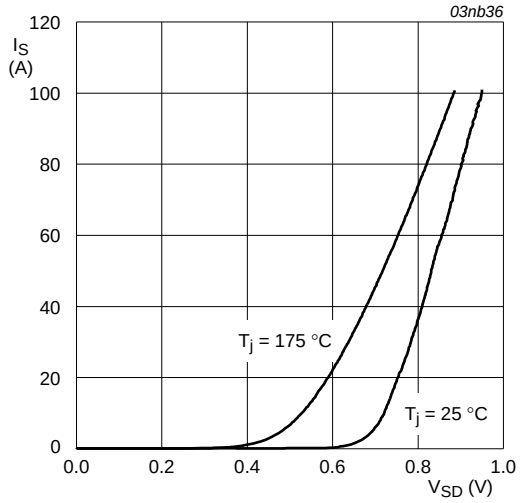
$T_j = 25°C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 14. Normalized drain-source on-state resistance factor as a function of junction temperature

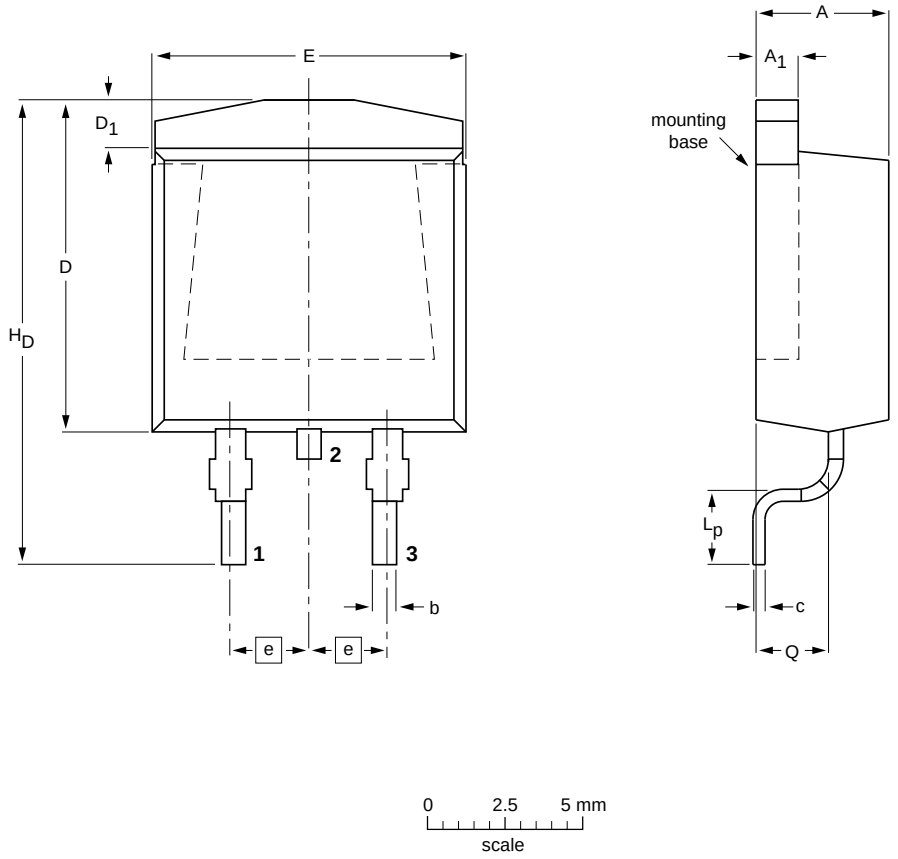


$V_{GS} = 0V$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9609-75A v.4	20110830	Product data sheet	-	BUK9609-75A v.3
Modifications:	• Various changes to content.			
BUK9609-75A v.3	20080922	Product data sheet	-	BUK9509_9609_75A v.2

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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