

# LD6938 series

Dual low-dropout regulators, low noise, 300 mA

Rev. 1 — 11 July 2013

Objective data sheet

## 1. Product profile

### 1.1 General description

The LD6938 series consists of small-size dual Low DropOut regulators (LDO). Each device delivers two times 300 mA with a typical voltage drop of 240 mV at full output load. The devices offer two separate fixed nominal output voltages ( $V_{O(nom)}$ ) in the range of 1.2 V to 3.3 V.

The LDO has an integrated Soft start to control the inrush current during start-up. The output mode, when disabled, can be high-ohmic 3-state or auto discharge. Optionally a delayed start-up circuit is available for the second output. The devices are available in a 6-bump Wafer-Level Chip-Scale Package (WLCSP) with a height of 0.47 mm.

### 1.2 Features and benefits

- High Power Supply Rejection Ratio (PSRR)
- Low output noise
- Low quiescent current
- Extremely low standby current ( $\leq 0.1 \mu\text{A}$ )
- Soft start circuit to limit inrush current
- Output current limiter with foldback circuit
- Overtemperature protection
- Delayed output circuit for second LDO (optional)
- Auto discharge or high-ohmic mode for output when disabled
- WLCSP6 with 0.4 mm pitch and package size of 1.2 mm  $\times$  0.8 mm  $\times$  0.47 mm

### 1.3 Applications

- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

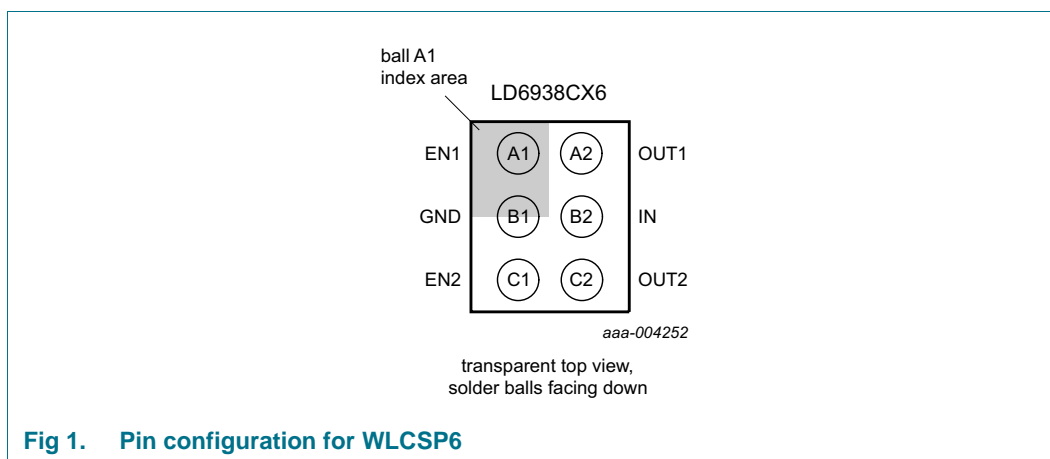
### 1.4 Quick reference data

- $I_O = 300 \text{ mA}$  for each LDO
- PSRR = 80 dB at 1 kHz
- RMS noise  $V_{n(o)RMS} = 70 \mu\text{V}$  at 10 Hz to 100 kHz
- $t_{startup(reg)} \leq 200 \mu\text{s}$
- $V_I = 1.7 \text{ V to } 5.5 \text{ V}$
- $V_O = 1.2 \text{ V to } 3.3 \text{ V}$  (fixed value)
- Drop voltage  $V_{do} = 240 \text{ mV}$  at  $I_O = 300 \text{ mA}$
- Quiescent current  $I_q = 30 \mu\text{A}$  for each LDO at  $I_O = 0 \text{ mA}$



## 2. Pinning information

### 2.1 Pinning



### 2.2 Pin description

**Table 1. Pin description for WLCSP6**

| Symbol | Pin | Description                |
|--------|-----|----------------------------|
| EN1    | A1  | regulator 1 enable input   |
| OUT1   | A2  | regulator 1 output voltage |
| GND    | B1  | supply ground              |
| IN     | B2  | supply voltage input       |
| EN2    | C1  | regulator 2 enable input   |
| OUT2   | C2  | regulator 2 output voltage |

### 3. Ordering information

Table 2. Ordering information

| Type number | Package |  |         |
|-------------|---------|--|---------|
|             | Name    | Description                                    | Version |
| LD6938CX6   | WLCSP6  | wafer level chip-size package; 6 bumps (2 × 3) | -       |

#### 3.1 Ordering options

Further output voltage versions and optional delay circuit for the second LDO are available on request; see [Section 15 "Contact information"](#).

Table 3. Type number extension of high ohmic output

| Type number     | Nominal output voltage $V_{O(nom)}$ |       |
|-----------------|-------------------------------------|-------|
|                 | OUT1                                | OUT2  |
| LD6938CX6/1818H | 1.8 V                               | 1.8 V |

Table 4. Type number extension for auto discharge

| Type number        | Nominal output voltage $V_{O(nom)}$ |        |
|--------------------|-------------------------------------|--------|
|                    | OUT1                                | OUT2   |
| LD6938CX6/1215PL   | 1.2 V                               | 1.5 V  |
| LD6938CX6/1218PL   | 1.2 V                               | 1.8 V  |
| LD6938CX6/18125PL  | 1.8 V                               | 1.25 V |
| LD6938CX6/1818PL   | 1.8 V                               | 1.8 V  |
| LD6938CX6/1833PL   | 1.8 V                               | 3.3 V  |
| LD6938CX6/285285PL | 2.85 V                              | 2.85 V |
| LD6938CX6/3018PL   | 3.0 V                               | 1.8 V  |
| LD6938CX6/3030PL   | 3.0 V                               | 3.0 V  |
| LD6938CX6/33285PL  | 3.3 V                               | 2.85 V |
| LD6938CX6/3333PL   | 3.3 V                               | 3.3 V  |

4. Block diagram

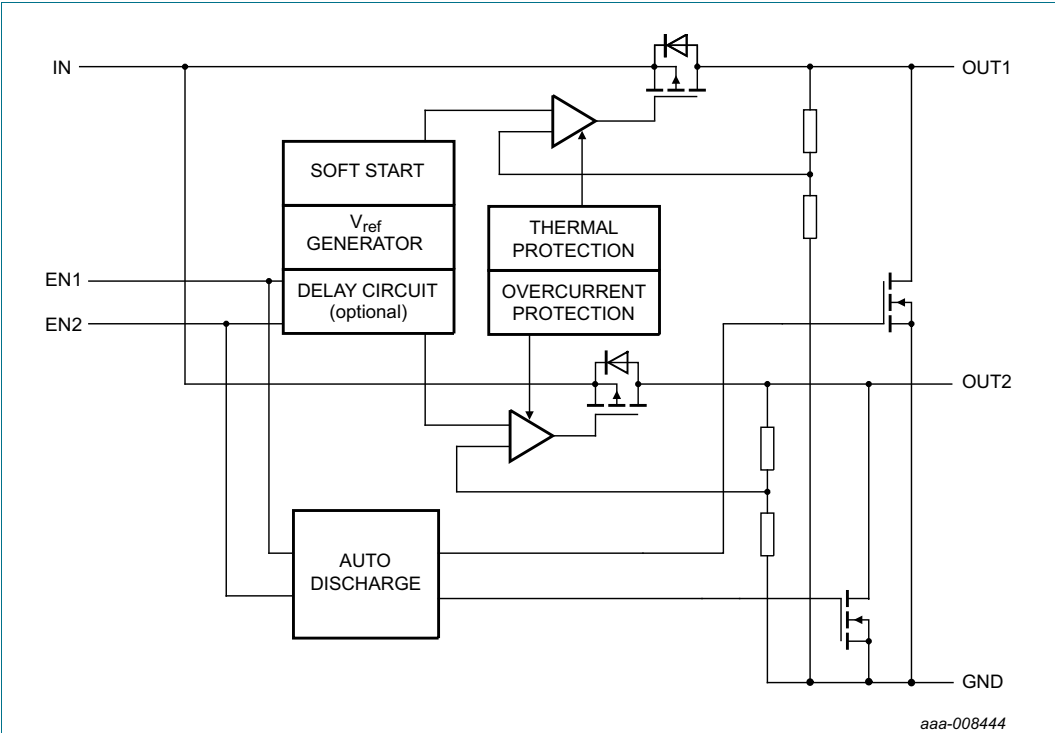


Fig 2. Block diagram dual LDO with auto discharge function (-PL version)

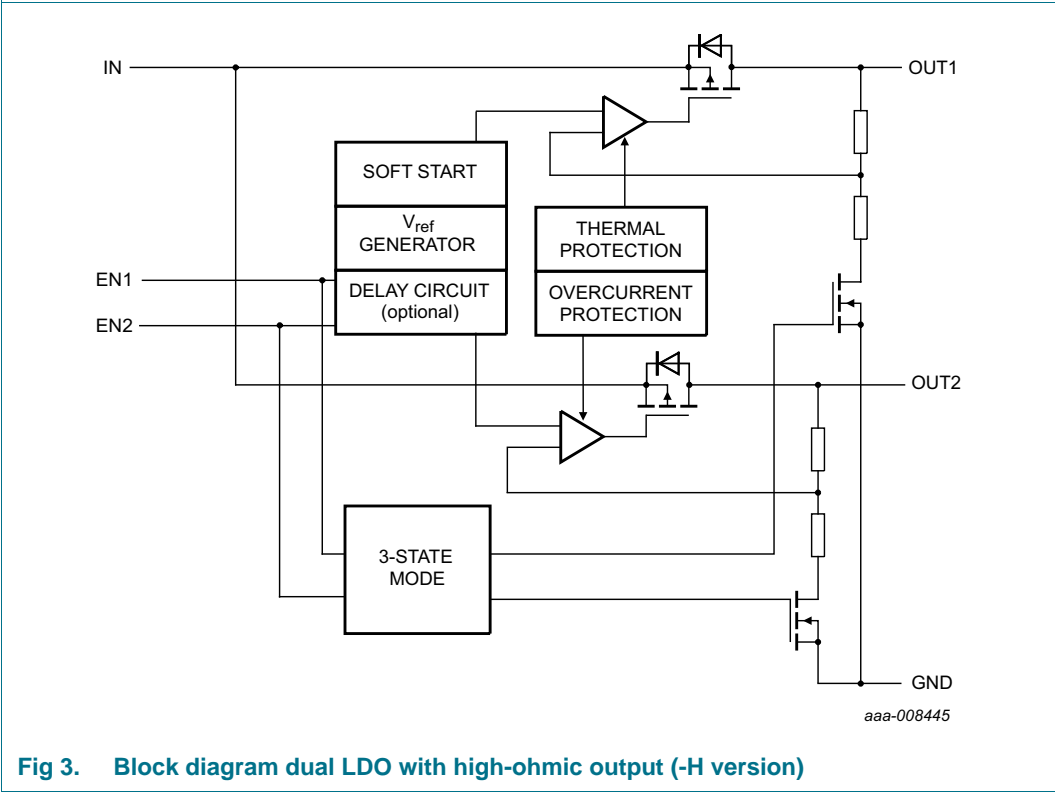


Fig 3. Block diagram dual LDO with high-ohmic output (-H version)

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol              | Parameter                       | Conditions               | Min   | Max  | Unit |
|---------------------|---------------------------------|--------------------------|-------|------|------|
| T <sub>stg</sub>    | storage temperature             |                          | −55   | +150 | °C   |
| T <sub>j</sub>      | junction temperature            |                          | −40   | +125 | °C   |
| T <sub>amb</sub>    | ambient temperature             |                          | −40   | +85  | °C   |
| P <sub>tot</sub>    | total power dissipation         |                          | [1] - | 1000 | mW   |
| V <sub>ESD</sub>    | electrostatic discharge voltage | human body model level 4 | [2] - | ±2   | kV   |
|                     |                                 | machine model class 3    | [3] - | ±200 | V    |
| Pin IN, EN1 and EN2 |                                 |                          |       |      |      |
| V <sub>I</sub>      | input voltage                   | 4 ms transient           | −0.5  | +6.0 | V    |
| V <sub>EN</sub>     | voltage on pin EN               | 4 ms transient           | −0.5  | +6.0 | V    |
| Pin OUT1 and OUT2   |                                 |                          |       |      |      |
| V <sub>O</sub>      | output voltage                  | 4 ms transient           | −0.5  | +6.0 | V    |
| I <sub>O</sub>      | output current                  |                          | 0     | 500  | mA   |

[1] The (absolute) maximum power dissipation depends on the junction temperature T<sub>j</sub>. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T<sub>amb</sub> = 25 °C and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to IEC 61340-3-1.

[3] According to JESD22-A115C.

## 6. Recommended operating conditions

**Table 6. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

| Symbol                   | Parameter                      | Conditions | Min | Max            | Unit |
|--------------------------|--------------------------------|------------|-----|----------------|------|
| T <sub>amb</sub>         | ambient temperature            |            | -40 | +85            | °C   |
| T <sub>j</sub>           | junction temperature           |            | -   | +125           | °C   |
| <b>Pin IN</b>            |                                |            |     |                |      |
| V <sub>I</sub>           | input voltage                  |            | 1.7 | 5.5            | V    |
| C <sub>ext(IN)</sub>     | external capacitance on pin IN | [1]        | 1.0 | -              | μF   |
| <b>Pin EN1 and EN2</b>   |                                |            |     |                |      |
| V <sub>EN</sub>          | voltage on pin EN              |            | 0   | V <sub>I</sub> | V    |
| <b>Pin OUT1 and OUT2</b> |                                |            |     |                |      |
| V <sub>O</sub>           | output voltage                 |            | 0   | 5.5            | V    |
| C <sub>L(ext)</sub>      | external load capacitance      | [1]        | 1.0 | -              | μF   |

[1] See [Section 9.1 "Input and output capacitor values"](#).

## 7. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions | Typ        | Unit |
|---------------|---|------------|------------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient |            | [1][2] 100 | K/W  |

- [1] The overall  $R_{th(j-a)}$  can vary depending on the board layout. To minimize the effective  $R_{th(j-a)}$ , all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.
- [2] Use the measurement data given for a rough estimation of the  $R_{th(j-a)}$  in your application. The actual  $R_{th(j-a)}$  value can vary in applications using different layer stacks and layouts.

## 8. Characteristics

**Table 8. Electrical characteristics**

At recommended input voltages and  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

| Symbol                                    | Parameter   | Conditions  | Min   | Typ    | Max    | Unit |
|---|---|---|-------|--------|--------|------|
| <b>Output voltage (pin OUT1 and OUT2)</b> |   |   |       |        |        |      |
| $V_{do}$                                  | dropout voltage                                       | $I_O = 300\text{ mA}$ ; $V_{IN} \leq V_{O(nom)}$                            | -     | 240    | 400    | mV   |
| $\Delta V_O$                              | output voltage variation                              | $V_O \geq 1.5\text{ V}$ ; $I_O = 1\text{ mA}$                               |       |        |        |      |
|   |   | $T_{amb} = +25\text{ }^{\circ}\text{C}$                                     | -2    | -      | +2     | %    |
|   |   | $-30\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$ | -3    | -      | +3     | %    |
|   |   | $V_O < 1.5\text{ V}$ ; $I_O = 1\text{ mA}$                                  |       |        |        |      |
|   |   | $T_{amb} = +25\text{ }^{\circ}\text{C}$                                     | -3    | -      | +3     | %    |
|   |   | $-30\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$ | -4    | -      | +4     | %    |
| <b>Line regulation error</b>              |   |   |       |        |        |      |
| $\Delta V_O / (V_O \times \Delta V_I)$    | relative output voltage variation with input voltage  | $V_I = (V_{O(nom)} + 1\text{ V})$ to $5.5\text{ V}$ ; $I_O = 1\text{ mA}$   | -0.1  | -      | +0.1   | %/V  |
| $\Delta V_O / V_O$                        | relative output voltage variation                     | $V_I = (V_{O(nom)} + 1\text{ V})$ to $5.5\text{ V}$ ; $I_O = 1\text{ mA}$   | -0.33 | -      | +0.33  | %    |
| <b>Load regulation error</b>              |   |   |       |        |        |      |
| $\Delta V_O / (V_O \times \Delta I_O)$    | relative output voltage variation with output current | $V_I = V_{O(nom)} + 1\text{ V}$ ; $1\text{ mA} \leq I_O \leq 300\text{ mA}$ | -     | 0.0025 | 0.0065 | %/mA |
| $\Delta V_O / V_O$                        | relative output voltage variation                     | $V_I = V_{O(nom)} + 1\text{ V}$   | -     | -      | 2      | %    |

**Table 8. Electrical characteristics ...continued**

At recommended input voltages and  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

| Symbol                                     | Parameter                       | Conditions   | Min                   | Typ | Max | Unit |
|--|---------------------------------|--|-----------------------|-----|-----|------|
| Output current (pin OUT1 and OUT2)         |                                 |  |                       |     |     |      |
| I <sub>O</sub>                             | output current                  |  | 300                   | -   | -   | mA   |
| I <sub>act(fold)</sub>                     | foldback activation current     | V <sub>O</sub> = 0.9 × V <sub>O(nom)</sub>   | -                     | 750 | -   | mA   |
| I <sub>sc</sub>                            | short-circuit current           | V <sub>O</sub> = 0 V   | -                     | 100 | -   | mA   |
| I <sub>q</sub>                             | quiescent current               | (EN1 or EN2) = HIGH;<br>I <sub>O</sub> = 0 mA at OUT1 and OUT2;<br>V <sub>I</sub> = V <sub>O(nom)</sub> + 1 V                  | -                     | 30  | -   | μA   |
|  |                                 | (EN1 and EN2) = HIGH;<br>I <sub>O</sub> = 0 mA at OUT1 and OUT2;<br>V <sub>I</sub> = V <sub>O(nom)</sub> + 1 V                 | -                     | 58  | 75  | μA   |
|  |                                 | (EN1 or EN2) = HIGH;<br>1 mA ≤ I <sub>O</sub> ≤ 300 mA at OUT1 and OUT2; V <sub>I</sub> = V <sub>O(nom)</sub> + 1 V            | -                     | 400 | -   | μA   |
|  |                                 | (EN1 and EN2) = LOW  | -                     | -   | 1.0 | μA   |
| Ripple rejection and output noise          |                                 |  |                       |     |     |      |
| PSRR                                       | power supply rejection ratio    | V <sub>I</sub> = V <sub>O(nom)</sub> + 1 V; I <sub>O</sub> = 50 mA;<br>f <sub>ripple</sub> = 1 kHz; C <sub>L(ext)</sub> = 1 μF | -                     | 80  | -   | dB   |
| V <sub>n(o)(RMS)</sub>                     | RMS output noise voltage        | bandwidth = 10 Hz to 100 kHz;<br>C <sub>L(ext)</sub> = 1 μF; V <sub>O</sub> = 1.8 V  | -                     | 70  | -   | μV   |
| Enable input and timing (pin EN1 and EN2)  |                                 |  |                       |     |     |      |
| V <sub>IL</sub>                            | LOW-level input voltage         |  | 0                     | -   | 0.4 | V    |
| V <sub>IH</sub>                            | HIGH-level input voltage        |  | 1.1                   | -   | 5.5 | V    |
| I <sub>en</sub>                            | enable current                  | -H version   | -                     | 250 | -   | nA   |
|  |                                 | -PL version; V <sub>EN</sub> = 1.8 V   | -                     | 12  | -   | μA   |
| R <sub>pd</sub>                            | pull-down resistance            | -PL version  | 100                   | 150 | 200 | kΩ   |
| t <sub>startup(reg)</sub>                  | regulator start-up time         | V <sub>I</sub> = 5.5 V; V <sub>O</sub> = 0.95 × V <sub>O(nom)</sub> ;<br>I <sub>O</sub> = 300 mA; C <sub>L(ext)</sub> = 1 μF   | -                     | 110 | 200 | μs   |
| Automatic discharge function (-PL version) |                                 |  |                       |     |     |      |
| R <sub>pd</sub>                            | pull-down resistance            |  | -                     | 100 | -   | Ω    |
| t <sub>sd(reg)</sub>                       | regulator shutdown time         | V <sub>I</sub> = 5.5 V; C <sub>L(ext)</sub> = 1 μF; I <sub>O</sub> = 0 A;<br>V <sub>O</sub> = 0.1 × V <sub>O(nom)</sub>        | <a href="#">[1]</a> - | 300 | -   | μs   |
| Thermal protection                         |                                 |  |                       |     |     |      |
| T <sub>sd</sub>                            | shutdown temperature            |  | -                     | 160 | -   | °C   |
| T <sub>sd(hys)</sub>                       | shutdown temperature hysteresis |  | <a href="#">[1]</a> - | 20  | -   | K    |

[1] After  $T_{sd}$  was reached and after the device was disabled, the junction temperature must decrease by  $T_{sd(hys)}$  to enable the device.

9. Application information

9.1 Input and output capacitor values

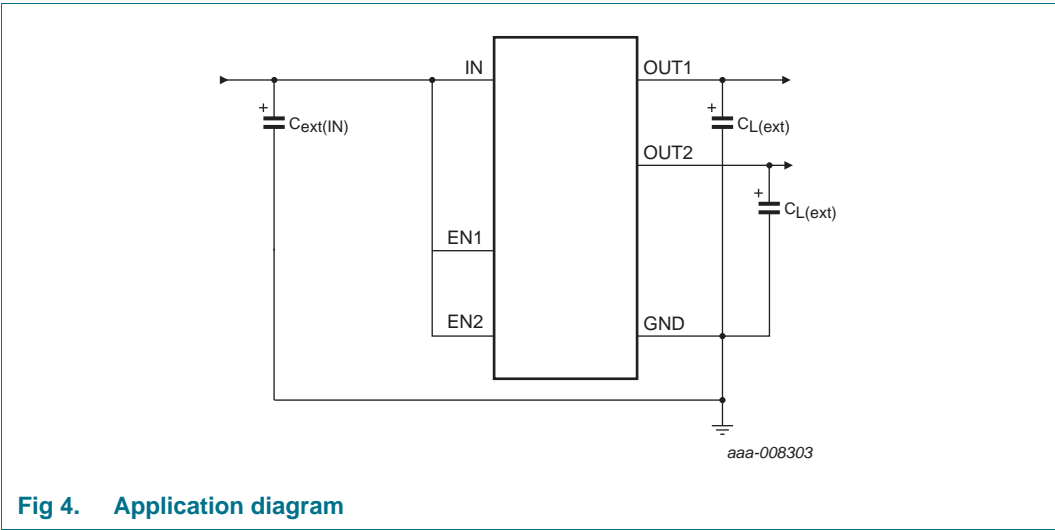
The devices require external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. These capacitors should not under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ( $t_{sd(reg)}$ ) of the devices.

Table 9. External load capacitor

| Symbol        | Parameter                      | Conditions | Min | Typ | Max | Unit      |
|---------------|--------------------------------|------------|-----|-----|-----|-----------|
| $C_{ext(IN)}$ | external capacitance on pin IN |            | 0.7 | 1.0 | -   | $\mu F$   |
| $C_{L(ext)}$  | external load capacitance      | [1]        | 0.7 | 1.0 | -   | $\mu F$   |
| ESR           | equivalent series resistance   |            | 5   | -   | 500 | $m\Omega$ |

[1] The minimum value of capacitance for stability and correct operation is 0.7  $\mu F$ . The capacitor tolerance should be  $\pm 30\%$  or better over the temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure that this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full device temperature specification of  $-40\text{ }^{\circ}C$  to  $+125\text{ }^{\circ}C$ .



10. Test information

10.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications



## 11. Package outline

WLCSP6: wafer level chip-size package; 6 bumps (2 x 3)

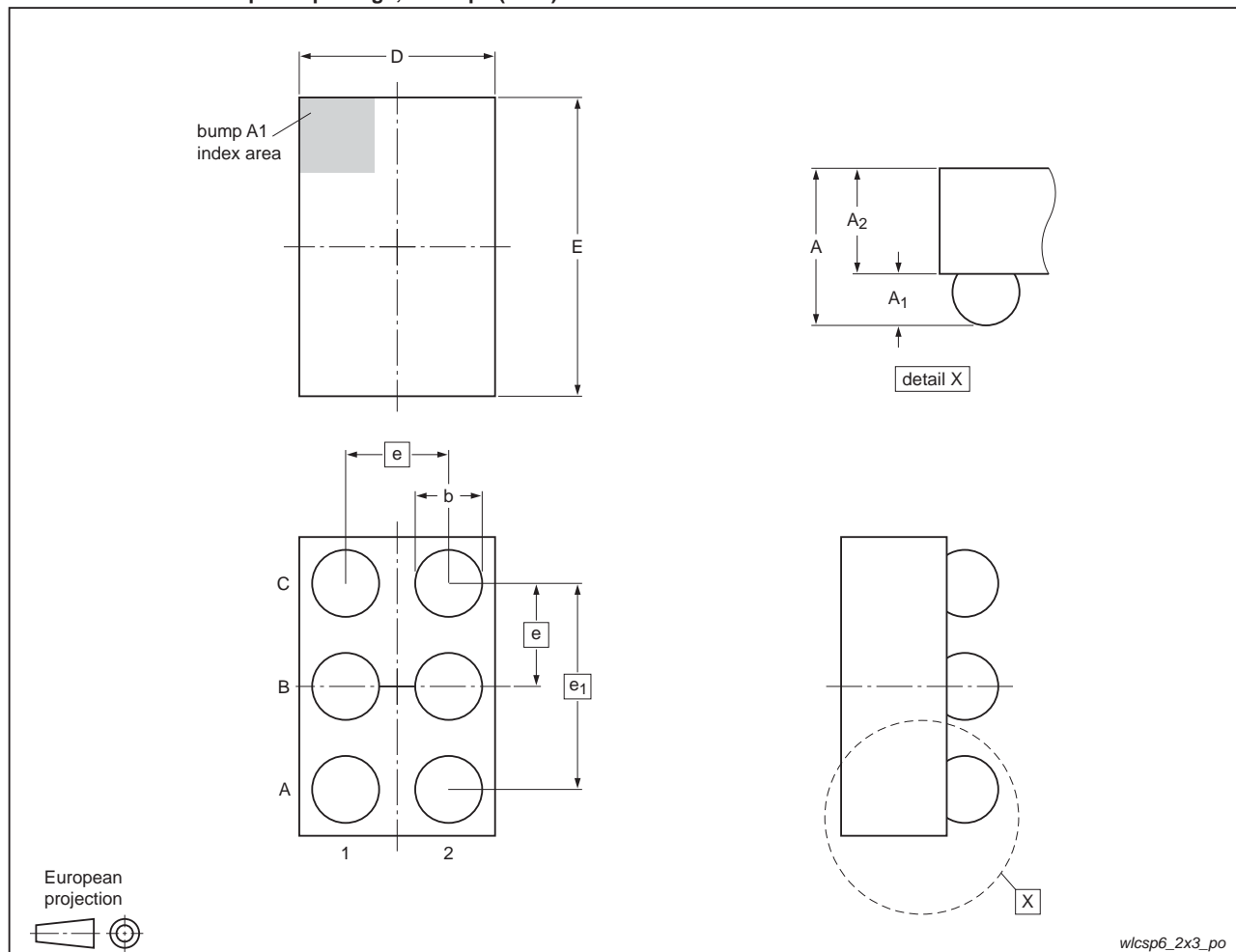


Fig 5. Package outline WLCSP6

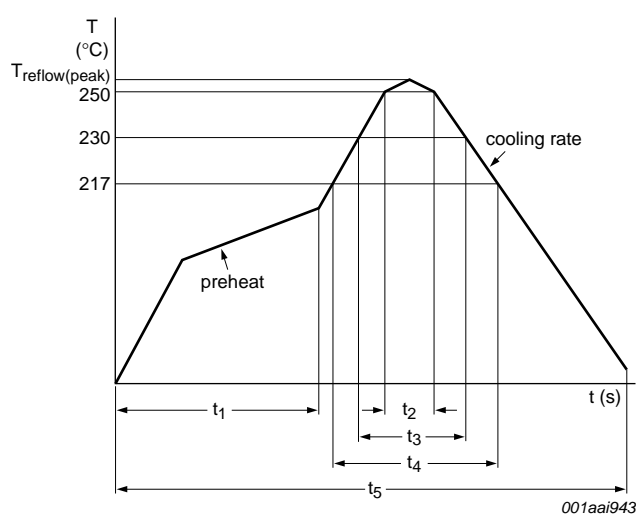
Table 10. Dimensions of LD6938 series in WLCSP6 (Figure 5)

| Symbol         | Min   | Typ   | Max   | Unit |
|----------------|-------|-------|-------|------|
| A              | 0.440 | 0.470 | 0.500 | mm   |
| A <sub>1</sub> | 0.180 | 0.200 | 0.220 | mm   |
| A <sub>2</sub> | 0.260 | 0.270 | 0.280 | mm   |
| b              | 0.210 | 0.260 | 0.310 | mm   |
| D              | 0.710 | 0.760 | 0.810 | mm   |
| E              | 1.110 | 1.160 | 1.210 | mm   |
| e              | -     | 0.400 | -     | mm   |
| e <sub>1</sub> | -     | 0.800 | -     | mm   |

## 12. PCB assembly guidelines for Pb-free soldering

Table 11. Assembly recommendations

| Parameter               | Value or specification                 |
|-------------------------|--|
| Solder screen thickness | 100 µm (0.004 inch)                    |
| Solder paste: Pb-free   | SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %) |
| Solder to flux ratio    | 50 : 50                                |
| Solder reflow profile   | see <a href="#">Figure 6</a>           |

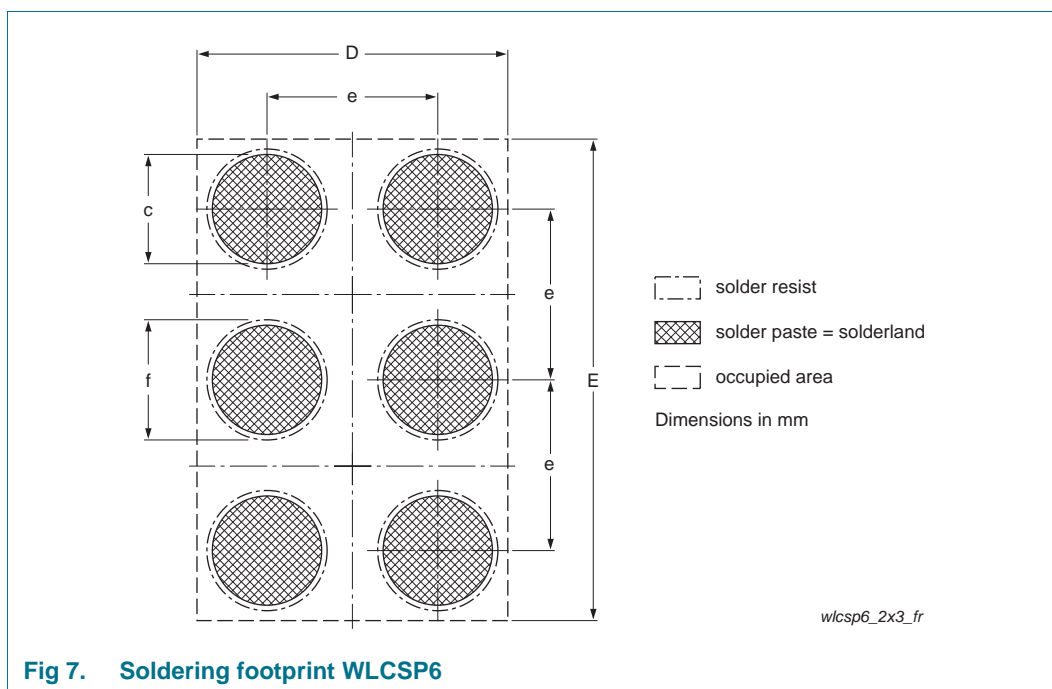


The device can withstand at least three reflows at this profile.

Fig 6. Pb-free solder reflow profile

Table 12. Characteristics

| Symbol                    | Parameter                     | Conditions                  | Min | Typ | Max | Unit |
|---------------------------|-------------------------------|-----------------------------|-----|-----|-----|------|
| $T_{\text{reflow(peak)}}$ | peak reflow temperature       |                             | 230 | -   | 260 | °C   |
| $t_1$                     | time 1                        | soak time                   | 60  | -   | 180 | s    |
| $t_2$                     | time 2                        | time during $T \geq 250$ °C | -   | -   | 30  | s    |
| $t_3$                     | time 3                        | time during $T \geq 230$ °C | 10  | -   | 50  | s    |
| $t_4$                     | time 4                        | time during $T > 217$ °C    | 30  | -   | 150 | s    |
| $t_5$                     | time 5                        |                             | -   | -   | 540 | s    |
| $dT/dt$                   | rate of change of temperature | cooling rate                | -   | -   | -6  | °C/s |
|                           |                               | preheat                     | 2.5 | -   | 4.0 | °C/s |



**Fig 7. Soldering footprint WLCSP6**

**Table 13. Dimensions of soldering footprint WLCSP6 (Figure 7)**

| Symbol | Min  | Typ   | Max  | Unit |
|--------|------|-------|------|------|
| c      | -    | 0.25  | -    | mm   |
| D      | 0.71 | 0.76  | 0.81 | mm   |
| E      | 1.11 | 1.16  | 1.21 | mm   |
| e      | -    | 0.4   | -    | mm   |
| f      | -    | 0.325 | -    | mm   |

## 13. Revision history

Table 14. Revision history

| Document ID    | Release date | Data sheet status    | Change notice | Supersedes |
|----------------|--------------|----------------------|---------------|------------|
| LD6938_SER v.1 | 20130711     | Objective data sheet | -             | -          |

## 14. Legal information

### 14.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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