

NVT2003/04/06

Bidirectional voltage-level translator for open-drain and push-pull applications

Rev. 4 — 7 September 2012

Product data sheet

1. General description

The NVT2003/04/06 is a family of bidirectional voltage level translators operational from 1.0 V to 3.6 V ($V_{\text{ref(A)}}$) and 1.8 V to 5.5 V ($V_{\text{ref(B)}}$), which allow bidirectional voltage translations between 1.0 V and 5 V without the need for a direction pin in open-drain or push-pull applications. Bit widths ranging from 3-bit to 6-bit are offered for level translation application with transmission speeds < 33 MHz for an open-drain system with a 50 pF capacitance and a pull-up of 197 Ω .

When the An or Bn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the An and Bn ports. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by VREFA. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{\text{pu(D)}}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

When EN is HIGH, the translator switch is on, and the An I/O are connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{\text{ref(B)}}$. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

2. Features and benefits

- Provides bidirectional voltage translation with no direction pin
- Less than 1.5 ns maximum propagation delay
- Allows voltage level translation between:
 - ◆ 1.0 V $V_{\text{ref(A)}}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{\text{ref(B)}}$
 - ◆ 1.2 V $V_{\text{ref(A)}}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{\text{ref(B)}}$
 - ◆ 1.8 V $V_{\text{ref(A)}}$ and 3.3 V or 5 V $V_{\text{ref(B)}}$
 - ◆ 2.5 V $V_{\text{ref(A)}}$ and 5 V $V_{\text{ref(B)}}$
 - ◆ 3.3 V $V_{\text{ref(A)}}$ and 5 V $V_{\text{ref(B)}}$



- Low $3.5\ \Omega$ ON-state connection between input and output ports provides less signal distortion
- 5 V tolerant I/O ports to support mixed-mode signal operation
- High-impedance An and Bn pins for EN = LOW
- Lock-up free operation
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 3.5 kV HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Packages offered: TSSOP10, HXSON12, DHVQFN16, HVQFN16, TSSOP16

3. Ordering information

Table 1. Ordering information

$T_{amb} = -40\ ^\circ\text{C}$ to $+85\ ^\circ\text{C}$.

Type number	Topside mark	Number of bits	Package		
			Name	Description	Version
NVT2003DP	N2003	3	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
NVT2004TL	N04	4	HXSON12	plastic, thermal enhanced extremely thin small outline package; no leads; 12 terminals; body $1.35 \times 2.5 \times 0.5$ mm	SOT973-2
NVT2006BQ	N2006	6	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm	SOT763-1
NVT2006BS	N06	6	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body $3 \times 3 \times 0.85$ mm	SOT758-1
NVT2006PW	NVT2006	6	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

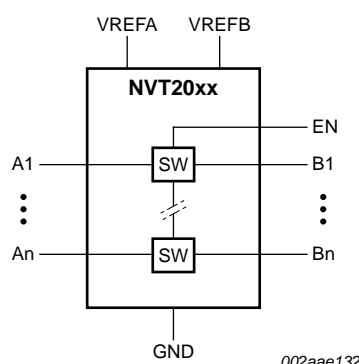
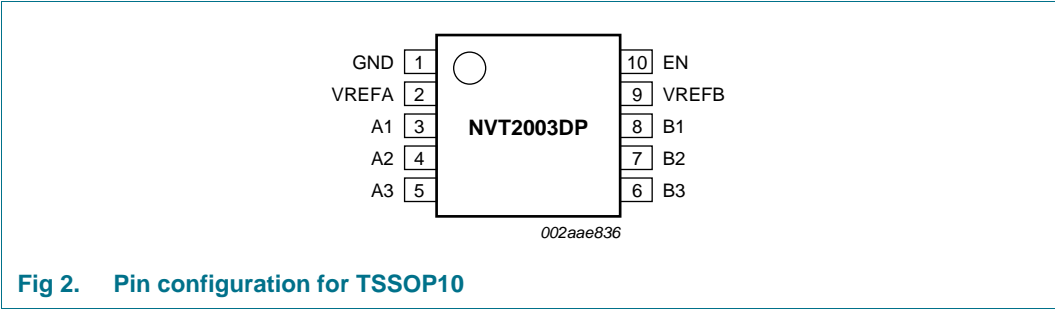


Fig 1. Logic diagram of NVT2003/04/06 (positive logic)

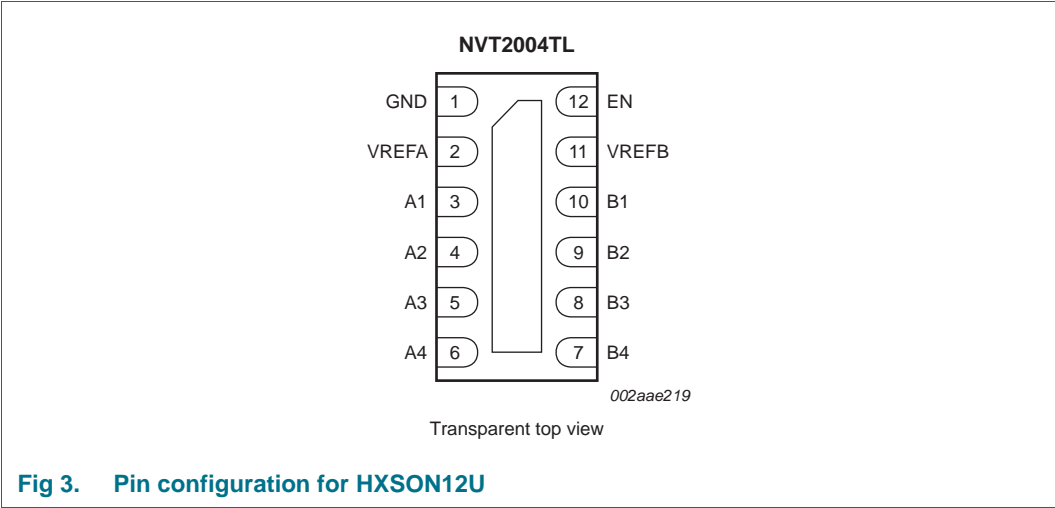
5. Pinning information

5.1 Pinning

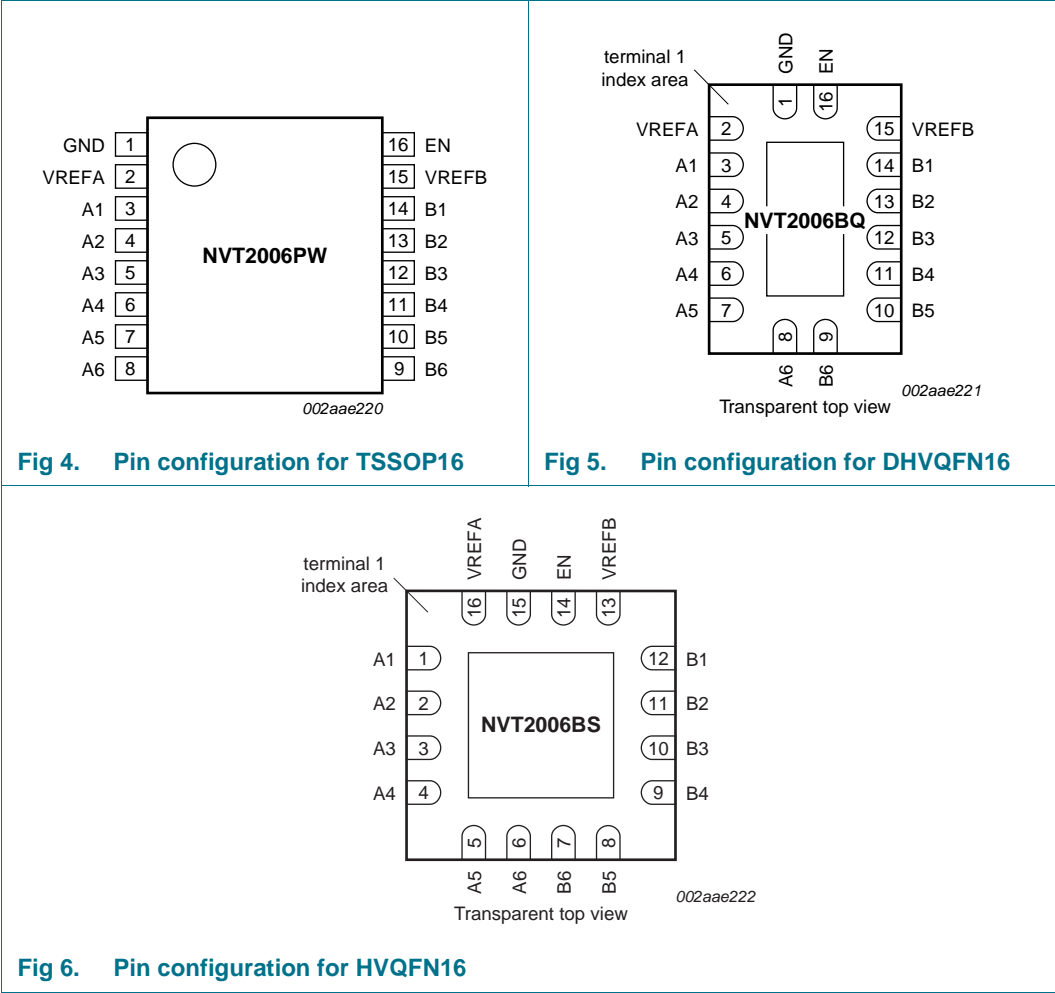
5.1.1 3-bit in TSSOP10 package



5.1.2 4-bit in HXSON12 package



5.1.3 6-bit in TSSOP16, DHVQFN16 and HVQFN16 packages



5.2 Pin description

Table 2. Pin description

Symbol	Pin				Description
	NVT2003DP ^[1]	NVT2004TL ^[2]	NVT2006BQ, NVT2006PW ^[3]	NVT2006BS ^[3]	
GND	1	1	1	15	ground (0 V)
VREFA	2	2	2	16	low-voltage side reference supply voltage for An
A1	3	3	3	1	low-voltage side; connect to VREFA through a pull-up resistor
A2	4	4	4	2	
A3	5	5	5	3	
A4	-	6	6	4	
A5	-	-	7	5	
A6	-	-	8	6	
B1	8	10	14	12	high-voltage side; connect to VREFB through a pull-up resistor
B2	7	9	13	11	
B3	6	8	12	10	
B4	-	7	11	9	
B5	-	-	10	8	
B6	-	-	9	7	
VREFB	9	11	15	13	high-voltage side reference supply voltage for Bn
EN	10	12	16	14	switch enable input; connect to VREFB and pull-up through a high resistor

[1] 3-bit NVT2003 available in TSSOP10 package.

[2] 4-bit NVT2004 available in HXSON12 package.

[3] 6-bit NVT2006 available in TSSOP16, DHVQFN16, HVQFN16 packages.

6. Functional description

Refer to Figure 1 “Logic diagram of NVT2003/04/06 (positive logic)”.

6.1 Function table

Table 3. Function selection (example)

H = HIGH level; L = LOW level.

Input EN ⁽¹⁾	Function
H	$A_n = B_n$
L	disconnect

[1] EN is controlled by the $V_{\text{ref(B)}}$ logic levels and should be at least 1 V higher than $V_{\text{ref(A)}}$ for best translator operation.

7. Application design-in information

The NVT2003/04/06 can be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The NVT2003/04/06 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The NVT2003/04/06 can also be used in applications where a push-pull driver is connected to the data I/Os.

7.1 Enable and disable

The NVT20xx has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state.

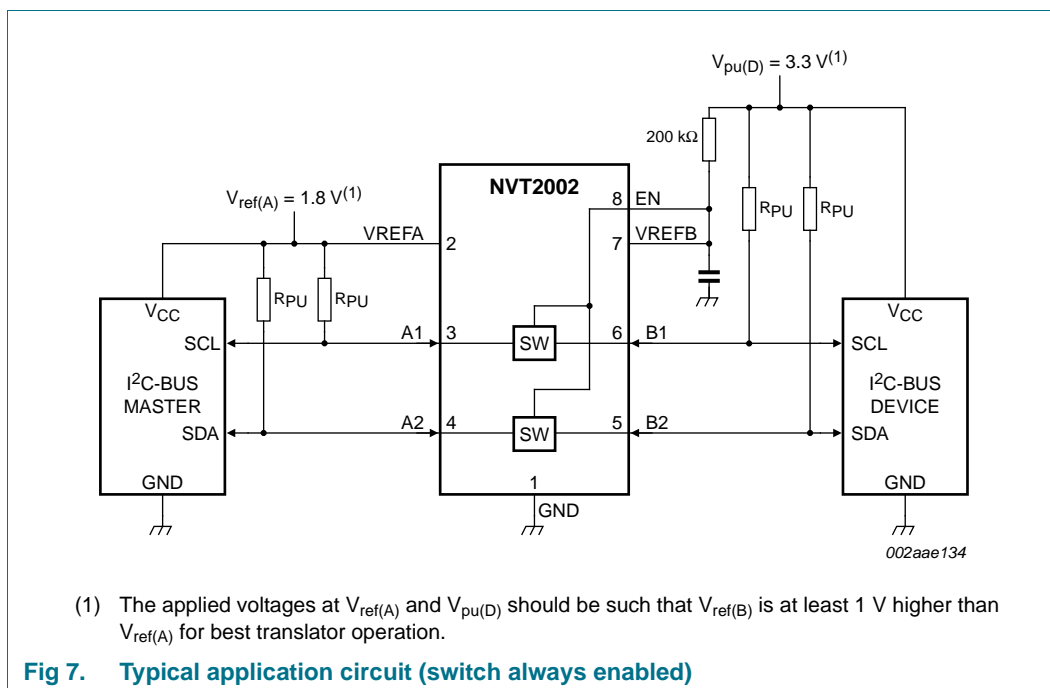
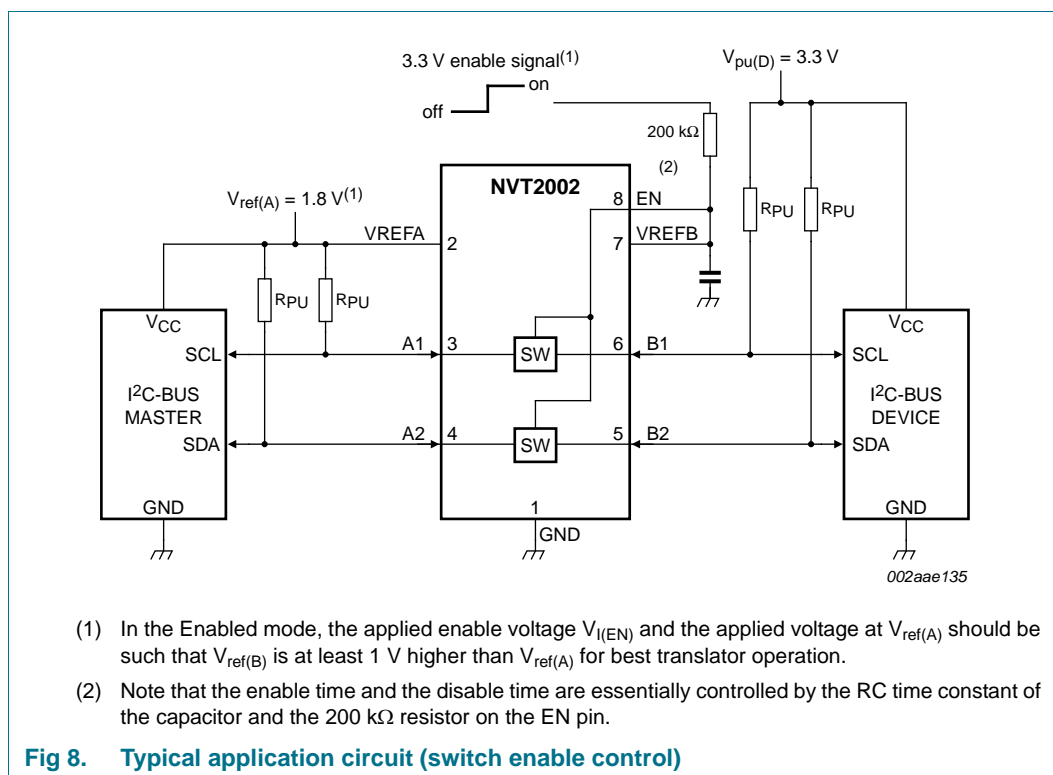


Table 4. Application operating conditionsRefer to [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$V_{\text{ref(B)}}$	reference voltage (B)		$V_{\text{ref(A)}} + 0.6$	2.1	5	V
$V_{\text{I(EN)}}$	input voltage on pin EN		$V_{\text{ref(A)}} + 0.6$	2.1	5	V
$V_{\text{ref(A)}}$	reference voltage (A)		0	1.5	4.4	V
$I_{\text{sw(pass)}}$	pass switch current		-	14	-	mA
I_{ref}	reference current	transistor	-	5	-	μA
T_{amb}	ambient temperature	operating in free-air	-40	-	+85	$^{\circ}\text{C}$

[1] All typical values are at $T_{\text{amb}} = 25^{\circ}\text{C}$.

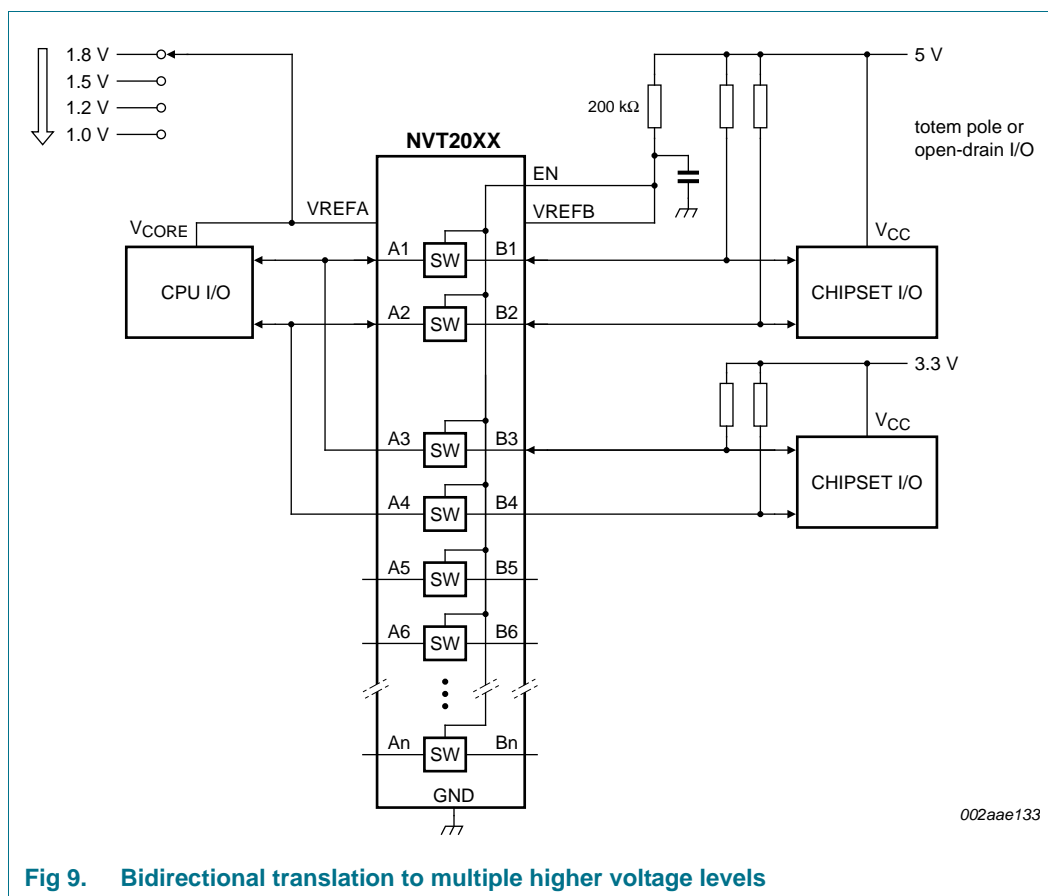


Fig 9. Bidirectional translation to multiple higher voltage levels

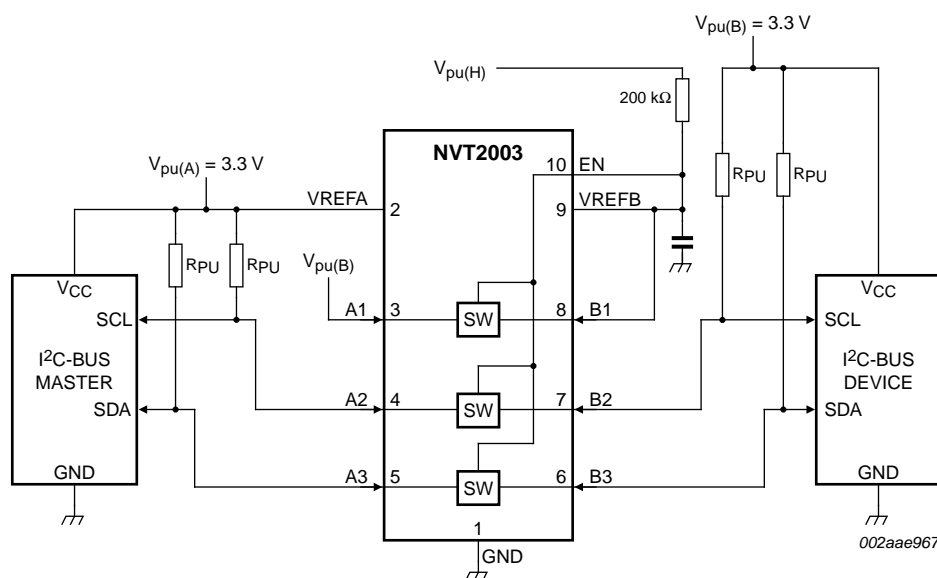
7.2 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200 k Ω). This allows VREFB to regulate the EN input. A filter capacitor on VREFB is recommended. The master output driver can be totem pole or open-drain (pull-up resistors may be required) and the slave device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to $V_{pu(D)}$). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{\text{ref(A)}}$) is connected to the processor core power supply voltage. When V_{REFB} is connected through a 200 k Ω resistor to a 3.3 V to 5.5 V $V_{\text{pu(D)}}$ power supply, and $V_{\text{ref(A)}}$ is set between 1.0 V and ($V_{\text{pu(D)}} - 1$ V), the output of each A_n has a maximum output voltage equal to V_{REFA} , and the output of each B_n has a maximum output voltage equal to $V_{\text{pu(D)}}$.

7.3 Bidirectional level shifting between two different power domains nominally at the same potential

The less obvious application for the NVT2003 is for level shifting between two different power domains that are nominally at the same potential, such as a 3.3 V system where the line crosses power supply domains that under normal operation would be at 3.3 V, but one could be at 3.0 V and the other at 3.6 V, or one could be experiencing a power failure while the other domain is trying to operate. One of the NVT2003 three channel transistors is used as a second reference transistor with its B side connected to a voltage supply that is at least 1 V (and preferably 1.5 V) above the maximum possible for either $V_{pu(A)}$ or $V_{pu(B)}$. Then if either pull-up voltage is at 0 V, the channels are disabled, and otherwise the channels are biased such that they turn OFF at the lower pull-up voltage, and if the two pull-up voltages are equal, the channel is biased such that it just turns OFF at the common pull-up voltage.



The applied enable voltage $V_{pu(H)}$ and the applied voltage at $V_{ref(A)}$ and $V_{ref(B)}$ should be such that $V_{ref(H)}$ is at least 1 V higher than $V_{ref(A)}$ and $V_{ref(B)}$ for best translator operation.

Fig 10. Bidirectional level shifting between two different power domains

7.4 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{pu(D)} - 0.35 \text{ V}}{0.015 \text{ A}}$$

[Table 5](#) summarizes resistor reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor values shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver

must be able to sink the total current from the resistors on both sides of the NVT20xx device at 0.175 V, although the 15 mA only applies to current flowing through the NVT20xx device.

Table 5. Pull-up resistor values

Calculated for $V_{OL} = 0.35$ V; assumes output driver $V_{OL} = 0.175$ V at stated current.

$V_{pu(D)}$	Pull-up resistor value (Ω)									
	64 mA		32 mA		15 mA		10 mA		3 mA	
	Nominal	+10 % ^[1]	Nominal	+10 % ^[1]	Nominal	+10 % ^[1]	Nominal	+10 % ^[1]	Nominal	+10 % ^[1]
5 V					310	341	465	512	1550	1705
3.3 V					197	217	295	325	983	1082
2.5 V					143	158	215	237	717	788
1.8 V					97	106	145	160	483	532
1.5 V					77	85	115	127	383	422
1.2 V					57	63	85	94	283	312

[1] +10 % to compensate for V_{CC} range and resistor tolerance.

7.4.1 Maximum frequency calculation

The maximum frequency is totally dependent upon the specifics of the application and the device can operate > 33 MHz. Basically, the NVT20xx behaves like a wire with the additional characteristics of transistor device physics and should be capable of performing at higher frequencies if used correctly.

Here are some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NVT20xx close to the processor.
- The trace length should have a time of flight less than half of the transition time to reduce ringing and reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher the drive strength (up to 15 mA), the higher the frequency the device can use.

In a 3.3 V to 1.8 V direction level shift, if the 3.3 V side is being driven by a totem pole type driver no pull-up resistor is needed on the 3.3 V side. The capacitance and line length of concern is on the 1.8 V side since it is driven through the ON resistance of the NVT20xx. If the line length on the 1.8 V side is long enough there can be a reflection at the chip/terminating end of the wire when the transition time is shorter than the time of flight of the wire because the NVT20xx looks like a high-impedance compared to the wire. If the wire is not too long and the lumped capacitance is not excessive the signal will only be slightly degraded by the series resistance added by passing through the NVT20xx. If the lumped capacitance is large the rise time will deteriorate, the fall time is much less affected and if the rise time is slowed down too much the duty cycle of the clock will be degraded and at some point the clock will no longer be useful. So the principle design consideration is to minimize the wire length and the capacitance on the 1.8 V side for the clock path. A pull-up resistor on the 1.8 V side can also be used to trade a slower fall time for a faster rise time and can also reduce the overshoot in some cases.

7.4.1.1 Example maximum frequency

Question — We need to make the PLL area of a new line card backwards compatible and need to convert one GTL signal to LVTTTL, invert it, and convert it back to GTL. The signal we want to convert is random in nature but will mostly be around 19 MHz with very long periods of inactivity where either a HIGH or LOW state will be maintained. The traces are 1 or 2 inches long with trace capacitance of about 2 pF per inch.

Answer — The frequency of the NVT20xx is limited by the capacitance of the part, the capacitance of the traces and the pull-up resistors used. The limiting case is probably the LOW-to-HIGH transition in the GTL to LVTTTL direction, and there the use of the lowest acceptable resistor values will minimize the rise time delay. Assuming 50 pF capacitance and 220 Ω resistance, the RC time constant is 11 ns (50 pF \times 220 Ω). With 19 MHz corresponding to 50 ns period the NVT20xx will support this application.

8. Limiting values

Table 6. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).
Over operating free-air temperature range.*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{ref(A)}}$	reference voltage (A)		−0.5	+6	V
$V_{\text{ref(B)}}$	reference voltage (B)		−0.5	+6	V
V_I	input voltage		−0.5 ^[1]	+6	V
$V_{I/O}$	voltage on an input/output pin		−0.5 ^[1]	+6	V
I_{ch}	channel current (DC)		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V	−50	-	mA
I_{OK}	output clamping current		^[2] −50	+50	mA
T_{stg}	storage temperature		−65	+150	°C

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

[2] Low duty cycle pulses, not DC because of heating.

9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	voltage on an input/output pin	An, Bn	0	5.5	V
$V_{\text{ref(A)}}$	reference voltage (A)	VREFA	^[1] 0	5.4	V
$V_{\text{ref(B)}}$	reference voltage (B)	VREFB	^[1] 0	5.5	V
$V_{I(\text{EN})}$	input voltage on pin EN		0	5.5	V
$I_{\text{sw(pass)}}$	pass switch current		-	64	mA
T_{amb}	ambient temperature	operating in free-air	−40	+85	°C

[1] $V_{\text{ref(A)}} \leq V_{\text{ref(B)}} - 1$ V for best results in level shifting applications.

10. Static characteristics

Table 8. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IK}	input clamping voltage	$I_I = -18\text{ mA}$; $V_{I(EN)} = 0\text{ V}$	-	-	-1.2	V
I_{IH}	HIGH-level input current	$V_I = 5\text{ V}$; $V_{I(EN)} = 0\text{ V}$	-	-	5	μA
$C_{i(EN)}$	input capacitance on pin EN	$V_I = 3\text{ V}$ or 0 V	-	12	-	pF
$C_{io(off)}$	off-state input/output capacitance	An, Bn; $V_O = 3\text{ V}$ or 0 V ; $V_{I(EN)} = 0\text{ V}$	-	5	7	pF
$C_{io(on)}$	on-state input/output capacitance	An, Bn; $V_O = 3\text{ V}$ or 0 V ; $V_{I(EN)} = 3\text{ V}$	-	11.5	13 ^[2]	pF
R_{on}	ON-state resistance	An, Bn; $V_I = 0\text{ V}$; $I_O = 64\text{ mA}$; $V_{I(EN)} = 4.5\text{ V}$	^{[3][4][5]} 1	2.4	5.0	Ω
		$V_I = 2.4\text{ V}$; $I_O = 15\text{ mA}$; $V_{I(EN)} = 4.5\text{ V}$	^{[3][4]} -	4.8	7.5	Ω

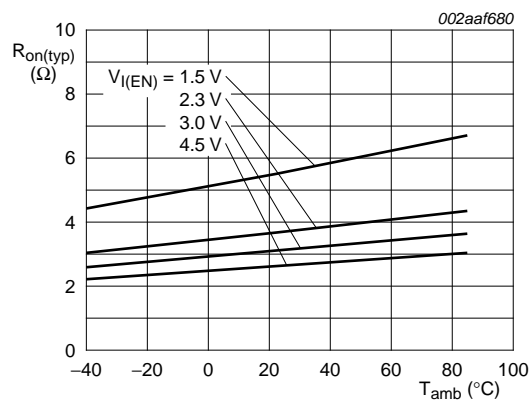
[1] All typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] Not production tested, maximum value based on characterization data of typical parts.

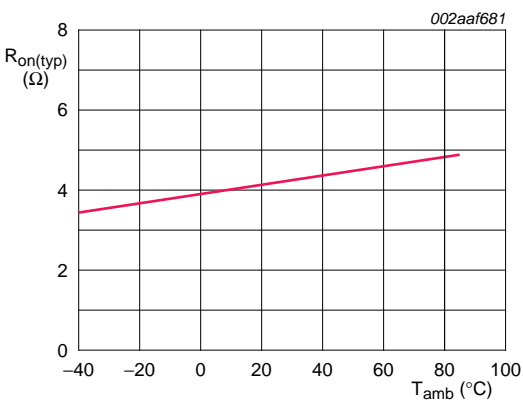
[3] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

[4] See curves in [Figure 11](#) for typical temperature and $V_{I(EN)}$ behavior.

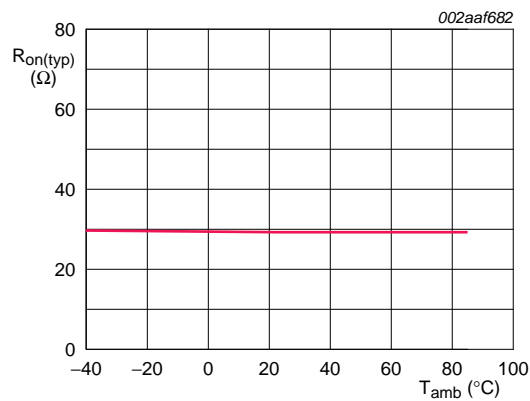
[5] Guaranteed by design.



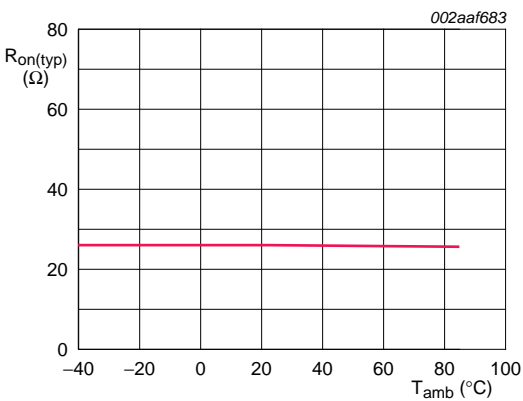
a. $I_O = 64\text{ mA}$; $V_I = 0\text{ V}$



b. $I_O = 15\text{ mA}$; $V_I = 2.4\text{ V}$; $V_{I(EN)} = 4.5\text{ V}$



c. $I_O = 15\text{ mA}$; $V_I = 2.4\text{ V}$; $V_{I(EN)} = 3.0\text{ V}$



d. $I_O = 15\text{ mA}$; $V_I = 1.7\text{ V}$; $V_{I(EN)} = 2.3\text{ V}$

Fig 11. NVT2006 typical ON-state resistance versus ambient temperature

11. Dynamic characteristics

11.1 Open-drain drivers

Table 9. Dynamic characteristics for open-drain drivers
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{I(EN)} = V_{ref(B)}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	from (input) Bn to (output) An	[1]	$R_{on} \times (C_L + C_{io(on)})$		ns
t_{PHL}	HIGH to LOW propagation delay	from (input) Bn to (output) An		$R_{on} \times (C_L + C_{io(on)})$		ns

[1] See graphs based on R_{on} typical and $C_{io(on)} + C_L = 50\text{ pF}$.

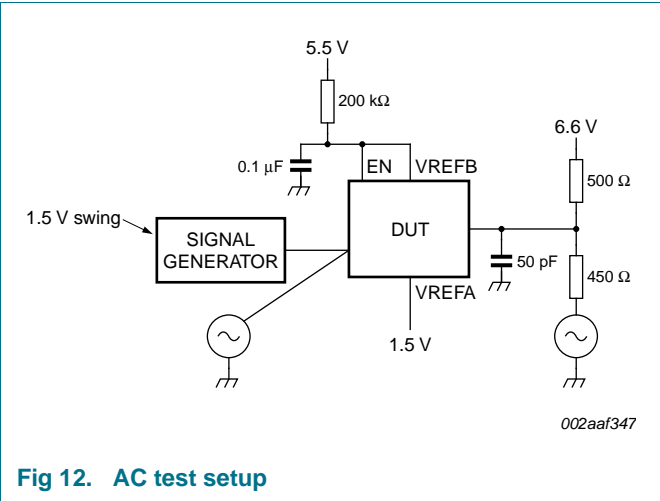


Fig 12. AC test setup

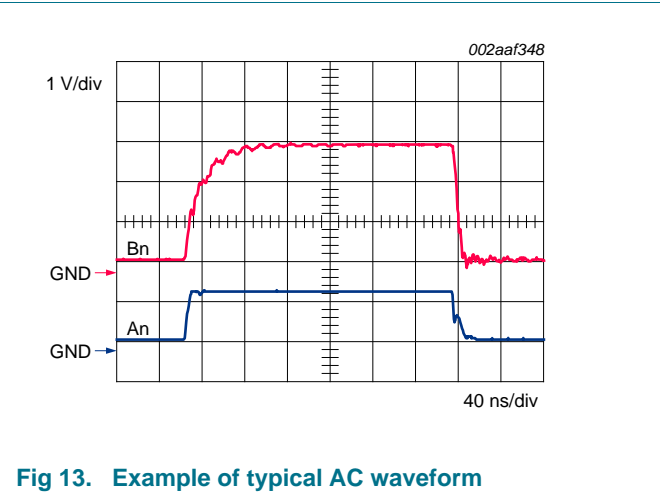
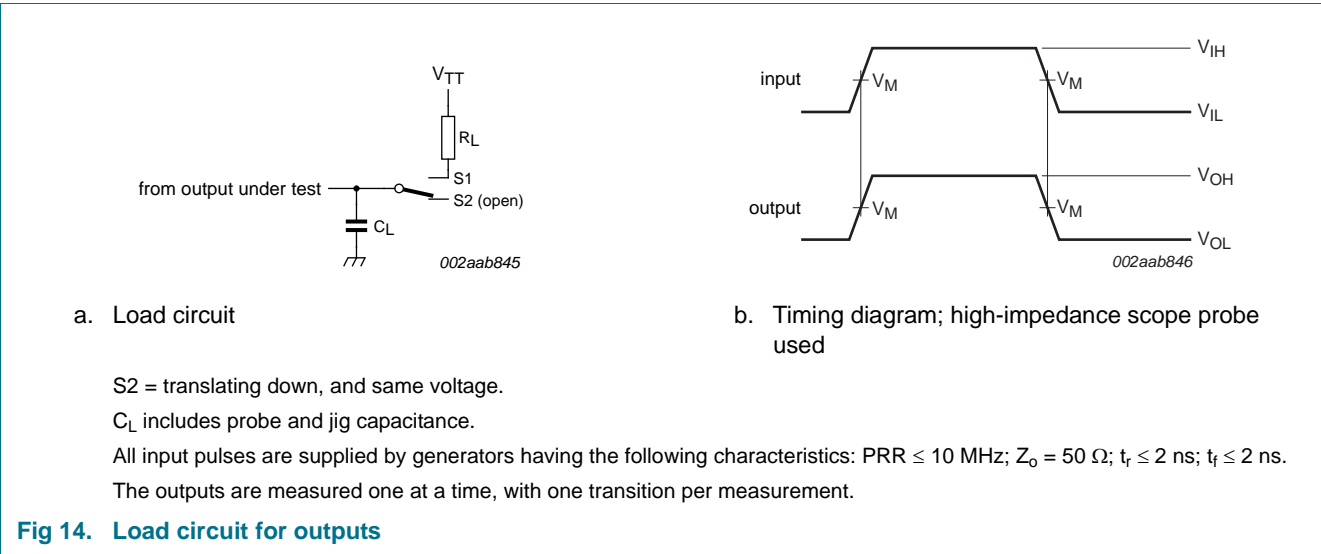


Fig 13. Example of typical AC waveform



12. Performance curves

t_{PLH} up-translation is typically dominated by the RC time constant, i.e.,
 $C_{L(tot)} \times R_{PU} = 50 \text{ pF} \times 197 \text{ } \Omega = 9.85 \text{ ns}$, but the $R_{on} \times C_{L(tot)} = 50 \text{ pF} \times 5 \text{ } \Omega = 0.250 \text{ ns}$.

t_{PHL} is typically dominated by the external pull-down driver + R_{on} , which is typically small compared to the t_{PLH} in an up-translation case.

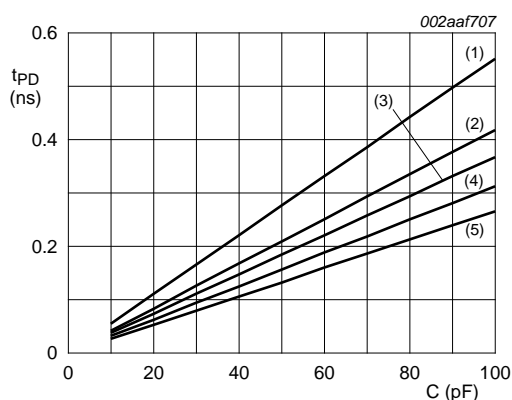
Enable/disable times are dominated by the RC time constant on the EN pin since the transistor turn off is on the order of ns, but the enable RC is on the order of ms.

Fall time is dominated by the external pull-down driver with only a slight R_{on} addition.

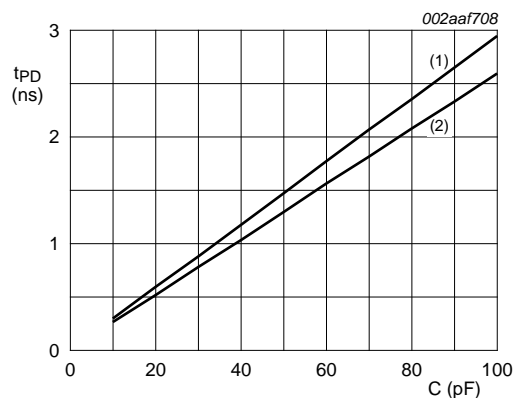
Rise time is dominated by the $R_{PU} \times C_L$.

Skew time within the part is virtually non-existent, dominated by the difference in bond wire lengths, which is typically small compared to the board-level routing differences.

Maximum data rate is dominated by the system capacitance and pull-up resistors.



- (1) $V_{I(EN)} = 1.5 \text{ V}$; $I_O = 64 \text{ mA}$; $V_I = 0 \text{ V}$.
- (2) $V_{I(EN)} = 4.5 \text{ V}$; $I_O = 15 \text{ mA}$; $V_I = 2.4 \text{ V}$.
- (3) $V_{I(EN)} = 2.3 \text{ V}$; $I_O = 64 \text{ mA}$; $V_I = 0 \text{ V}$.
- (4) $V_{I(EN)} = 3.0 \text{ V}$; $I_O = 64 \text{ mA}$; $V_I = 0 \text{ V}$.
- (5) $V_{I(EN)} = 4.5 \text{ V}$; $I_O = 64 \text{ mA}$; $V_I = 0 \text{ V}$.



- (1) $V_{I(EN)} = 3.0 \text{ V}$; $I_O = 15 \text{ mA}$; $V_I = 2.4 \text{ V}$.
- (2) $V_{I(EN)} = 2.3 \text{ V}$; $I_O = 15 \text{ mA}$; $V_I = 1.7 \text{ V}$.

Fig 15. NVT2006 typical capacitance versus propagation delay

13. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1

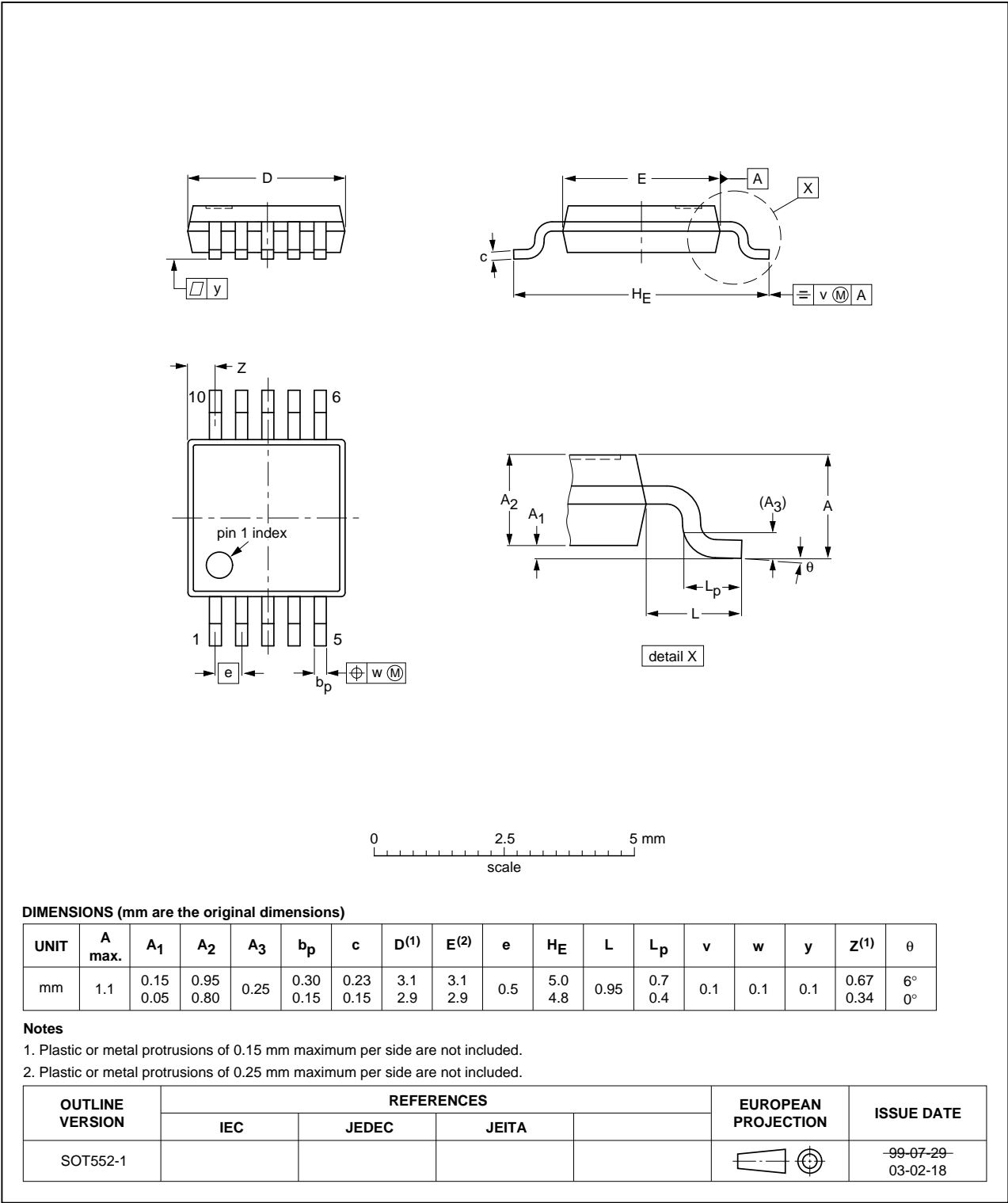


Fig 16. Package outline SOT552-1 (TSSOP10)

HXSON12: plastic, thermal enhanced extremely thin small outline package; no leads;
12 terminals; body 1.35 x 2.5 x 0.5 mm

SOT973-2

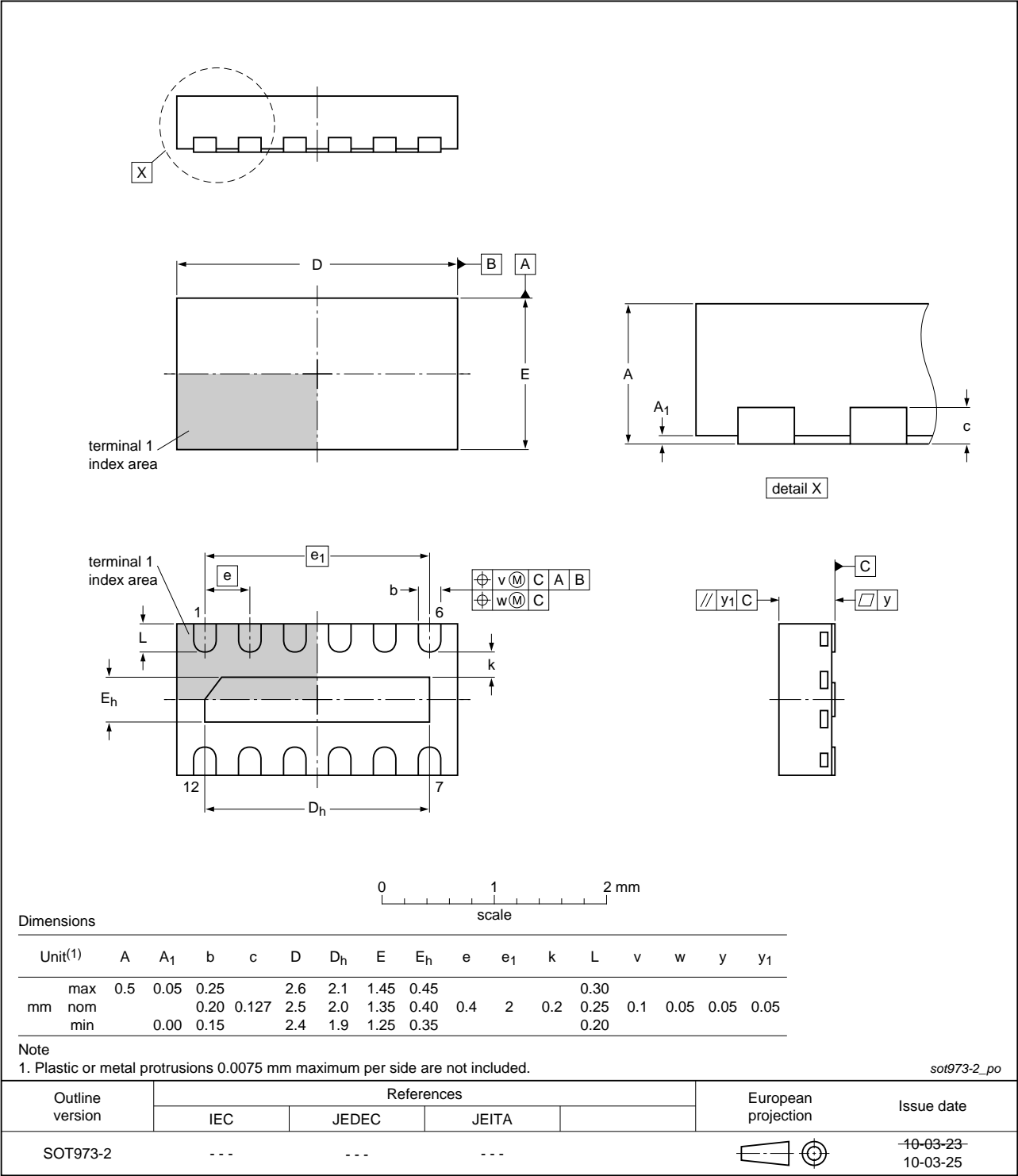


Fig 17. Package outline SOT973-2 (HXSON12)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

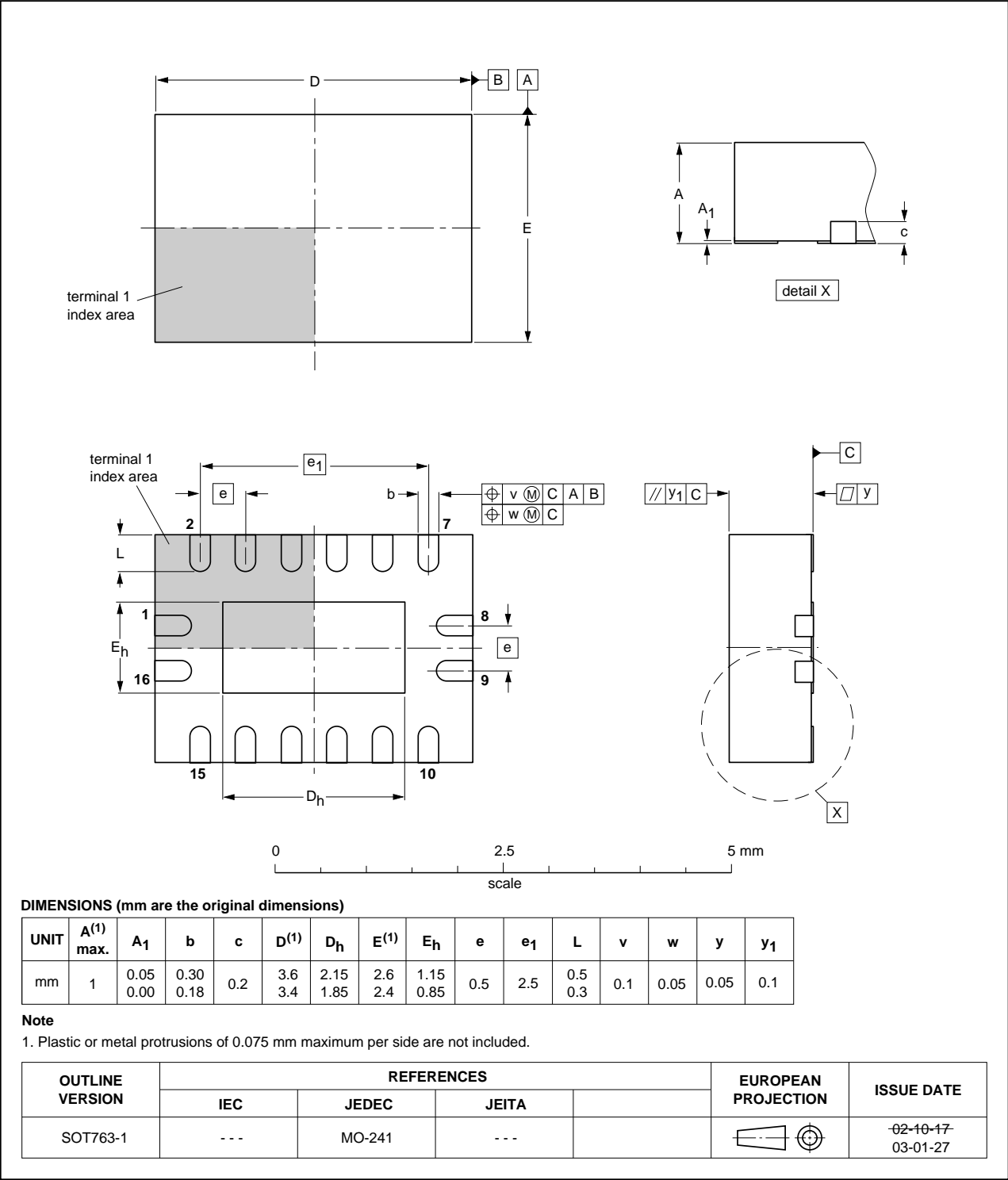


Fig 18. Package outline SOT763-1 (DHVQFN16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads;
16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

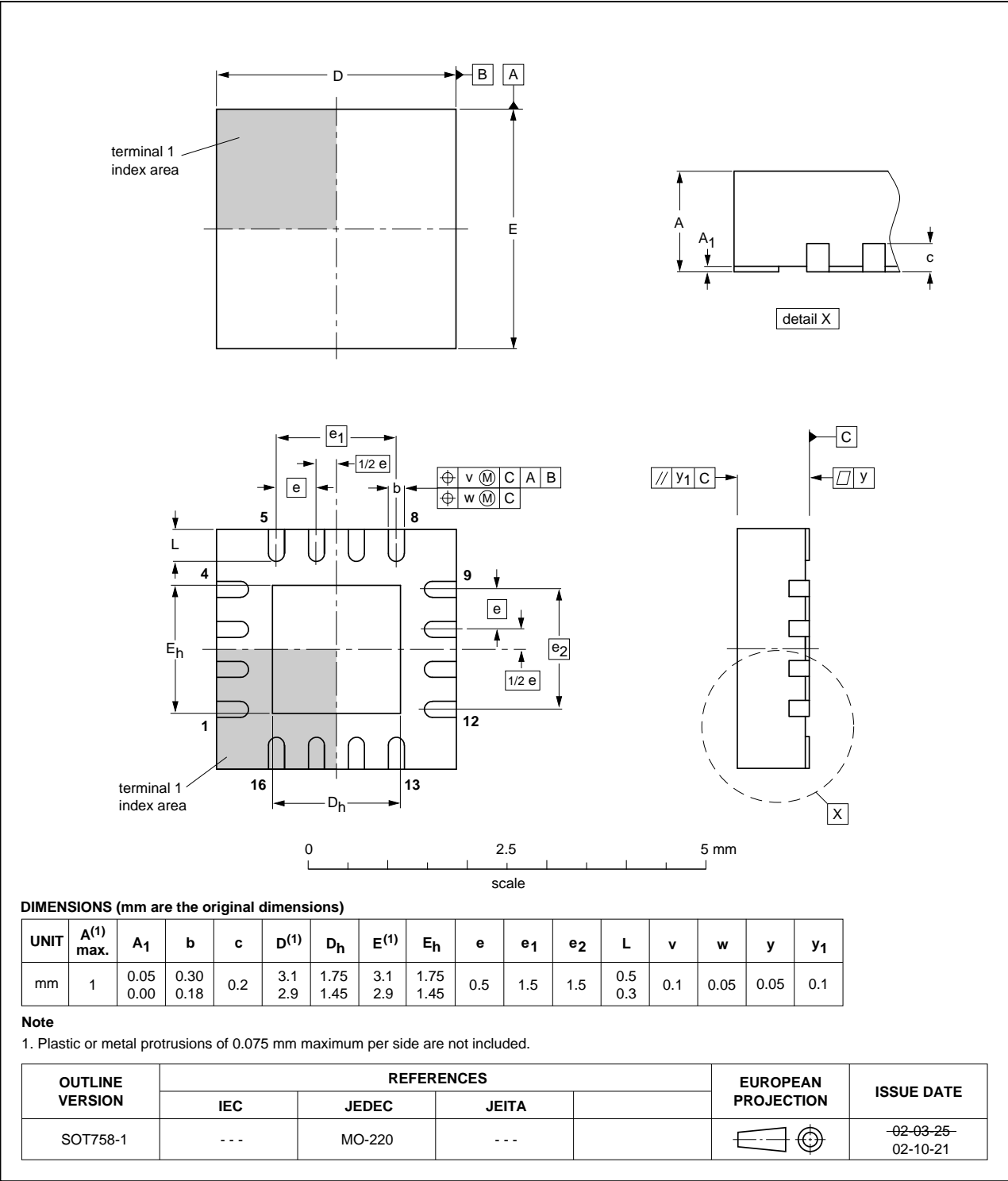


Fig 19. Package outline SOT758-1 (HVQFN16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

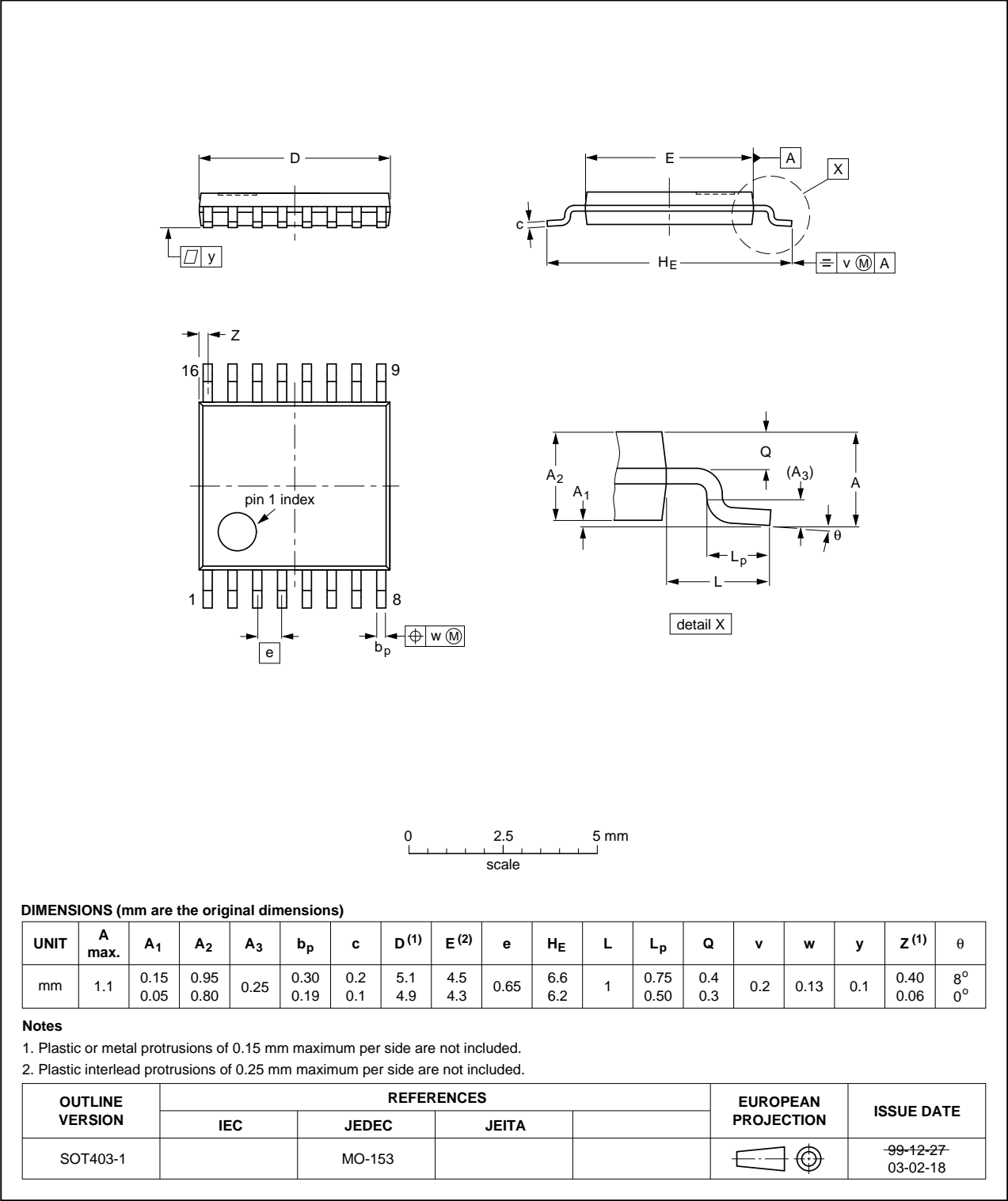


Fig 20. Package outline SOT403-1 (TSSOP16)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 21](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

Table 10. SnPb eutectic process (from J-STD-020C)

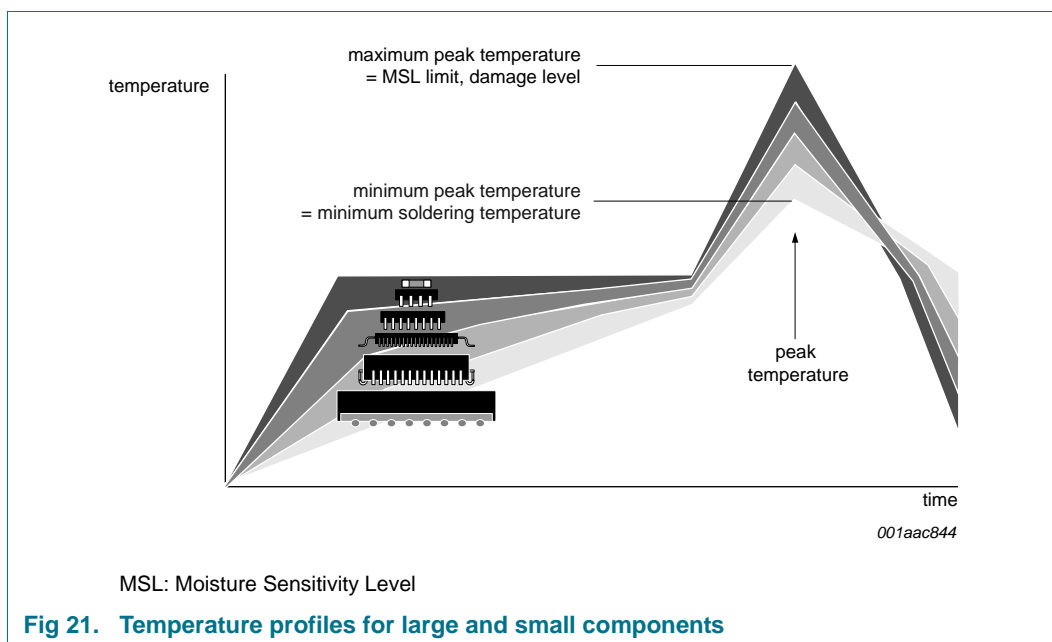
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 21](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT2003_04_06 v.4	20120907	Product data sheet	-	NVT2003_04_06 v.3
Modifications:	<ul style="list-style-type: none">• Figure 6 “Pin configuration for HVQFN16”: pin arrangement updated• Table 2 “Pin description”:<ul style="list-style-type: none">– added separate column for NVT2006BS pinning– added package suffix to type number column headings under “Pin”– inserted rows to show every signal separately			
NVT2003_04_06 v.3	20111025	Product data sheet	-	NVT2003_04_06 v.2
NVT2003_04_06 v.2	20110329	Product data sheet	-	NVT2003_04_06 v.1
NVT2003_04_06 v.1	20101004	Product data sheet	-	-

17. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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