# PCA8565A

## Real-time clock/calendar

Rev. 02 — 4 December 2009 Product data sheet

## 1. General description

The PCA8565A is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional $I^2C$-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

AEC-Q100 compliant for automotive applications.

## 2. Features

- Provides year, month, day, weekday, hours, minutes, and seconds based on 32.768 kHz quartz crystal
- Clock operating voltage: 1.8 V to 5.5 V
- Extended operating temperature range: –40 °C to +125 °C
- Low backup current: typical 0.65 µA at $V_{DD}$ = 3.0 V and $T_{amb}$ = 25 °C
- 400 kHz two-line $I^2C$-bus interface (at $V_{DD}$ = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)
- Alarm and timer functions
- Two integrated oscillator capacitors
- Internal Power-On Reset (POR)
- $I^2C$-bus slave address: read A3h; write A2h
- Open-drain interrupt pin
- Century flag

## 3. Applications

- Automotive
- Industrial
- Applications that require a wide operating temperature range

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 18.

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Name | Description | Delivery form | Version |
| **Die type 1**[1] | | | | |
| PCA8565AU/5BA/1 | PCA8565AU | wire bond die; 9 bonding pads | unsawn wafer; thickness 280 µm | PCA8565AU |
| **Die type 2** | | | | |
| PCA8565AU/5BB/1 | PCA8565AU | wire bond die; 9 bonding pads | unsawn wafer; thickness 280 µm | PCA8565AU |

[1] Not to be used for new designs.

## 5. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| PCA8565AU/5BA/1 | PC8565A-1 |
| PCA8565AU/5BB/1 | PC8565A-1 |

## 6. Block diagram

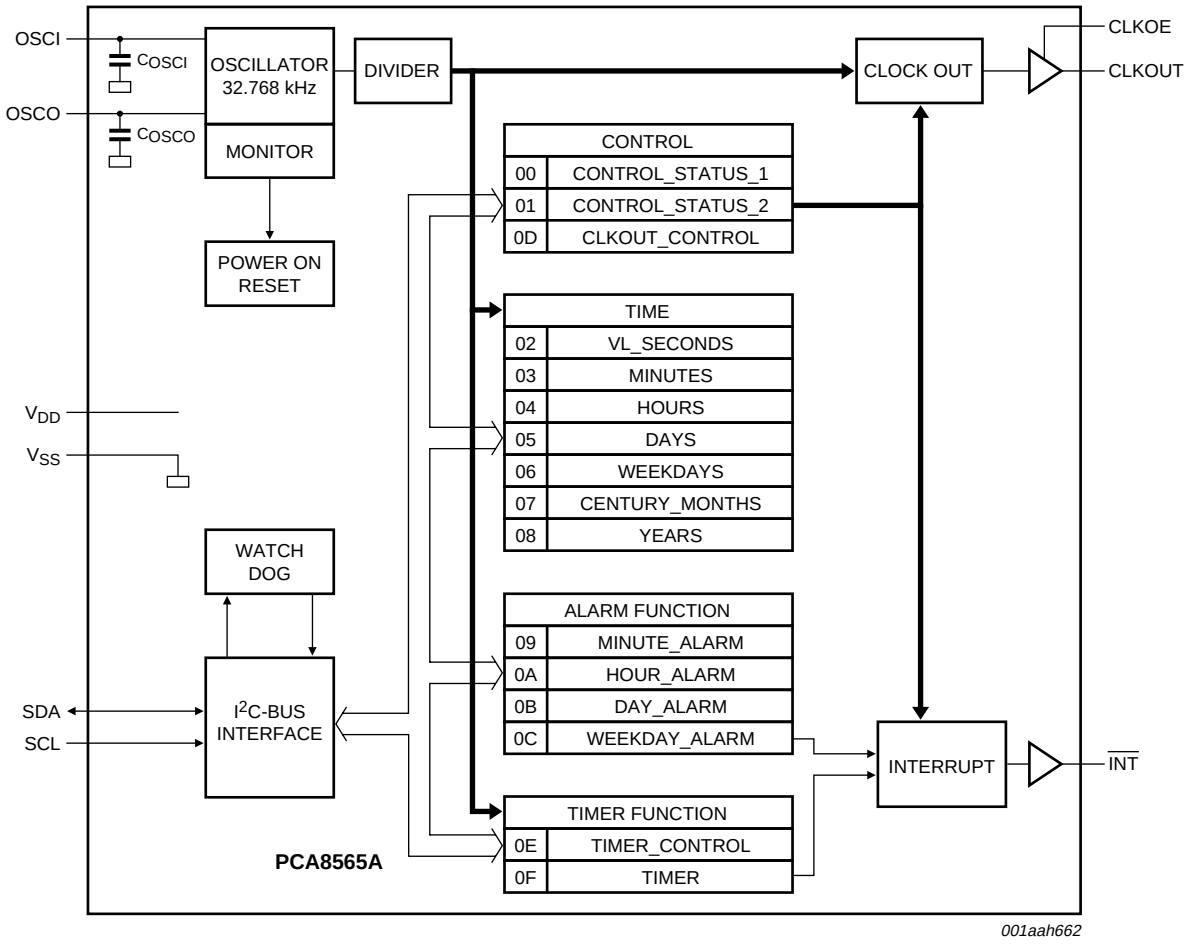
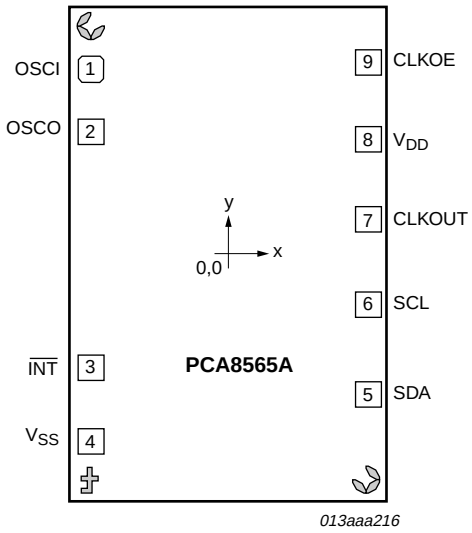



**Fig 1. Block diagram of PCA8565A**

# 7. Pinning information

## 7.1 Pinning




Viewed from active side. For mechanical details, see Figure 22.

**Fig 2. Pin configuration for PCA8565A**

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| OSCI | 1 | oscillator input |
| OSCO | 2 | oscillator output |
| $\overline{INT}$ | 3 | interrupt output (open-drain; active LOW) |
| $V_{SS}$ | 4 | ground supply voltage[1] |
| SDA | 5 | serial data input and output |
| SCL | 6 | serial clock input |
| CLKOUT | 7 | clock output (open-drain) |
| $V_{DD}$ | 8 | supply voltage |
| CLKOE | 9 | CLKOUT output enable input |

[1] The substrate (rear side of the die) is wired to $V_{SS}$ but should not be electrically contacted.

# 8. Functional description

The PCA8565A contains 16 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with two integrated capacitors, a frequency divider which provides the source clock for the RTC, a programmable clock output, a timer, an alarm, a voltage low detector, and a 400 kHz $I^2C$-bus interface.

All 16 registers (see Table 4) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years, as well as the minute alarm, hour alarm, day alarm, and weekday alarm registers are all in Binary Coded Decimal (BCD) format.

When one of the RTC registers is read, the contents of all time counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

## 8.1 CLKOUT output

A programmable square wave is available at the CLKOUT pin. Frequencies of 32.768 kHz, 1.024 kHz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output, and if disabled it becomes high-impedance.

## 8.2 Register organization

**Table 4. Register overview**

*Bit positions labelled as - are not implemented. Bit positions labelled as N should always be written with logic 0. After reset, all registers are set according to Table 29.*

| Address | Register name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Control registers** | | | | | | | | | |
| 00h | Control_status_1 | TEST1 | N | STOP | N | TESTC | N | N | N |
| 01h | Control_status_2 | N | N | N | TI_TP | AF | TF | AIE | TIE |
| **Time and date registers** | | | | | | | | | |
| 02h | VL_seconds | VL | SECONDS (0 to 59) | | | | | | |
| 03h | Minutes | - | MINUTES (0 to 59) | | | | | | |
| 04h | Hours | - | - | HOURS (0 to 23) | | | | | |
| 05h | Days | - | - | DAYS (1 to 31) | | | | | |
| 06h | Weekdays | - | - | - | - | - | WEEKDAYS (0 to 6) | | |
| 07h | Century_months | C | - | - | MONTH (1 to 12) | | | | |
| 08h | Years | YEARS (0 to 99) | | | | | | | |
| **Alarm registers** | | | | | | | | | |
| 09h | Minute_alarm | AE_M | MINUTE_ALARM (0 to 59) | | | | | | |
| 0Ah | Hour_alarm | AE_H | - | HOUR_ALARM (0 to 23) | | | | | |
| 0Bh | Day_alarm | AE_D | - | DAY_ALARM (1 to 31) | | | | | |
| 0Ch | Weekday_alarm | AE_W | - | - | - | - | WEEKDAY_ALARM (0 to 6) | | |
| **CLKOUT control register** | | | | | | | | | |
| 0Dh | CLKOUT_control | - | - | - | - | - | - | FD | |
| **Timer registers** | | | | | | | | | |
| 0Eh | Timer_control | TE | - | - | - | - | - | TD | |
| 0Fh | Timer | TIMER | | | | | | | |

## 8.3 Control registers

### 8.3.1 Register Control_status_1

**Table 5. Control_status_1 - control and status register 1 (address 00h) bit description**

| Bit | Symbol | Value | Description | Reference |
|---|---|---|---|---|
| 7 | TEST1 | 0[1] | normal mode;<br>must be set logic 0 during normal operations | Section 8.9 |
| | | 1 | EXT_CLK test mode | |
| 6 | N | 0[2] | default value | |
| 5 | STOP | 0[1] | RTC clock runs | Section 8.10 |
| | | 1 | RTC clock is stopped;<br>all RTC divider chain flip-flops are asynchronously set logic 0;<br>the RTC clock is stopped (CLKOUT at 32.768 kHz is still available);<br>$I^2C$-bus watchdog doesn't work | |
| 4 | N | 0[2] | default value | |
| 3 | TESTC | 0 | Power-On Reset (POR) override facility is disabled;<br>set logic 0 for normal operation | Section 8.11.1 |
| | | 1[1] | Power-On Reset (POR) override is enabled | |
| 2 to 0 | N | 000[2] | default value | |

[1] Default value.

[2] Bits labeled as N should always be written with logic 0.

### 8.3.2 Register Control_status_2

**Table 6. Control_status_2 - control and status register 2 (address 01h) bit description**

| Bit | Symbol | Value | Description | Reference |
|---|---|---|---|---|
| 7 to 5 | N | 000[1] | default value | |
| 4 | TI_TP | 0[2] | $\overline{INT}$ active when TF or AF is active (subject to the status of TIE and AIE) | Section 8.3.2.1 and Section 8.8 |
| | | 1 | $\overline{INT}$ pulses active according to Table 9 (subject to the status of TIE);<br>**Remark:** if AF and AIE are active then $\overline{INT}$ will be permanently active | |
| 3 | AF | 0[2] | read: alarm flag inactive | Section 8.3.2.1 |
| | | | write: alarm flag is cleared | |
| | | 1 | read: alarm flag active | |
| | | | write: alarm flag remains unchanged | |
| 2 | TF | 0[2] | read: timer flag inactive | Section 8.3.2.1 |
| | | | write: timer flag is cleared | |
| | | 1 | read: timer flag active | |
| | | | write: timer flag remains unchanged | |
| 1 | AIE | 0[2] | alarm interrupt disabled | Section 8.3.2.1 |
| | | 1 | alarm interrupt enabled | |
| 0 | TIE | 0[2] | timer interrupt disabled | Section 8.3.2.1 |
| | | 1 | timer interrupt enabled | |

[1] Bits labeled as N should always be written with logic 0.

[2] Default value.

#### 8.3.2.1 Interrupt output

**Bits TF and AF:** When an alarm occurs, AF is set logic 1. Similarly, at the end of a timer countdown, TF is set logic 1. These bits maintain their value until overwritten using the interface. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits.

To prevent one flag being overwritten while clearing another, logic AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

The following two tables are showing an example for clearing bit AF, but leaving bit TF unaffected. The flag is cleared by a write command, therefore bits 7 to 4 and 1 to 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

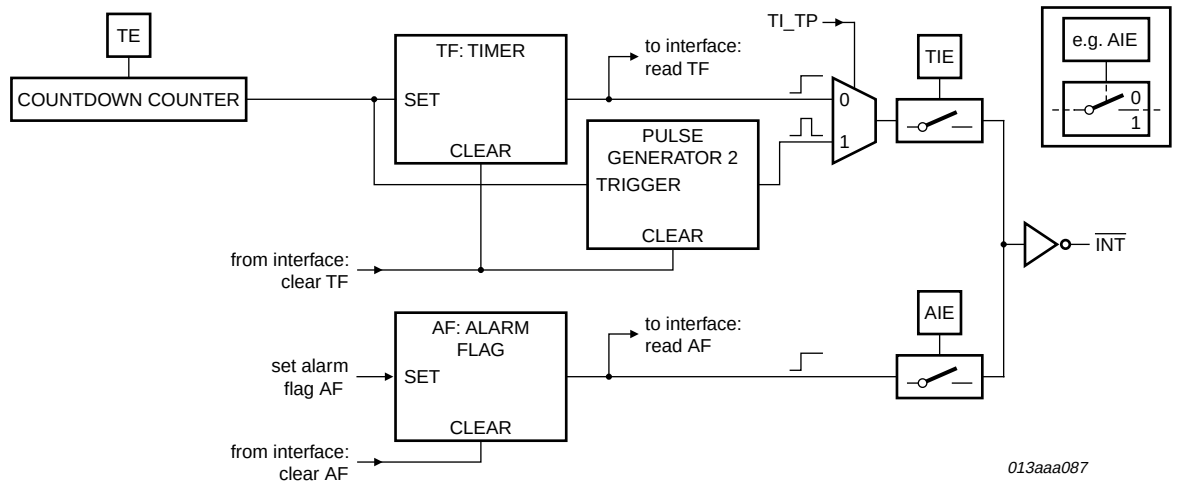
**Table 7. AF and TF flag location in register Control_status_2**

| Register | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Control_status_2 | - | - | - | - | AF | TF | - | - |

Table 8 shows what instruction must be sent to clear bit AF. In this example, bit TF is unaffected.

**Table 8. Example to clear only AF (bit 3) in register Control_status_2**

| Register | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Control_status_2 | - | - | - | - | 0 | 1 | - | - |




When bits TIE and AIE are disabled, pin $\overline{INT}$ will remain high-impedance.

**Fig 3. Interrupt scheme**

**Bits TIE and AIE:** These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

**Countdown timer interrupts:** The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 9).

**Table 9. $\overline{INT}$ operation (bit TI_TP = 1)[1]**

| Source clock (Hz) | $\overline{INT}$ period (s) | |
|---|---|---|
| | n = 1[2] | n > 1[2] |
| 4096 | $1/8192$ | $1/4096$ |
| 64 | $1/128$ | $1/64$ |
| 1 | $1/64$ | $1/64$ |
| $1/60$ | $1/64$ | $1/64$ |

[1] TF and $\overline{INT}$ become active simultaneously.

[2] n = loaded countdown value. Timer stops when n = 0.

## 8.4 Time and date registers

The majority of the registers are coded in the BCD format to simplify application use.

### 8.4.1 Register VL_seconds

**Table 10. VL_seconds - seconds and clock integrity status register (address 02h) bit description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | VL | 0 | - | clock integrity is guaranteed |
| | | 1[1] | - | integrity of the clock information is not guaranteed |
| 6 to 4 | SECONDS | 0 to 5 | ten's place | actual seconds coded in BCD format, see Table 11 |
| 3 to 0 | | 0 to 9 | unit place | |

[1] Start-up value.

**Table 11. Seconds coded in BCD format**

| Seconds value in decimal | Upper-digit (ten's place) | | | Digit (unit place) | | | |
|---|---|---|---|---|---|---|---|
| | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : | : | : |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

#### 8.4.1.1 Voltage-low detector and clock monitor

The PCA8565A has an on-chip voltage-low detector (see Figure 4). When $V_{DD}$ drops below $V_{low}$, bit VL in the VL_seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by using the interface.

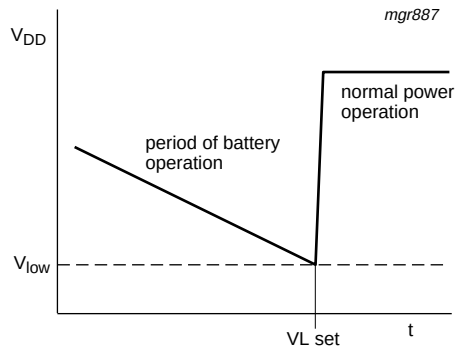



**Fig 4. Voltage-low detection**

The VL flag is intended to detect the situation when $V_{DD}$ is decreasing slowly, for example under battery operation. Should the oscillator stop or $V_{DD}$ reach $V_{low}$ before power is re-asserted, then the VL flag is set. This will indicate that the time may be corrupted.

### 8.4.2 Register Minutes

**Table 12. Minutes - minutes register (address 03h) bit description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | - | - | - | unused |
| 6 to 4 | MINUTES | 0 to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 8.4.3 Register Hours

**Table 13. Hours - hours register (address 04h) bit description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | HOURS | 0 to 2 | ten's place | actual hours coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 8.4.4 Register Days

**Table 14. Days - days register (address 05h) bit description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | DAYS[1] | 0 to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1] The PCA8565A compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

### 8.4.5 Register Weekdays

**Table 15. Weekdays - weekdays register (address 06h) bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 3 | - | - | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 16. |

**Table 16. Weekday assignments**

| Day[1] | Bit | | |
|---|---|---|---|
| | 2 | 1 | 0 |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday | 1 | 1 | 0 |

[1] Definition may be re-assigned by the user.

### 8.4.6 Register Century_months

**Table 17. Century_months - century flag and months register (address 07h) bit description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | C[1] | 0[2] | - | indicates the century is x |
| | | 1 | - | indicates the century is x + 1 |
| 6 to 5 | - | - | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 18 |
| 3 to 0 | | 0 to 9 | unit place | |

[1] This bit may be re-assigned by the user.

[2] This bit is toggled when the register Years overflows from 99 to 00.

**Table 18. Month assignments in BCD format**

| Month | Upper-digit (ten's place) | Digit (unit place) | | | |
|---|---|---|---|---|---|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

### 8.4.7 Register Years

Table 19. Years - years register (08h) bit description

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 to 4 | YEARS | 0 to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

## 8.5 Setting and reading the time

Figure 5 shows the data flow and data dependencies starting from the 1 Hz clock tick.

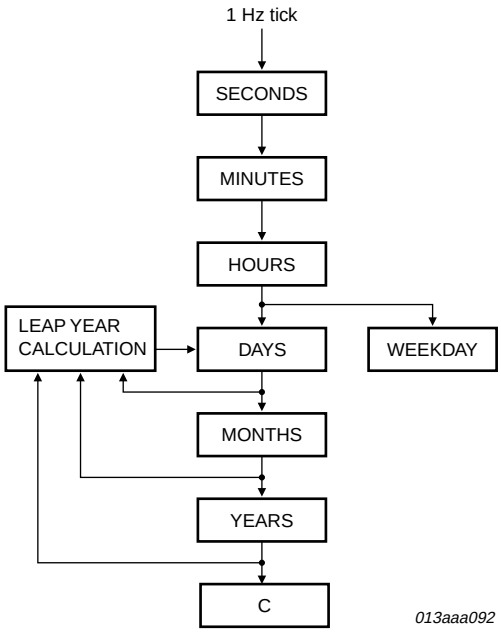



Fig 5. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers, during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 6).

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

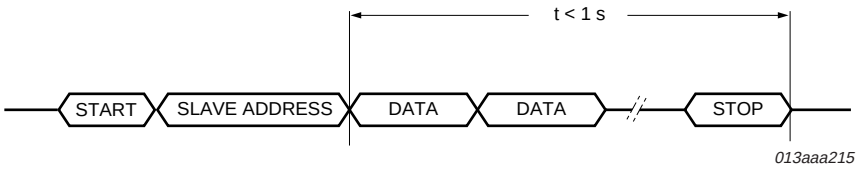



**Fig 6. Access time for read/write operations**

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).
2. Set the address pointer to 2 (VL_seconds) by sending 02h.
3. Send a RESTART condition or STOP followed by START.
4. Send the slave address for read (A3h).
5. Read VL_seconds.
6. Read Minutes.
7. Read Hours.
8. Read Days.
9. Read Weekdays.
10. Read Century_months.
11. Read Years.
12. Send a STOP condition.

## 8.6 Alarm registers

### 8.6.1 Register Minute_alarm

Table 20. Minute_alarm - minute alarm register (address 09h) bit description

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | AE_M | 0 | - | minute alarm is enabled |
| | | 1[1] | - | minute alarm is disabled |
| 6 to 4 | MINUTE_ALARM | 0 to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1] Default value.

### 8.6.2 Register Hour_alarm

Table 21. Hour_alarm - hour alarm register (address 0Ah) bit description

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | AE_H | 0 | - | hour alarm is enabled |
| | | 1[1] | - | hour alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | HOUR_ALARM | 0 to 2 | ten's place | hour alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1] Default value.

### 8.6.3 Register Day_alarm

Table 22. Day_alarm - day alarm register (address 0Bh) bit description

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | AE_D | 0 | - | day alarm is enabled |
| | | 1[1] | - | day alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | DAY_ALARM | 0 to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1] Default value.

### 8.6.4 Register Weekday_alarm

Table 23. Weekday_alarm - weekday alarm register (address 0Ch) bit description

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | AE_W | 0 | weekday alarm is enabled |
| | | 1[1] | weekday alarm is disabled |
| 6 to 3 | - | - | unused |
| 2 to 0 | WEEKDAY_ALARM | 0 to 6 | weekday alarm information coded in BCD format |

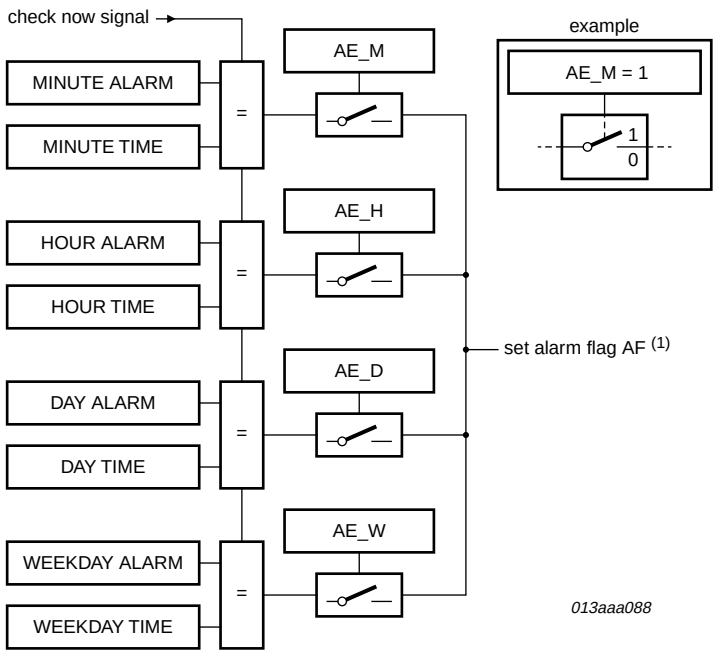
[1] Default value.

### 8.6.5 Alarm flag

By clearing the MSB of one or more of the alarm registers, AE_x (Alarm Enable), the corresponding alarm condition(s) are active. When an alarm occurs, AF is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by using the interface.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day or weekday, and its corresponding Alarm Enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF in register Control_status_2) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by using the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.




(1) Only when all enabled alarm settings are matching.
It's only on increment to a matched case that the alarm flag is set, see Section 8.6.5.

**Fig 7. Alarm function block diagram**

## 8.7 Register CLKOUT_control and clock output

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. To enable pin CLKOUT pin CLKOE must be set HIGH. When disabled, CLKOUT is high-impedance.

Table 24. CLKOUT_control - CLKOUT control register (address 0Dh) bit description

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 2 | - | - | unused |
| 1 to 0 | FD[1:0] | | frequency output at pin CLKOUT |
| | | 00[1] | 32.768 kHz |
| | | 01 | 1.024 kHz |
| | | 10 | 32 Hz |
| | | 11 | 1 Hz |

[1] Default value.

## 8.8 Timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $1/60$ Hz) and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag (TF) in the register Control_status_2. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt (on pin $\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI_TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

### 8.8.1 Register Timer_control

Table 25. Timer_control - timer control register (address 0Eh) bit description

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | TE | 0[1] | timer is disabled |
| | | 1 | timer is enabled |
| 6 to 2 | - | - | unused |
| 1 to 0 | TD[1:0] | | timer source clock frequency select[2] |
| | | 00 | 4.096 kHz |
| | | 01 | 64 Hz |
| | | 10 | 1 Hz |
| | | 11[2] | $1/60$ Hz |

[1] Default value.

[2] These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to $1/60$ Hz for power saving.

### 8.8.2 Register Timer

Table 26. Timer - timer register (address 0Fh) bit description

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 0 | TIMER[7:0] | 00h to FFh | countdown period in seconds: $CountdownPeriod = \frac{n}{SourceClockFrequency}$ where n is the countdown value |

Table 27. Timer register bits value range

| Bit | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

The timer register is an 8-bit binary countdown timer. It is enabled or disabled via the Timer_control register. The source clock for the timer is also selected by the Timer_control register. Other timer properties such as single or periodic interrupt generation are controlled via the register Control_status_2 (address 01h).

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

## 8.9 EXT_CLK test mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in register Control_status_1. Then pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a $2^6$ divide chain called a prescaler. The prescaler can be set into a known state by using the bit STOP. When the STOP bit is set, the prescaler is reset to logic 0 (STOP must be cleared before the prescaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a one-second increment.

**Remark:** Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_CLK test mode (Control_status_1, bit TEST1 = 1).
2. Set bit STOP (Control_status_1, bit STOP = 1).
3. Clear bit STOP (Control_status_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

## 8.10 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler ($F_2$ to $F_{14}$) to be held in reset and thus no 1 Hz ticks will be generated (see Figure 8). The time circuits can then be set and will not increment until the STOP bit is released (see Figure 9 and Table 28).

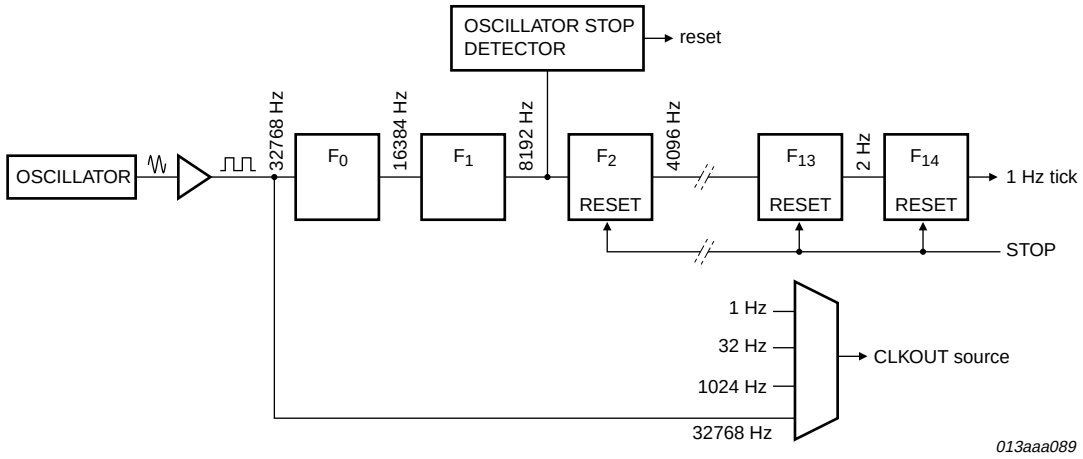



**Fig 8. STOP bit functional diagram**

The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz, and 1 Hz.

The lower two stages of the prescaler ($F_0$ and $F_1$) are not reset; and because the $I^2C$-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle (see Figure 9).

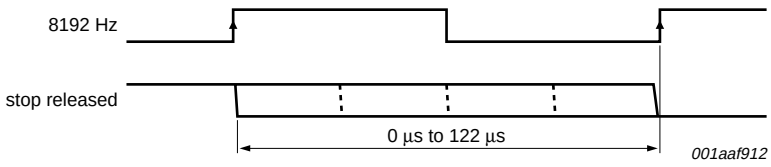
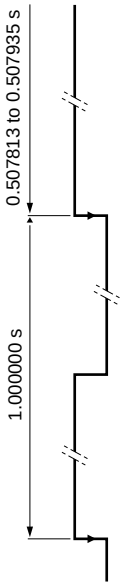



**Fig 9. STOP bit release timing**

**Table 28. First increment of time circuits after STOP bit release**

| Bit | Prescaler bits [1] | 1 Hz tick | Time | Comment |
|---|---|---|---|---|
| STOP | $F_0F_1$-$F_2$ to $F_{14}$ | | hh:mm:ss | |
| **Clock is running normally** | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | prescaler counting normally |
| **STOP bit is activated by user. $F_0F_1$ are not reset and values cannot be predicted externally** | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | prescaler is reset; time circuits are frozen |
| **New time is set by user** | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is reset; time circuits are frozen |
| **STOP bit is released by user** | | | | |
| 0 | XX-0 0000 0000 0000 |  | 08:00:00 | prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of $F_{14}$ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | - |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of $F_{14}$ increments the time circuits |



[1] $F_0$ is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits $F_0$ and $F_1$ not being reset (see Table 28) and the unknown state of the 32 kHz clock.

## 8.11 Reset

The PCA8565A includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the $I^2C$-bus logic is initialized including the address pointer and all registers are set according to Table 29. $I^2C$-bus communication is not possible during reset.

Table 29. Register reset values[1]

| Address | Register name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Control_status_1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 01h | Control_status_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | VL_seconds | 1 | x | x | x | x | x | x | x |
| 03h | Minutes | x | x | x | x | x | x | x | x |
| 04h | Hours | x | x | x | x | x | x | x | x |
| 05h | Days | x | x | x | x | x | x | x | x |
| 06h | Weekdays | x | x | x | x | x | x | x | x |
| 07h | Century_months | x | x | x | x | x | x | x | x |
| 08h | Years | x | x | x | x | x | x | x | x |
| 09h | Minute_alarm | 1 | x | x | x | x | x | x | x |
| 0Ah | Hour_alarm | 1 | x | x | x | x | x | x | x |
| 0Bh | Day_alarm | 1 | x | x | x | x | x | x | x |
| 0Ch | Weekday_alarm | 1 | x | x | x | x | x | x | x |
| 0Dh | CLKOUT_control | x | x | x | x | x | x | 0 | 0 |
| 0Eh | Timer_control | 0 | x | x | x | x | x | 1 | 1 |
| 0Fh | Timer | x | x | x | x | x | x | x | x |

[1] Registers marked ‘x’ are undefined at power-up and unchanged by subsequent resets.

### 8.11.1 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the $I^2C$-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 10. All timings are required minimums.

Once the override mode has been entered, the device immediately stops, being reset, and normal operation may commence, i.e., entry into the EXT_CLK test mode via $I^2C$-bus access. The override mode may be cleared by writing logic 0 to TESTC. TESTC must be set logic 1 before re-entry into the override mode is possible. Setting TESTC logic 0 during normal operation has no effect, except to prevent entry into the POR override mode.

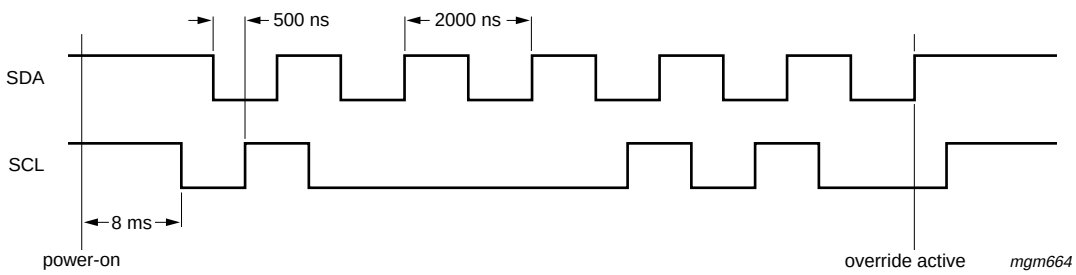



Fig 10. POR override sequence

# 9. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

## 9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

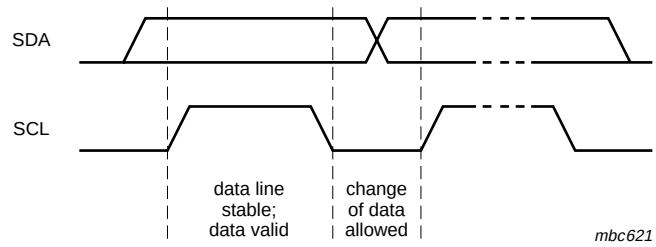



**Fig 11. Bit transfer**

## 9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P); see Figure 12.

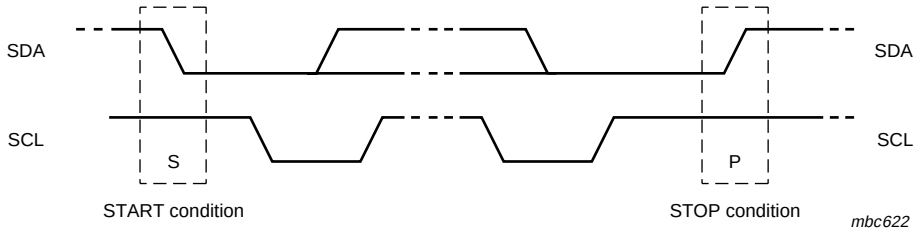



**Fig 12. Definition of START and STOP conditions**

## 9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 13).

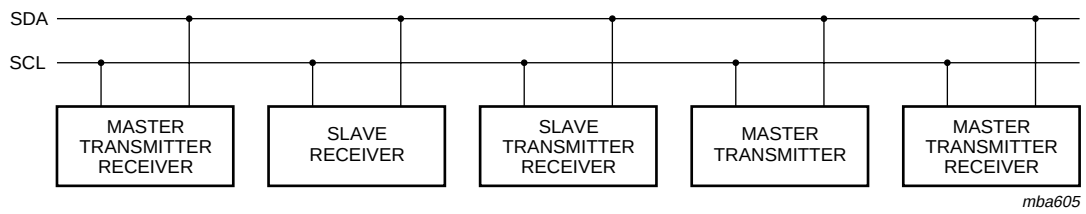



**Fig 13. System configuration**

## 9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the $I^2C$-bus is shown in Figure 14.

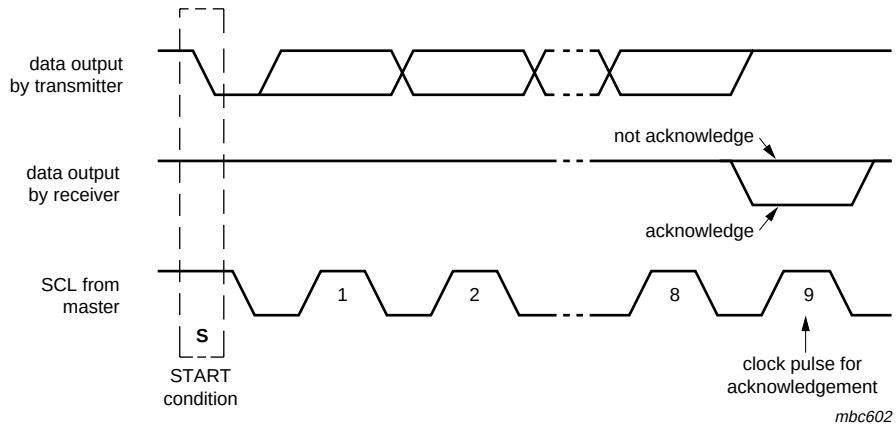



**Fig 14. Acknowledgement on the $I^2C$-bus**

## 9.5 I²C-bus protocol

### 9.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCA8565A acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Two slave addresses are reserved for the PCA8565A:

Read: A3h (10100011)

Write: A2h (10100010)

The PCA8565A slave address is shown in Figure 15.

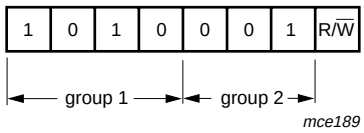



**Fig 15. Slave address**

### 9.5.2 Clock and calendar READ or WRITE cycles

The I²C-bus configuration for the different PCA8565A READ and WRITE cycles is shown in Figure 16, Figure 17, and Figure 18. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

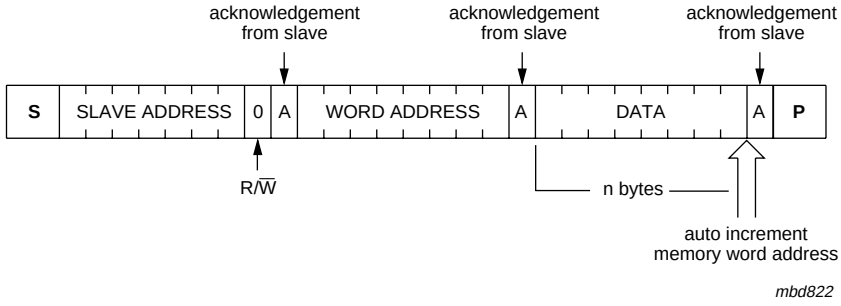
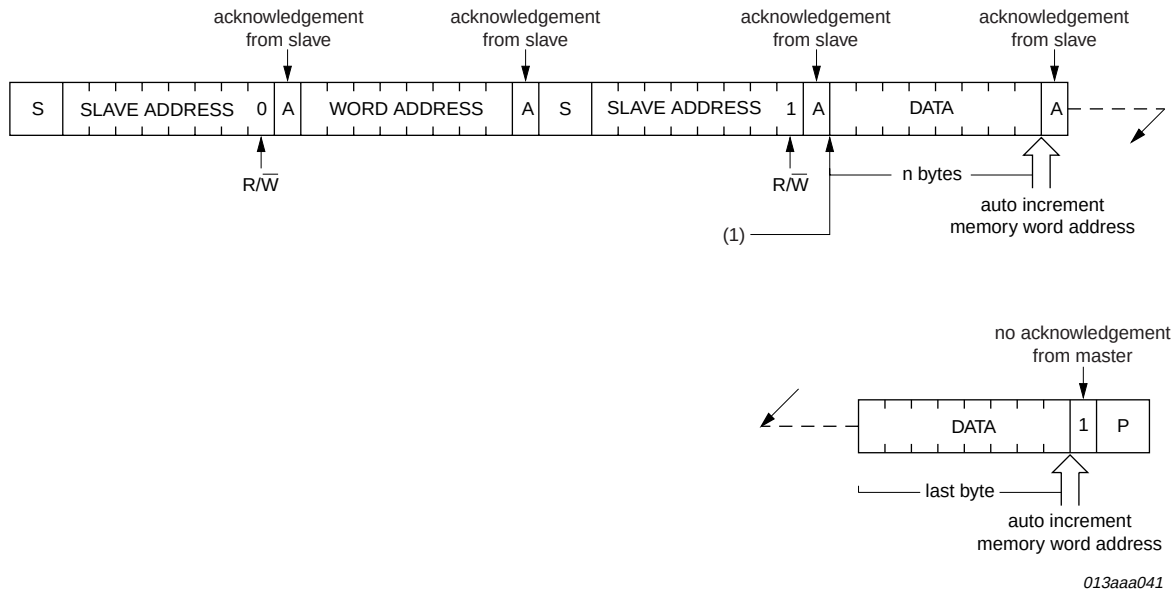



**Fig 16. Master transmits to slave receiver (WRITE mode)**




(1) At this moment master transmitter becomes master receiver and PCA8565A slave receiver becomes slave transmitter.

**Fig 17. Master reads after setting word address (write word address; READ data)**

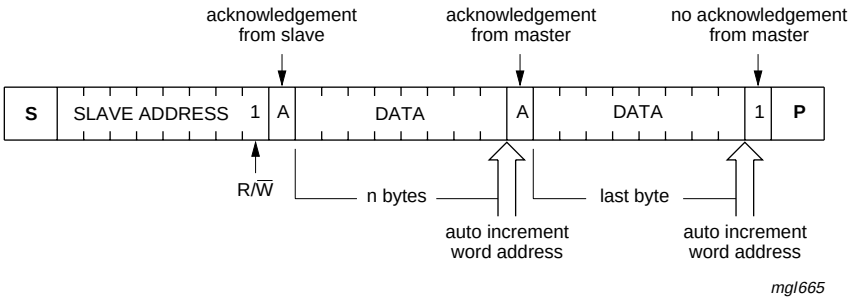



**Fig 18. Master reads slave immediately after first byte (READ mode)**

### 9.5.3 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface, the PCA8565A has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the PCA8565A will automatically clear the interface and allow the time counting circuits to continue counting.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid slave address.

## 10. Internal circuitry

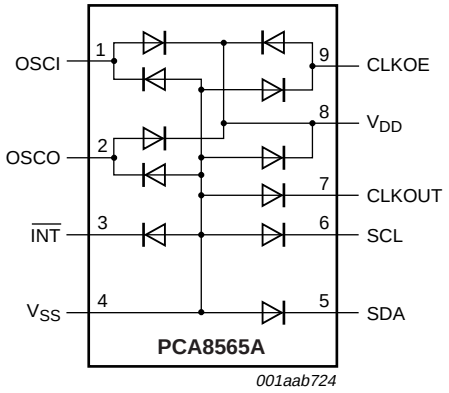



**Fig 19. Device diode protection**

# 11. Limiting values

**Table 30. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.5 | +6.5 | V |
| $I_{DD}$ | supply current | | | –50 | +50 | mA |
| $I_{SS}$ | ground supply current | | | –50 | +50 | mA |
| $V_I$ | input voltage | | | –0.5 | +6.5 | V |
| $V_O$ | output voltage | | | –0.5 | +6.5 | V |
| $I_I$ | input current | | | –10 | +10 | mA |
| $I_O$ | output current | | | –10 | +10 | mA |
| $P_{tot}$ | total power dissipation | | | - | 300 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [1] | | | |
| | | die type 1 | | - | ±2000 | V |
| | | die type 2 | | - | ±3500 | V |
| | | MM | [2] | | | |
| | | die type 1 | | - | ±200 | V |
| | | die type 2 | | - | ±250 | V |
| $I_{lu}$ | latch-up current | all pins but OSCI | [3] | - | 100 | mA |
| $T_{stg}$ | storage temperature | | [4] | –65 | +150 | °C |

[1] Pass level; Human Body Model (HBM) according to Ref. 4 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 5 “JESD22-A115”.

[3] Pass level; latch-up testing, according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$ = +125 °C).

[4] According to the NXP store and transport requirements (see Ref. 9 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

# 12. Static characteristics

**Table 31. Static characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +125 °C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DD}$ | supply voltage | $I^2C$-bus active; $f_{SCL}$ = 400 kHz | | 1.8 | - | 5.5 | V |
| | | for clock data integrity | | $V_{low}$ | - | 5.5 | V |
| $I_{DD}$ | supply current | interface active; $T_{amb}$ = −40 °C to +125 °C | | | | | |
| | | $f_{SCL}$ = 400 kHz | | - | 100 | 250 | µA |
| | | $f_{SCL}$ = 100 kHz | | - | 25 | 100 | µA |
| | | interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT = $V_{DD}$ | [1][2] | | | | |
| | | $T_{amb}$ = 125 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 1100 | 1800 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 1000 | 1600 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 950 | 1500 | nA |
| | | $T_{amb}$ = 105 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 850 | 1500 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 775 | 1300 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 750 | 1200 | nA |
| | | $T_{amb}$ = 85 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 600 | 1200 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 550 | 1000 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 550 | 900 | nA |
| | | $T_{amb}$ = 25 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 600 | 1200 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 550 | 1000 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 550 | 900 | nA |
| | | $T_{amb}$ = −40 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 850 | 1500 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 775 | 1300 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 750 | 1200 | nA |
| | | $T_{amb}$ = −40 °C to +85 °C | | | | | |
| | | $V_{DD}$ = 1.8 V | | - | 550 | - | nA |

**Table 31. Static characteristics** *...continued*

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +125 °C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | supply current | interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT enabled at 32 kHz | [1][2] | | | | |
| | | $T_{amb}$ = 125 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 1300 | 2500 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 1100 | 1900 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 1000 | 1700 | nA |
| | | $T_{amb}$ = 105 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 1100 | 2200 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 900 | 1600 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 800 | 1400 | nA |
| | | $T_{amb}$ = 85 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 900 | 1900 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 700 | 1300 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 600 | 1100 | nA |
| | | $T_{amb}$ = 25 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 900 | 1900 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 700 | 1300 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 600 | 1100 | nA |
| | | $T_{amb}$ = −40 °C | | | | | |
| | | $V_{DD}$ = 5.0 V | | - | 1100 | 2200 | nA |
| | | $V_{DD}$ = 3.0 V | | - | 900 | 1600 | nA |
| | | $V_{DD}$ = 2.0 V | | - | 800 | 1400 | nA |
| **Inputs** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | $V_{SS}$ − 0.3 | - | 0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | pins SCL, SDA, CLKOE, OSCI | | 0.7$V_{DD}$ | - | - | V |
| $I_{LI}$ | input leakage current | pins SCL, SDA; $V_I$ = $V_{DD}$ or $V_{SS}$ | | −1 | 0 | +1 | µA |
| $C_i$ | input capacitance | | [3] | - | - | 7 | pF |
| **Outputs** | | | | | | | |
| $I_{OL}$ | LOW-level output current | output sink current; $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | | | | |
| | | pin SDA | | 3 | - | - | mA |
| | | pin $\overline{INT}$ | | 1 | - | - | mA |
| | | pin CLKOUT; $V_O$ = $V_{DD}$ or $V_{SS}$ | | 1 | - | - | mA |
| $I_{LO}$ | output leakage current | | | −1 | 0 | +1 | µA |
| **Voltage detector and temperature** | | | | | | | |
| $V_{low}$ | low voltage | | | - | 0.9 | 1.7 | V |
| $T_{amb}$ | ambient temperature | | | −40 | - | +125 | °C |

[1] Timer source clock = $\frac{1}{60}$ Hz, level of pins SCL and SDA is $V_{DD}$ or $V_{SS}$.

[2] Worst case is at high temperature and high supply voltage.

[3] Tested on sample basis.

# 13. Dynamic characteristics

**Table 32. Dynamic characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to + 125 °C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Oscillator** | | | | | | | |
| $C_{L(itg)}$ | integrated load capacitance | | [1] | 6 | 8 | 10 | pF |
| $\Delta f_{osc}/f_{osc}$ | relative oscillator frequency variation | $\Delta V_{DD}$ = 200 mV; $T_{amb}$ = 25 °C | | - | 0.2 | - | ppm |
| **CLKOUT output** | | | | | | | |
| $\delta_{CLKOUT}$ | duty cycle on pin CLKOUT | | [2] | - | 50 | - | % |
| **Timing characteristics: I²C-bus** [3][4] | | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | [5] | - | - | 400 | kHz |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 0.6 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 0.6 | - | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 0.6 | - | - | µs |
| $t_r$ | rise time | of SCL and SDA signals | | - | - | 0.3 | µs |
| $t_f$ | fall time | of SCL and SDA signals | | - | - | 0.3 | µs |
| $C_b$ | capacitive load for each bus line | | | - | - | 400 | pF |
| $t_{SU;DAT}$ | data set-up time | | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | µs |
| $t_{w(spike)}$ | spike pulse width | tolerable | | - | - | 50 | ns |

[1] Integrated load capacitance, $C_{L(itg)}$, is a calculation of $C_{OSCI}$ and $C_{OSCO}$ in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

[2] Unspecified for $f_{CLKOUT}$ = 32.768 kHz.

[3] All timing values are valid within the operating supply voltage range at ambient temperature and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.

[4] A detailed description of the I²C-bus specification is given in Ref. 10 “UM10204”.

[5] I²C-bus access time between two starts or between a start and a stop condition to this device must be less than one second.

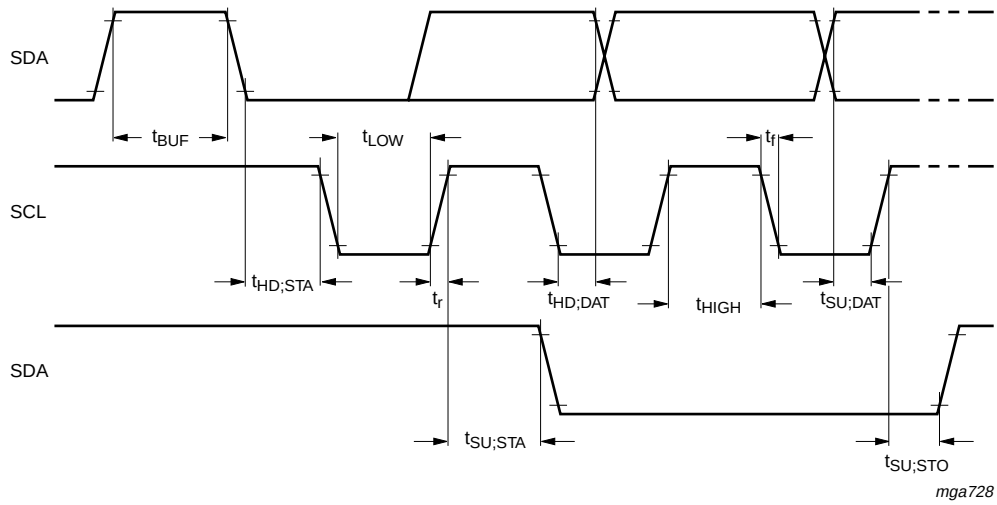
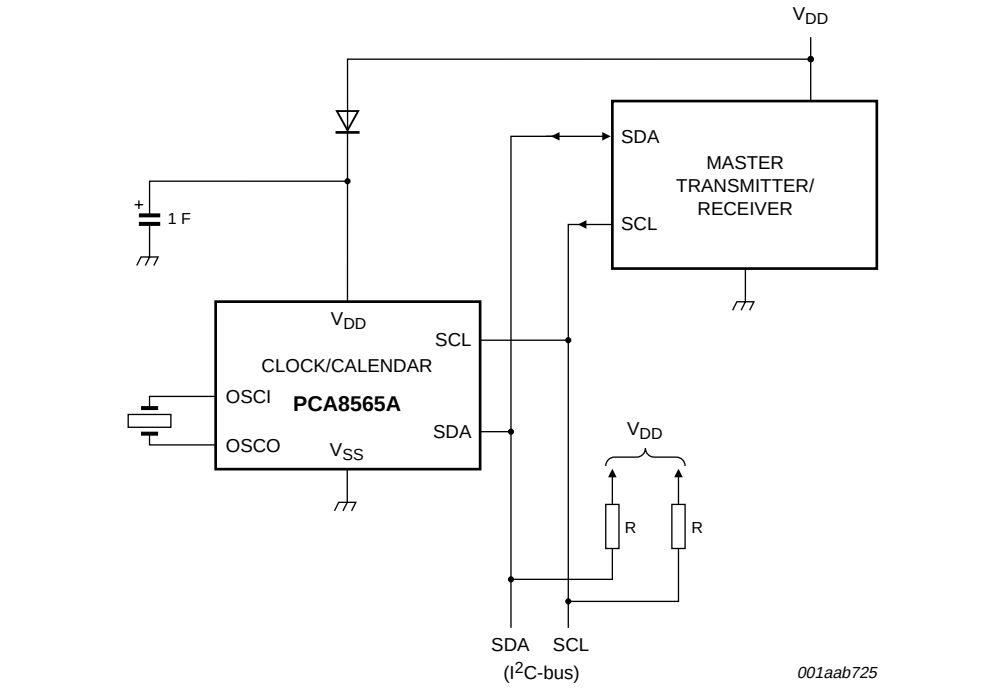



Fig 20. I²C-bus timing waveforms

## 14. Application information

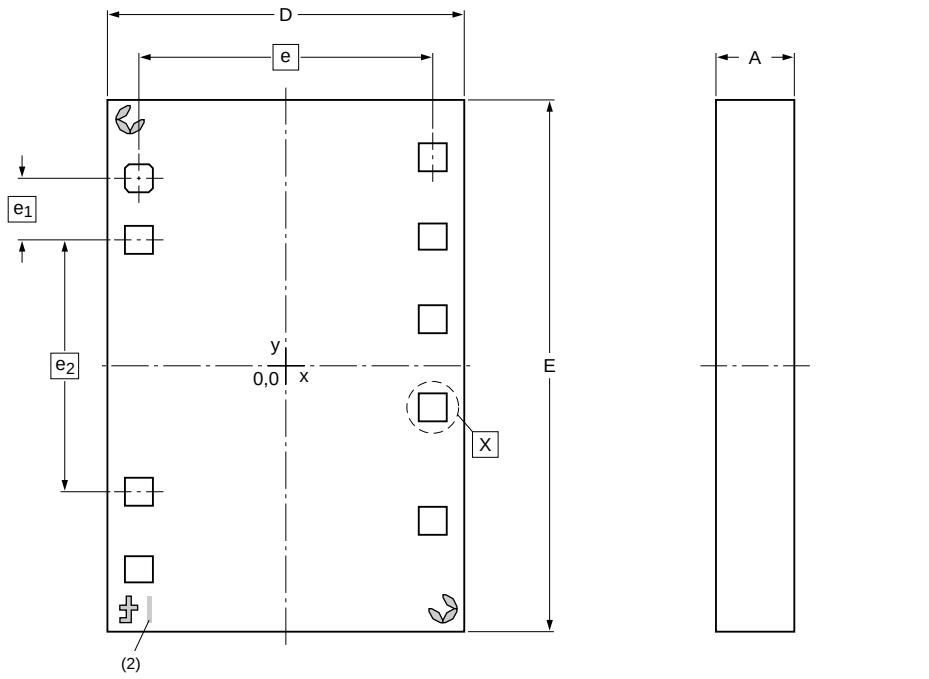



Connect CLKOE to an appropriate level.

Fig 21. Application diagram

# 15. Bare die outline

**Wire bond die; 9 bonding pads** **PCA8565AU**




Dimensions Die type 1

| Unit | | A | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $P_1$ | $P_2$ | $P_3$ | $P_4$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | | | | | | | | | | |
| | nom | 0.28 | 1.27 | 1.9 | 1.05 | 0.22 | 0.9 | 0.1 | 0.09 | 0.1 | 0.09 |
| | min | | | | | | | | | | |

Dimensions Die type 2

| Unit | | A | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $P_1$ | $P_2$ | $P_3$ | $P_4$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | | | | | | | | | | |
| | nom | 0.28 | 1.26 | 1.89 | 1.05 | 0.22 | 0.9 | 0.1 | 0.09 | 0.1 | 0.09 |
| | min | | | | | | | | | | |

Note
1. Chip dimensions including sawline.
2. Marking code: PC8565A-1

*pca8565au_do*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PCA8565AU | | | | | | ~~09-08-29~~ 09-09-09 |

**Fig 22. Bare die outline**

**Table 33. Pin description**

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip; see Figure 22.*

| Symbol | Pad | X | Y |
|---|---|---|---|
| OSCI | 1 | –523.0 µm | 689.4 µm |
| OSCO | 2 | –523.0 µm | 469.4 µm |
| $\overline{INT}$ | 3 | –523.0 µm | –429.8 µm |
| $V_{SS}$ | 4 | –523.0 µm | –684.4 µm |
| SDA | 5 | 524.9 µm | –523.8 µm |
| SCL | 6 | 524.9 µm | –138.6 µm |
| CLKOUT | 7 | 524.9 µm | 162.5 µm |
| $V_{DD}$ | 8 | 524.9 µm | 443.3 µm |
| CLKOE | 9 | 524.9 µm | 716.3 µm |

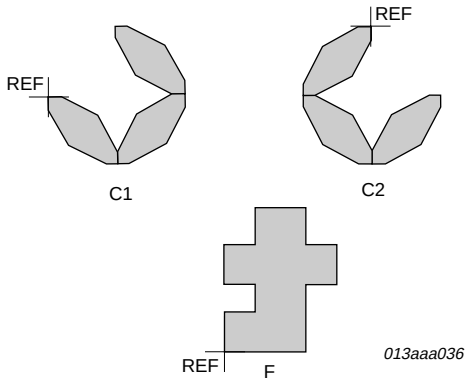



**Fig 23. Alignment marks**

**Table 34. Alignment mark description**

*All x/y coordinates represent the position of the REF point (see Figure 23) with respect to the center (x/y = 0) of the chip; see Figure 22.*

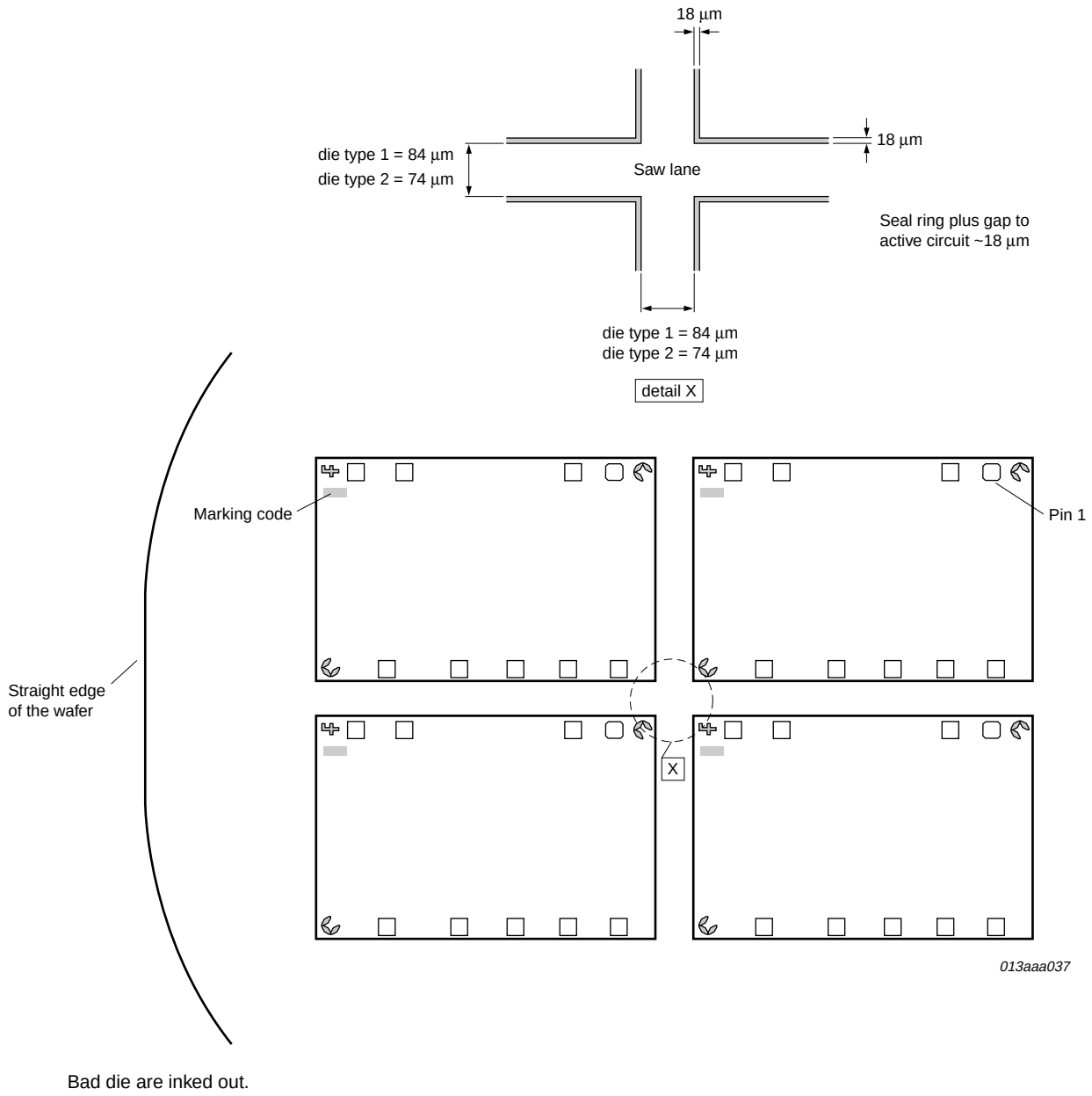
| Symbol | Size (µm) | X | Y |
|---|---|---|---|
| C1 | 100 × 100 | 465.2 µm | –826.3 µm |
| C2 | 100 × 100 | –523.5 µm | 890.0 µm |
| F | 90 × 117 | –569.9 µm | –885.5 µm |

## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

# 17. Packing information

## 17.1 Wafer information




Bad die are inked out.

**Fig 24. Wafer layout**

# 18. Abbreviations

Table 35. Abbreviations

| Acronym | Description |
|---|---|
| AEC | Automotive Electronics Council |
| BCD | Binary Coded Decimal |
| CMOS | Complementary Metal Oxide Semiconductor |
| HBM | Human Body Model |
| $I^2C$ | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| MM | Machine Model |
| MOS | Metal Oxide Semiconductor |
| MSB | Most Significant Bit |
| POR | Power-On Reset |
| RTC | Real Time Clock |
| SCL | Serial Clock Line |
| SDA | Serial Data Line |

## 19. References

[1] **AN10706 —** Handling bare die

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[5] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[6] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **NX3-00092 —** NXP store and transport requirements

[10] **UM10204 —** $I^2C$-bus specification and user manual

## 20. Revision history

**Table 36. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA8565A_2 | 20091204 | Product data sheet | - | PCA8565A_1 |
| Modifications: | • Added new product type PCA8565AU/5BB/1 | | | |
| PCA8565A_1 | 20080222 | Product data sheet | - | - |

# 21. Legal information

## 21.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 21.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 21.3 Disclaimers

**General —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Bare die —** All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

## 21.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I²C-bus —** logo is a trademark of NXP B.V.

# 22. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 23. Contents


**1 General description . . . . . 1**
**2 Features . . . . . 1**
**3 Applications . . . . . 1**
**4 Ordering information . . . . . 2**
**5 Marking . . . . . 2**
**6 Block diagram . . . . . 3**
**7 Pinning information . . . . . 4**
7.1 Pinning . . . . . 4
7.2 Pin description . . . . . 4
**8 Functional description . . . . . 5**
8.1 CLKOUT output . . . . . 5
8.2 Register organization . . . . . 6
8.3 Control registers . . . . . 7
8.3.1 Register Control_status_1 . . . . . 7
8.3.2 Register Control_status_2 . . . . . 7
8.3.2.1 Interrupt output . . . . . 8
8.4 Time and date registers . . . . . 10
8.4.1 Register VL_seconds . . . . . 10
8.4.1.1 Voltage-low detector and clock monitor . . . . . 10
8.4.2 Register Minutes . . . . . 11
8.4.3 Register Hours . . . . . 11
8.4.4 Register Days . . . . . 11
8.4.5 Register Weekdays . . . . . 11
8.4.6 Register Century_months . . . . . 12
8.4.7 Register Years . . . . . 13
8.5 Setting and reading the time . . . . . 13
8.6 Alarm registers . . . . . 15
8.6.1 Register Minute_alarm . . . . . 15
8.6.2 Register Hour_alarm . . . . . 15
8.6.3 Register Day_alarm . . . . . 15
8.6.4 Register Weekday_alarm . . . . . 15
8.6.5 Alarm flag . . . . . 16
8.7 Register CLKOUT_control and clock output . . 16
8.8 Timer function . . . . . 17
8.8.1 Register Timer_control . . . . . 17
8.8.2 Register Timer . . . . . 17
8.9 EXT_CLK test mode . . . . . 18
8.10 STOP bit function . . . . . 19
8.11 Reset . . . . . 20
8.11.1 Power-On Reset (POR) override . . . . . 21
**9 Characteristics of the I²C-bus . . . . . 22**
9.1 Bit transfer . . . . . 22
9.2 START and STOP conditions . . . . . 22
9.3 System configuration . . . . . 22
9.4 Acknowledge . . . . . 23
9.5 I²C-bus protocol . . . . . 24
9.5.1 Addressing . . . . . 24
9.5.2 Clock and calendar READ or WRITE cycles . 24
9.5.3 Interface watchdog timer . . . . . 25
**10 Internal circuitry . . . . . 26**
**11 Limiting values . . . . . 27**
**12 Static characteristics . . . . . 28**
**13 Dynamic characteristics . . . . . 30**
**14 Application information . . . . . 31**
**15 Bare die outline . . . . . 32**
**16 Handling information . . . . . 33**
**17 Packing information . . . . . 34**
17.1 Wafer information . . . . . 34
**18 Abbreviations . . . . . 35**
**19 References . . . . . 36**
**20 Revision history . . . . . 36**
**21 Legal information . . . . . 37**
21.1 Data sheet status . . . . . 37
21.2 Definitions . . . . . 37
21.3 Disclaimers . . . . . 37
21.4 Trademarks . . . . . 37
**22 Contact information . . . . . 37**
**23 Contents . . . . . 38**




For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 4 December 2009**
**Document identifier: PCA8565A_2**