



# PCA8576C

Universal LCD driver for low multiplex rates

Rev. 1 — 22 July 2010

Product data sheet

## 1. General description

The PCA8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)<sup>1</sup> with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCA8576C is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I<sup>2</sup>C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing and by hardware subaddressing.

AEC-Q100 compliant for automotive applications.

## 2. Features and benefits

- Single-chip LCD controller and driver
- 40 segment drives:
  - ◆ Up to twenty 7-segment alphanumeric characters
  - ◆ Up to ten 14-segment alphanumeric characters
  - ◆ Any graphics of up to 160 elements
- Versatile blinking modes
- No external components required (even in multiple device applications)
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static,  $\frac{1}{2}$ , or  $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Wide logic LCD supply range:
  - ◆ From 2 V for low-threshold LCDs
  - ◆ Up to 6 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- May be cascaded for large LCD applications (up to 2560 segments possible)
- No external components
- Separate or combined LCD and logic supplies
- Optimized pinning for plane wiring in both and multiple PCA8576C applications
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 16](#).



3. Ordering information

Table 1. Ordering information

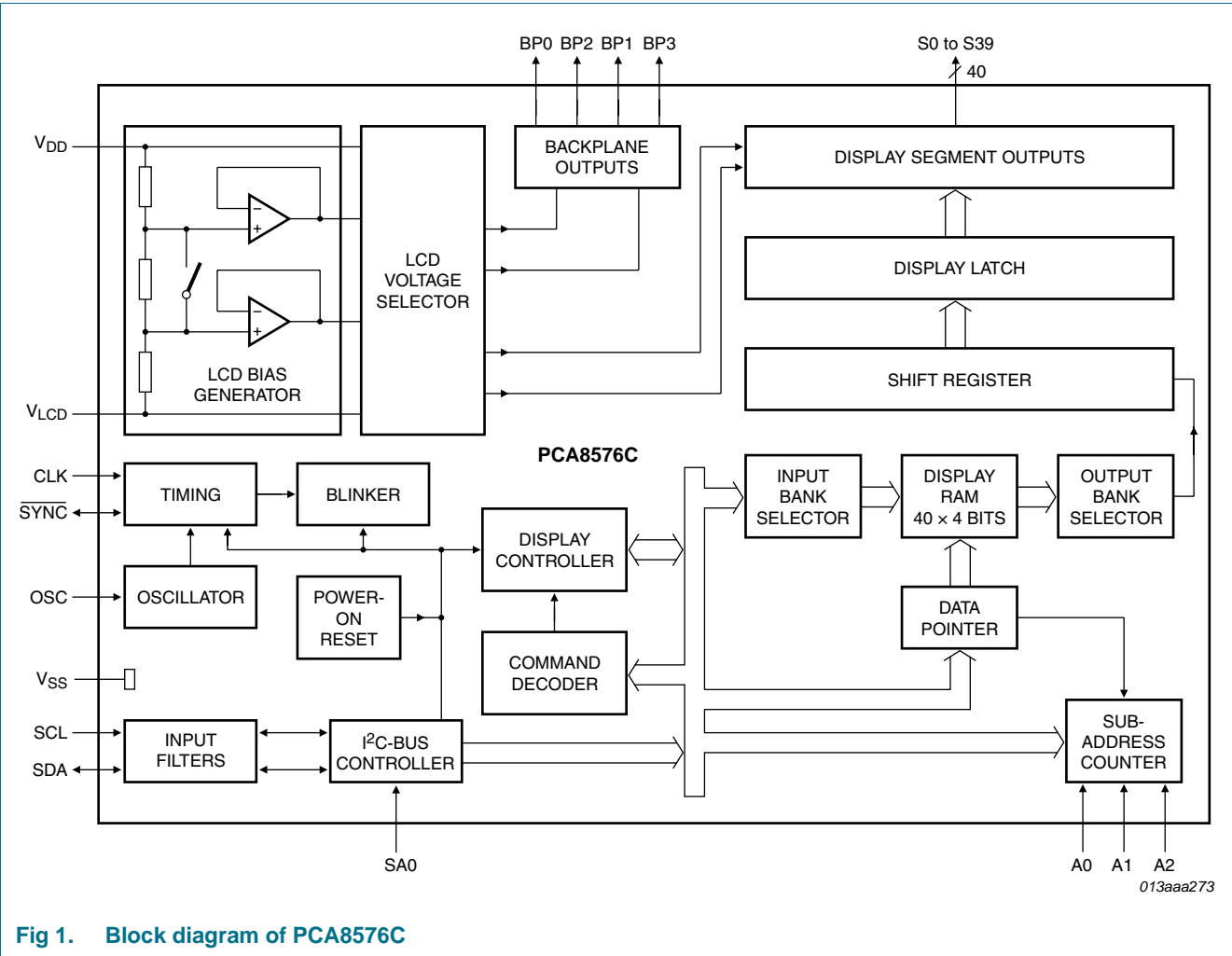
Type number	Package		
	Name	Description	Version
PCA8576CH/Q900/1	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4. Marking

Table 2. Marking codes

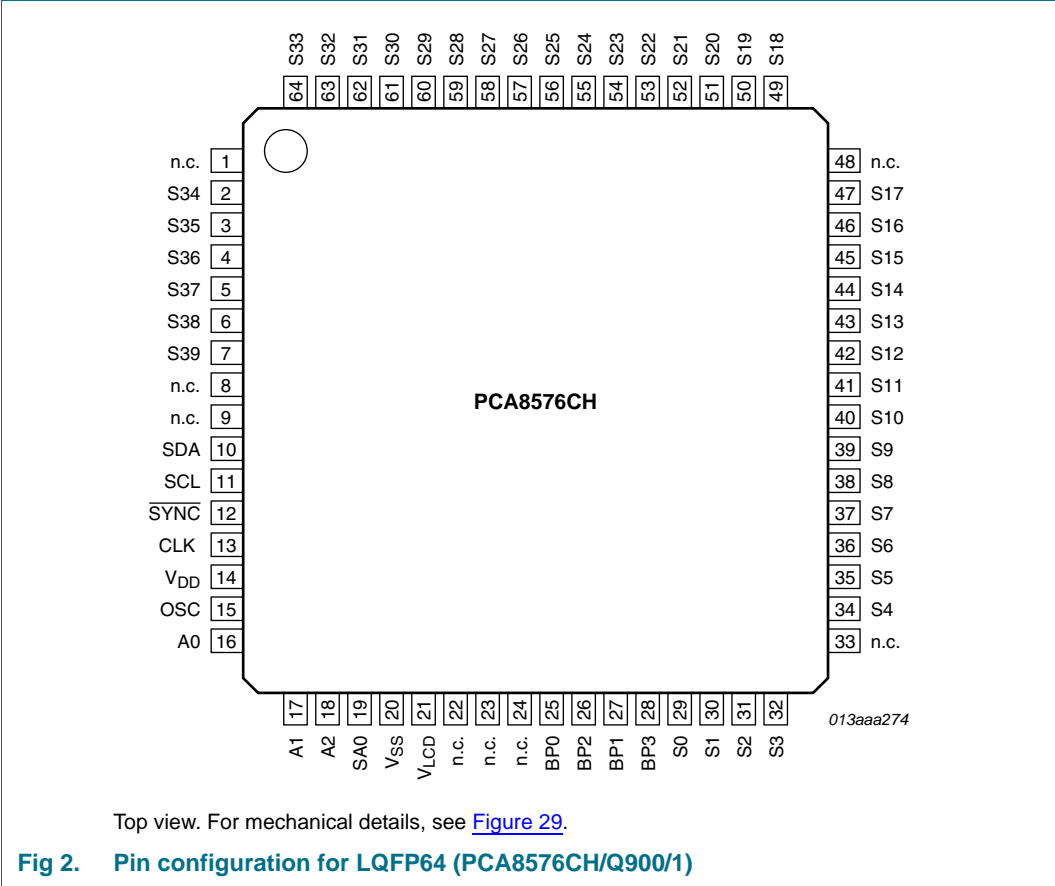
Type number	Marking code
PCA8576CH/Q900/1	PCA8576CQ900

5. Block diagram



6. Pinning information

6.1 Pinning



## 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	LQFP64 (PCA8576CH/Q900/1)	Type	
SDA	10	input/output	I <sup>2</sup> C-bus serial data input and output
SCL	11	input	I <sup>2</sup> C-bus serial clock input
$\overline{\text{SYNC}}$	12	input/output	cascade synchronization input and output
CLK	13	input/output	external clock input/output
V <sub>DD</sub>	14	supply	supply voltage
OSC	15	input	internal oscillator enable input
A0 to A2	16 to 18	input	subaddress inputs
SA0	19	input	I <sup>2</sup> C-bus address input; bit 0
V <sub>SS</sub>	20	supply	ground supply voltage
V <sub>LCD</sub>	21	supply	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	output	LCD backplane outputs
S0 to S39	2 to 7, 29 to 32, 34 to 47, 49 to 64	output	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	not connected; do not connect and do not use as feed through

7. Functional description

The PCA8576C is a versatile peripheral device designed to interface between any microprocessor or microcontroller to a wide variety of LCD segment or dot matrix displays (see [Figure 3](#)). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

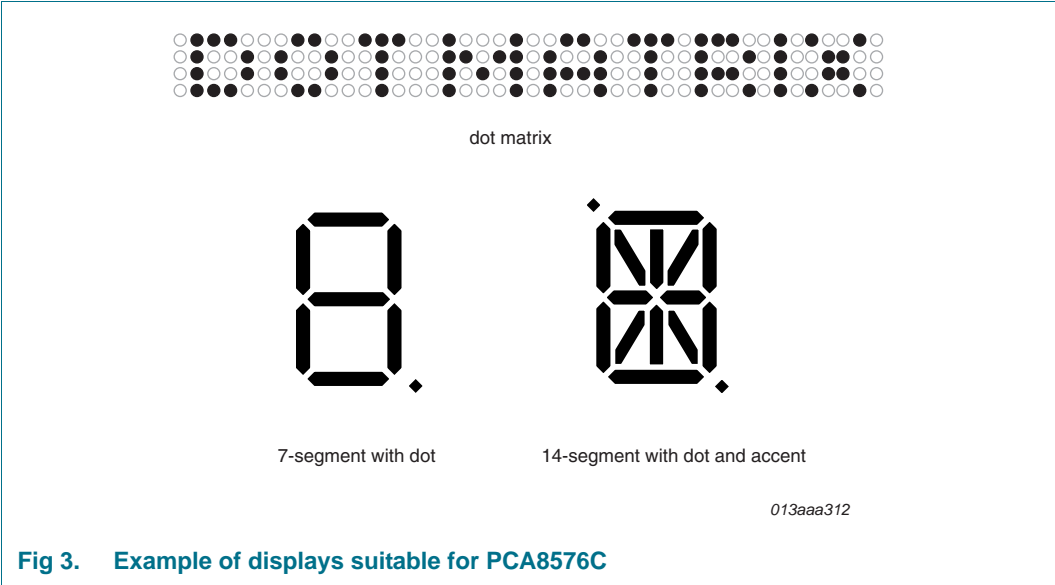


Fig 3. Example of displays suitable for PCA8576C

The possible display configurations of the PCA8576C depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 4](#). All of these configurations can be implemented in the typical system shown in [Figure 4](#).

Table 4. Selection of possible display configurations

Number of				
Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment	14-segment	
4	160	20	10	160 dots (4 × 40)
3	120	15	7	120 dots (3 × 40)
2	80	10	5	80 dots (2 × 40)
1	40	5	2	40 dots (1 × 40)

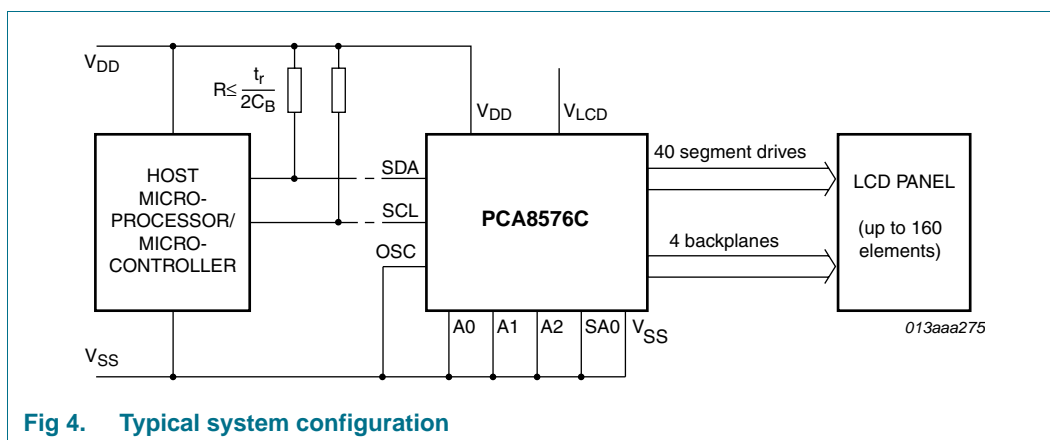


Fig 4. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I<sup>2</sup>C-bus communication channel with the PCA8576C.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V<sub>SS</sub>. The only other connections required to complete the system are the power supplies (pins V<sub>DD</sub>, V<sub>SS</sub>, and V<sub>LCD</sub>) and the LCD panel selected for the application.

## 7.1 Power-On-Reset (POR)

At power-on the PCA8576C resets to the following starting conditions:

- All backplane and segment outputs are set to V<sub>DD</sub>
- The selected drive mode is 1:4 multiplex with  $\frac{1}{3}$  bias
- Blinking is switched off
- Input and output bank selectors are reset (as defined in [Table 8](#))
- The I<sup>2</sup>C-bus interface is initialized
- The data pointer and the subaddress counter are cleared

**Remark:** Do not transfer data on the I<sup>2</sup>C-bus for at least 1 ms after a power-on to allow the reset action to complete.

## 7.2 LCD bias generator

The full-scale LCD voltage (V<sub>oper</sub>) is obtained from V<sub>DD</sub> – V<sub>LCD</sub>. The LCD voltage may be temperature compensated externally through the V<sub>LCD</sub> supply to pin V<sub>LCD</sub>.

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between V<sub>DD</sub> and V<sub>LCD</sub>. The center resistor can be switched out of the circuit to provide a  $\frac{1}{2}$  bias voltage level for the 1:2 multiplex configuration.

### 7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of  $V_{LCD}$  and the resulting discrimination ratios (D) are given in [Table 5](#).

**Table 5. Biasing characteristics**

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	$\infty$
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for  $V_{LCD}$  is determined by equating  $V_{off(RMS)}$  with a defined LCD threshold voltage ( $V_{th}$ ), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is  $V_{LCD} > 3V_{th}$ .

Multiplex drive modes of 1:3 and 1:4 with  $\frac{1}{2}$  bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by  $\frac{1}{1+a}$ , where the values for a are

a = 1 for  $\frac{1}{2}$  bias

a = 2 for  $\frac{1}{3}$  bias

The RMS on-state voltage ( $V_{on(RMS)}$ ) for the LCD is calculated with [Equation 1](#):

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ( $V_{off(RMS)}$ ) for the LCD is calculated with [Equation 2](#):

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of  $V_{on(RMS)}$  to  $V_{off(RMS)}$  and is determined from [Equation 3](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

Using [Equation 3](#), the discrimination for an LCD drive mode of 1:3 multiplex with  $\frac{1}{2}$  bias is  $\sqrt{3} = 1.732$  and the discrimination for an LCD drive mode of 1:4 multiplex with  $\frac{1}{2}$  bias is  $\frac{\sqrt{21}}{3} = 1.528$ .

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage  $V_{LCD}$  as follows:

- 1:3 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \left[ \frac{(4 \times \sqrt{3})}{3} \right] = 2.309V_{off(RMS)}$

These compare with  $V_{LCD} = 3V_{off(RMS)}$  when  $\frac{1}{3}$  bias is used.

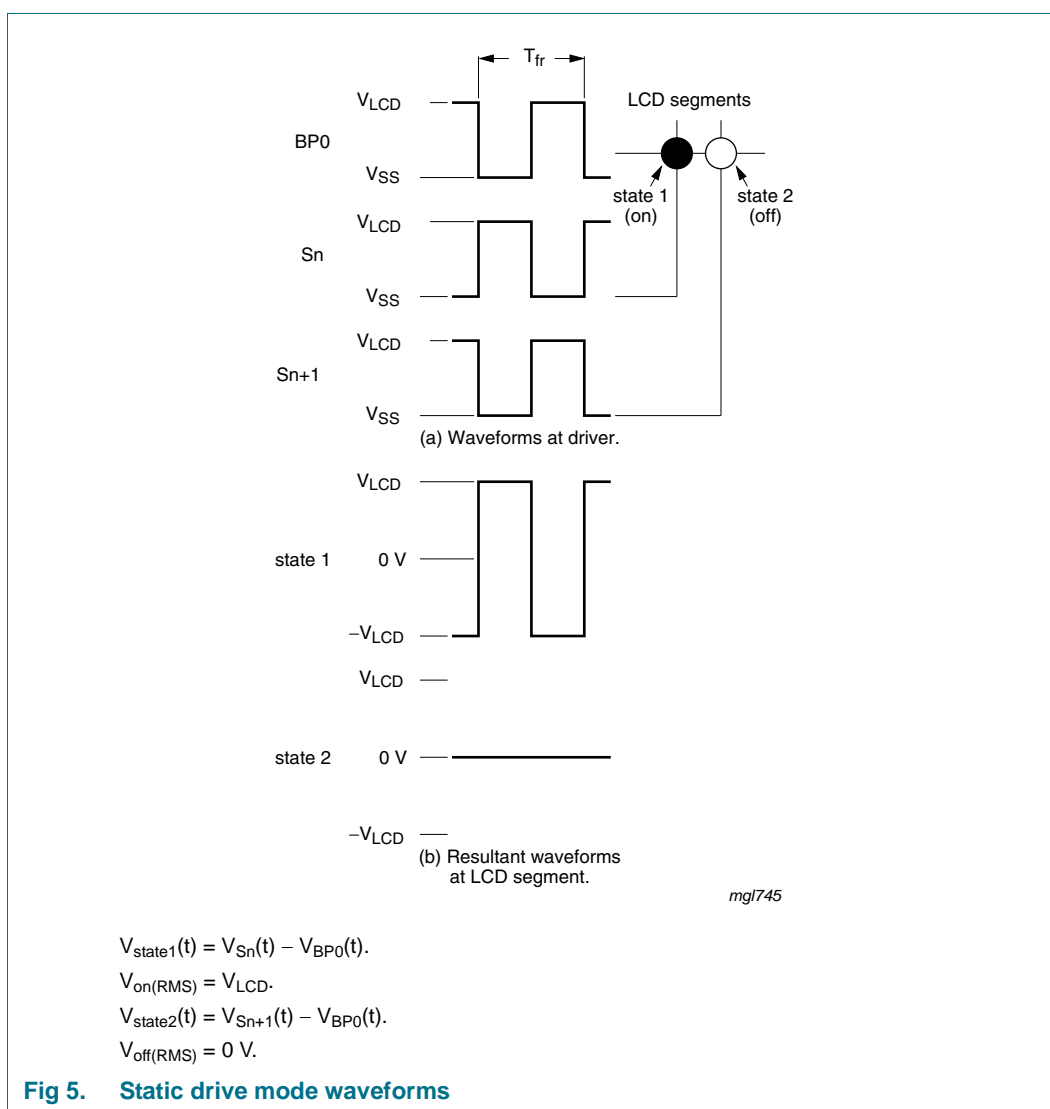
It should be noted that  $V_{LCD}$  is sometimes referred as the LCD operating voltage.



## 7.4 LCD drive mode waveforms

### 7.4.1 Static drive mode

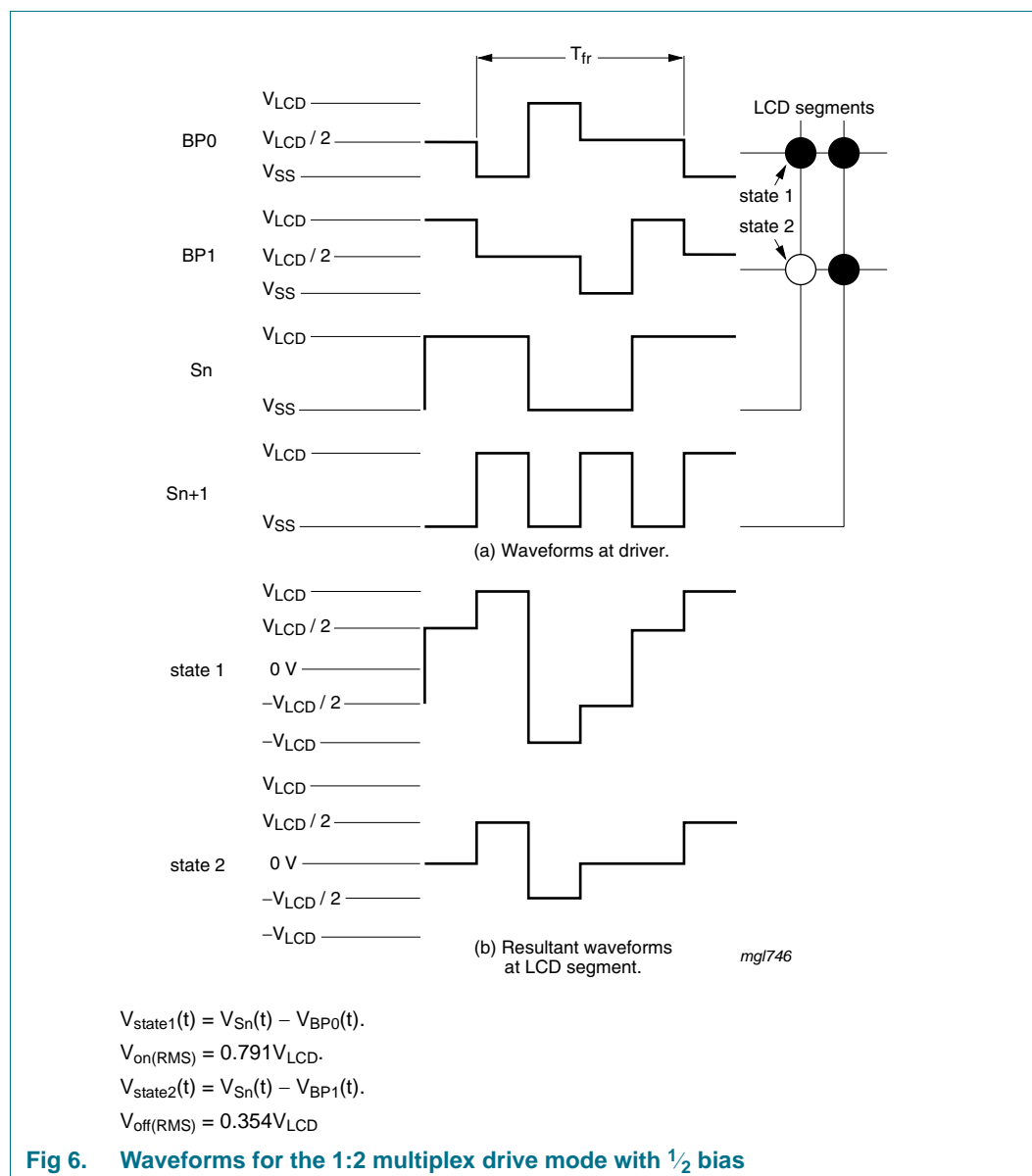
The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in [Figure 5](#).

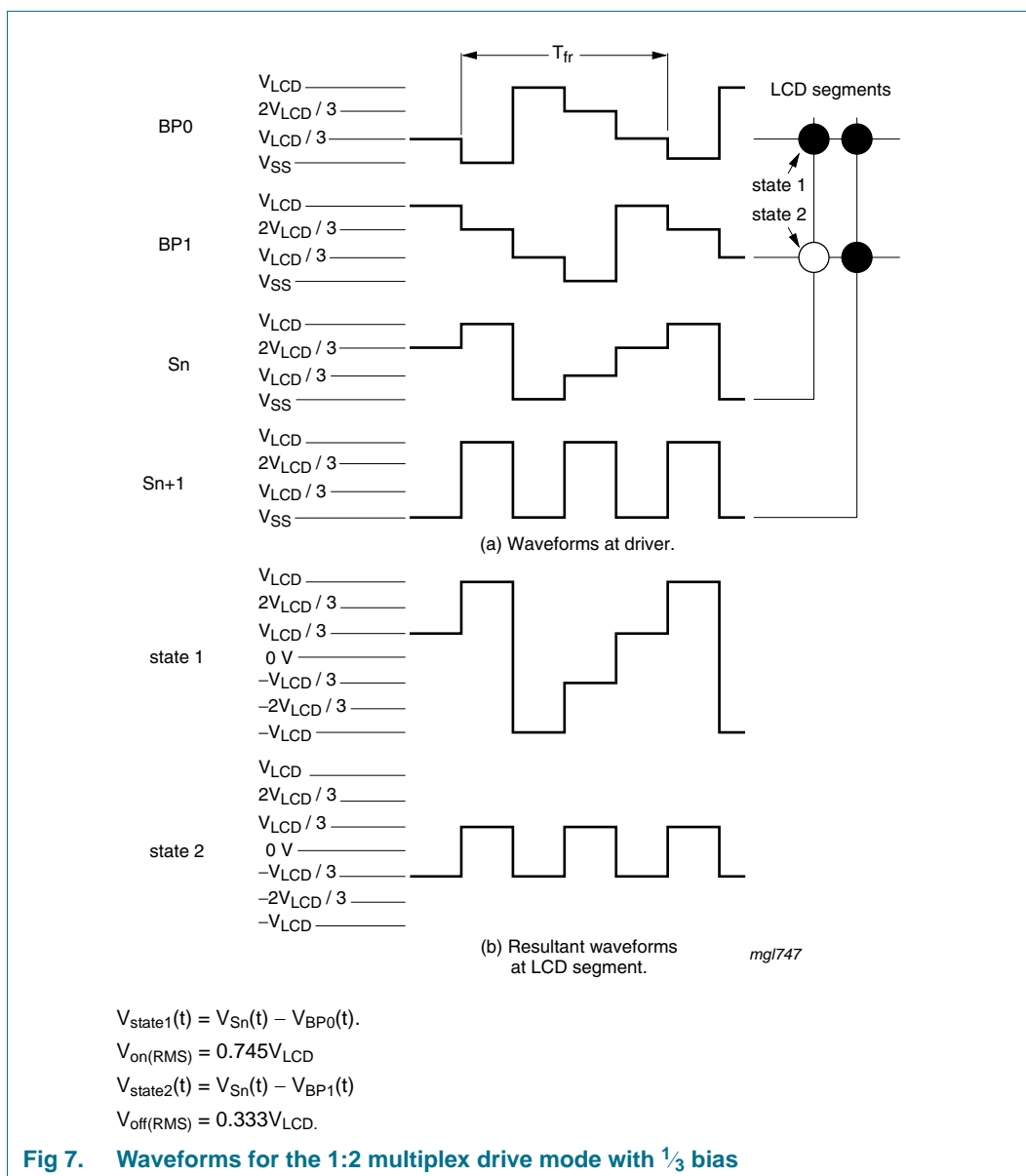


**Fig 5. Static drive mode waveforms**

### 7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA8576C allows the use of  $\frac{1}{2}$  bias or  $\frac{1}{3}$  bias (see [Figure 6](#) and [Figure 7](#)).

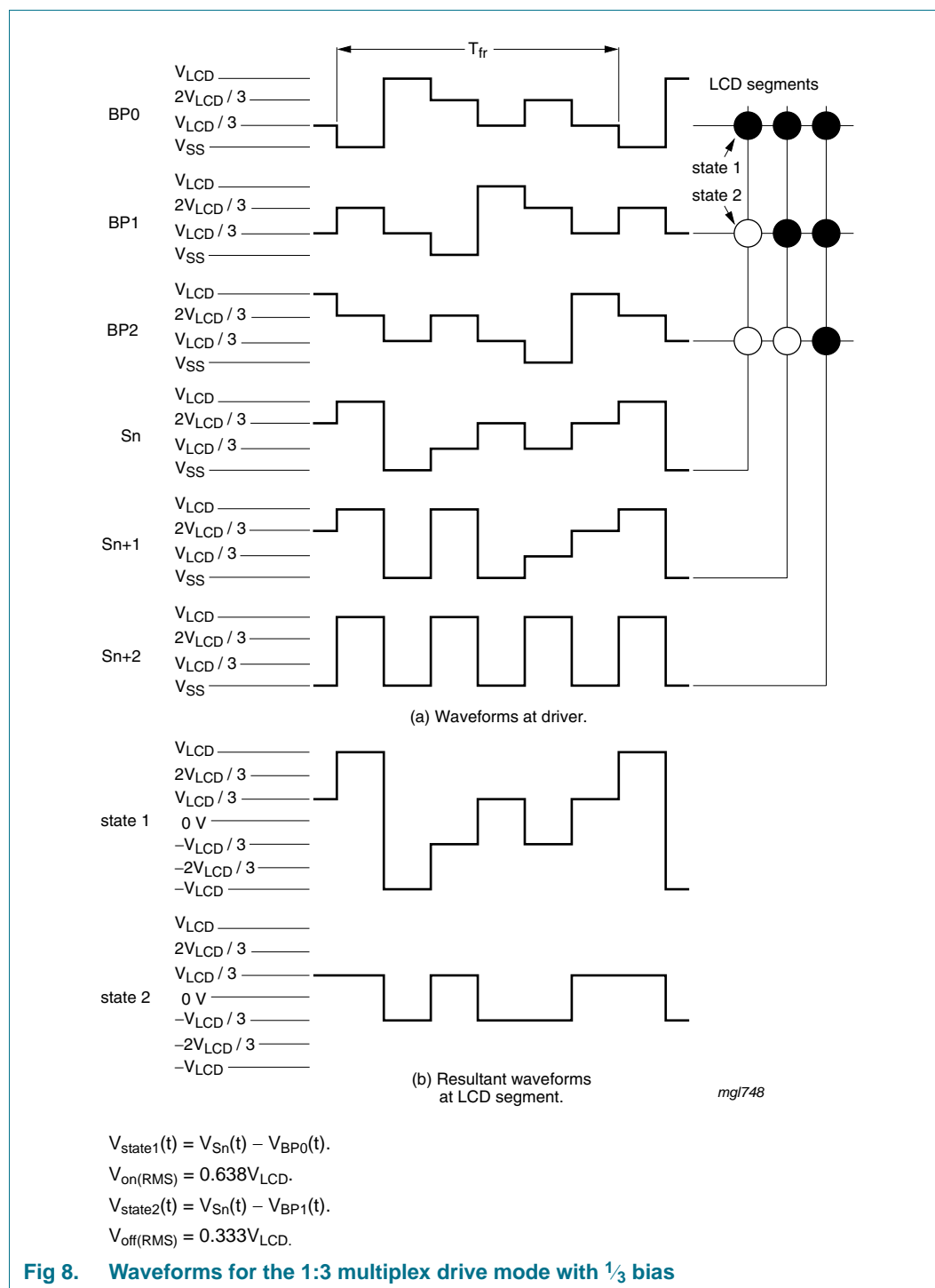




**Fig 7. Waveforms for the 1:2 multiplex drive mode with  $\frac{1}{3}$  bias**

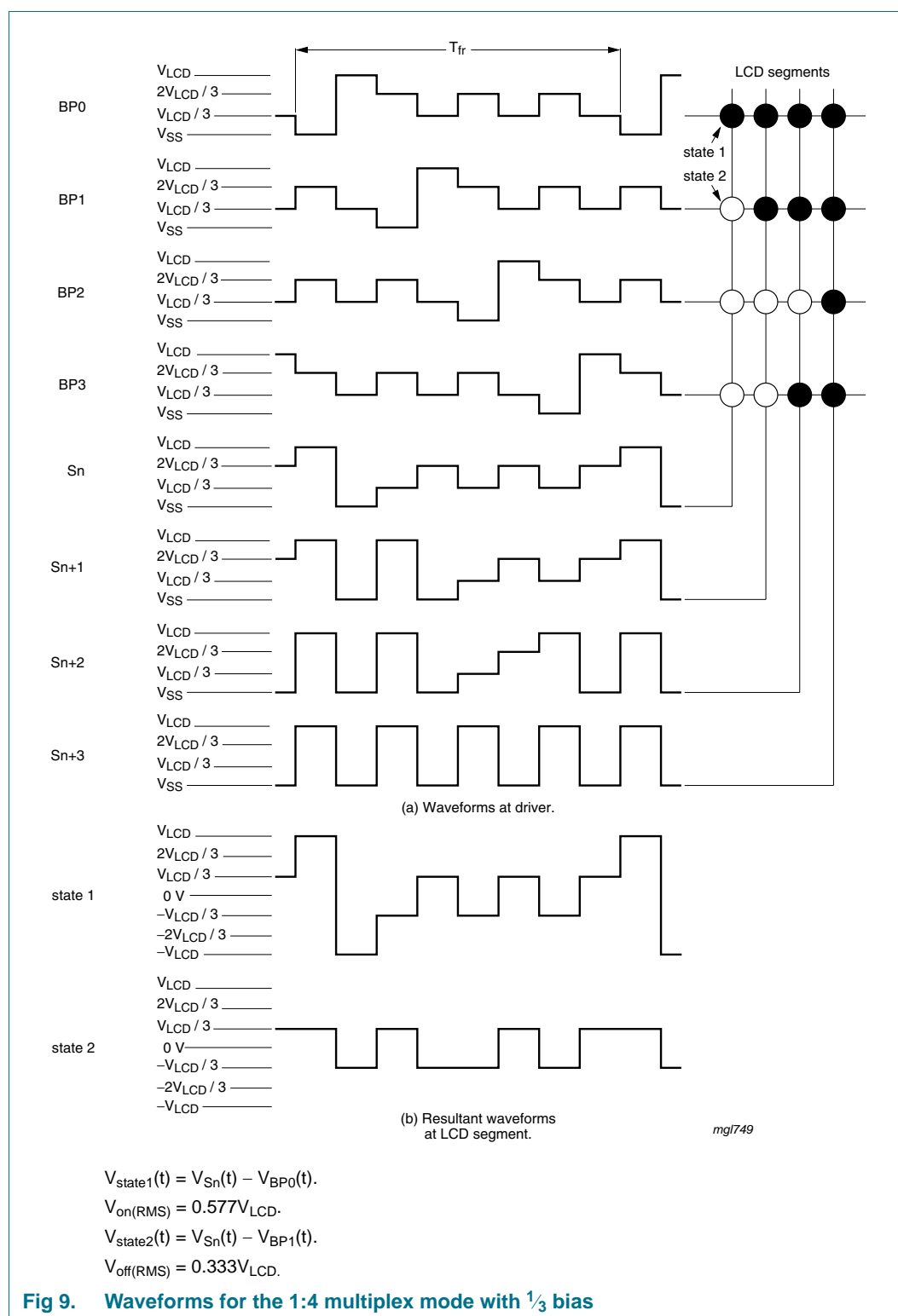
### 7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in [Figure 8](#).



### 7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in [Figure 9](#).



## 7.5 Oscillator

The internal logic and the LCD drive signals of the PCA8576C are timed by the frequency  $f_{clk}$ , which equals either the built-in oscillator frequency  $f_{osc}$  or the external clock frequency  $f_{clk(ext)}$ .

The clock frequency ( $f_{clk}$ ) determines the LCD frame frequency ( $f_{fr}$ ) and the maximum rate for data reception from the I<sup>2</sup>C-bus. To allow I<sup>2</sup>C-bus transmissions at their maximum data rate of 100 kHz,  $f_{clk}$  should be chosen to be above 125 kHz.

### 7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V<sub>SS</sub>. In this case, the output from pin CLK is the clock signal for any cascaded PCA8576C in the system.

### 7.5.2 External clock

Connecting pin OSC to V<sub>DD</sub> enables an external clock source. Pin CLK then becomes the external clock input.

**Remark:** A clock signal must always be supplied to the device. Removing the clock, freezes the LCD in a DC state, which is not suitable for the liquid crystal.

## 7.6 Timing

The timing of the PCA8576C sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal (SYNC) maintains the correct timing relationship between the PCA8576Cs in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see [Table 6](#)). The frame frequency is set by the mode-set command (see [Table 9](#)) when an internal clock is used or by the frequency applied to the pin CLK when an external clock is used.

**Table 6.** LCD frame frequencies [\[1\]](#)

PCA8576C mode	Frame frequency	Nominal frame frequency (Hz)
Normal-power mode	$f_{fr} = \frac{f_{clk}}{2880}$	69 <a href="#">[2]</a>
Power-saving mode	$f_{fr} = \frac{f_{clk}}{480}$	65 <a href="#">[3]</a>

[1] The possible values for  $f_{clk}$  see [Table 16](#).

[2] For  $f_{clk} = 200$  kHz.

[3] For  $f_{clk} = 31$  kHz.

The ratio between the clock frequency and the LCD frame frequency depends on the power mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power consumption.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I<sup>2</sup>C-bus. When a device is unable to process a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I<sup>2</sup>C-bus but no data loss occurs.

## 7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

## 7.8 Shift register

The shift register transfers display information from the display RAM to the display register while previous data is displayed.

## 7.9 Segment outputs

The LCD drive section includes 40 segment outputs, S0 to S39, which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

## 7.10 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

## 7.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map [Figure 10](#) shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

The diagram illustrates the mapping from Display RAM addresses to segment outputs and backplane outputs. It features a grid where rows represent Display RAM bits (0-3) and columns represent Display RAM addresses (0-9). The top row of the grid is labeled with segment outputs S0 through S9. To the left of the grid, labels indicate that rows correspond to display RAM bits and backplane outputs.

	0	1	2	3	4					35	36	37	38	39
0						_____	_____	_____	_____					
1						_____	_____	_____	_____					
2						_____	_____	_____	_____					
3						_____	_____	_____	_____					

*mbe525*

The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

**Fig 10. Display RAM bit map**

When display data is transmitted to the PCA8576C, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in [Figure 11](#); the RAM filling organization depicted applies equally to other LCD types.



drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte																																																																																																																																																																										
static			<p>columns display RAM address/segment outputs (s) byte1</p> <table><tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th><th>n + 4</th><th>n + 5</th><th>n + 6</th><th>n + 7</th></tr><tr><th>rows display RAM</th><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr><tr><th>rows/backplane outputs (BP)</th><td>0</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr></table>		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7	rows display RAM	c	b	a	f	g	e	d	DP	rows/backplane outputs (BP)	0	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	2	x	x	x	x	x	x	x	x	3	x	x	x	x	x	x	x	x	<p>MSB</p> <p>LSB</p> <table><tr><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr></table>	c	b	a	f	g	e	d	DP																																																																																																												
	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7																																																																																																																																																																						
rows display RAM	c	b	a	f	g	e	d	DP																																																																																																																																																																						
rows/backplane outputs (BP)	0	x	x	x	x	x	x	x																																																																																																																																																																						
1	x	x	x	x	x	x	x	x																																																																																																																																																																						
2	x	x	x	x	x	x	x	x																																																																																																																																																																						
3	x	x	x	x	x	x	x	x																																																																																																																																																																						
c	b	a	f	g	e	d	DP																																																																																																																																																																							
1:2 multiplex			<p>columns display RAM address/segment outputs (s) byte1</p> <table><tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th></tr><tr><th>rows display RAM</th><td>a</td><td>f</td><td>e</td><td>d</td></tr><tr><th>rows/backplane outputs (BP)</th><td>0</td><td>b</td><td>g</td><td>c</td></tr><tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td></tr></table> <p>byte2</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>		n	n + 1	n + 2	n + 3	rows display RAM	a	f	e	d	rows/backplane outputs (BP)	0	b	g	c	1	x	x	x	x	2	x	x	x	x	3	x	x	x	x																																					<p>MSB</p> <p>LSB</p> <table><tr><td>a</td><td>b</td><td>f</td><td>g</td><td>e</td><td>c</td><td>d</td><td>DP</td></tr></table>	a	b	f	g	e	c	d	DP																																																																																																
	n	n + 1	n + 2	n + 3																																																																																																																																																																										
rows display RAM	a	f	e	d																																																																																																																																																																										
rows/backplane outputs (BP)	0	b	g	c																																																																																																																																																																										
1	x	x	x	x																																																																																																																																																																										
2	x	x	x	x																																																																																																																																																																										
3	x	x	x	x																																																																																																																																																																										
a	b	f	g	e	c	d	DP																																																																																																																																																																							
1:3 multiplex			<p>columns display RAM address/segment outputs (s) byte1</p> <table><tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th></tr><tr><th>rows display RAM</th><td>b</td><td>a</td><td>f</td></tr><tr><th>rows/backplane outputs (BP)</th><td>0</td><td>DP</td><td>d</td></tr><tr><td>1</td><td>c</td><td>g</td><td>x</td></tr><tr><td>2</td><td>x</td><td>x</td><td>x</td></tr><tr><td>3</td><td>x</td><td>x</td><td>x</td></tr></table> <p>byte2</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>byte3</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>		n	n + 1	n + 2	rows display RAM	b	a	f	rows/backplane outputs (BP)	0	DP	d	1	c	g	x	2	x	x	x	3	x	x	x																																																																									<p>MSB</p> <p>LSB</p> <table><tr><td>b</td><td>DP</td><td>c</td><td>a</td><td>d</td><td>g</td><td>f</td><td>e</td></tr></table>	b	DP	c	a	d	g	f	e																																																																		
	n	n + 1	n + 2																																																																																																																																																																											
rows display RAM	b	a	f																																																																																																																																																																											
rows/backplane outputs (BP)	0	DP	d																																																																																																																																																																											
1	c	g	x																																																																																																																																																																											
2	x	x	x																																																																																																																																																																											
3	x	x	x																																																																																																																																																																											
b	DP	c	a	d	g	f	e																																																																																																																																																																							
1:4 multiplex			<p>columns display RAM address/segment outputs (s) byte1</p> <table><tr><th></th><th>n</th><th>n + 1</th></tr><tr><th>rows display RAM</th><td>a</td><td>f</td></tr><tr><th>rows/backplane outputs (BP)</th><td>0</td><td>c</td></tr><tr><td>1</td><td>b</td><td>e</td></tr><tr><td>2</td><td>DP</td><td>g</td></tr><tr><td>3</td><td>DP</td><td>d</td></tr></table> <p>byte2</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>byte3</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>byte4</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>byte5</p> <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>		n	n + 1	rows display RAM	a	f	rows/backplane outputs (BP)	0	c	1	b	e	2	DP	g	3	DP	d																																																																																																																																																	<p>MSB</p> <p>LSB</p> <table><tr><td>a</td><td>c</td><td>b</td><td>DP</td><td>f</td><td>e</td><td>g</td><td>d</td></tr></table>	a	c	b	DP	f	e	g	d
	n	n + 1																																																																																																																																																																												
rows display RAM	a	f																																																																																																																																																																												
rows/backplane outputs (BP)	0	c																																																																																																																																																																												
1	b	e																																																																																																																																																																												
2	DP	g																																																																																																																																																																												
3	DP	d																																																																																																																																																																												
a	c	b	DP	f	e	g	d																																																																																																																																																																							

001aa|646

x = data bit unchanged.

Fig 11. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I<sup>2</sup>C-bus

The following applies to [Figure 11](#):

- In the static drive mode, the eight transmitted data bits are placed in row 0 of eight successive 4-bit RAM words.
- In the 1:2 multiplex mode, the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In the 1:3 multiplex mode, the eight bits are placed in triples into row 0, 1, and 2 to three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of two successive 4-bit RAM words.

## 7.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see [Table 10](#)). After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see [Figure 11](#)). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I<sup>2</sup>C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

## 7.13 Sub-address counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see [Table 11](#)). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is blocked but the data pointer will be incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

## 7.14 Bank selector

### 7.14.1 Output bank selector

The output bank selector (see [Table 12](#)), selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of row 0 are selected, followed sequentially by the contents of row 1, row 2, and then row 3.
- In 1:3 multiplex mode: rows 0, 1, and 2 are selected sequentially.
- In 1:2 multiplex mode: rows 0 and 1 are selected.
- In the static mode: row 0 is selected.

The PCA8576C includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In 1:2 multiplex drive mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

### 7.14.2 Input bank selector

The input bank selector (see [Table 12](#)) loads display data into the display RAM based on the selected LCD drive configuration. Using the bank-select command, display data can be loaded in row 2 into static drive mode or in rows 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently of the output bank selector.

## 7.15 Blinker

The display blinking capabilities of the PCA8576C are very versatile. The whole display can be blinked at frequencies selected by the blink-select command. The blinking frequencies are integer fractions of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see [Table 7](#)).

**Table 7. Blink frequencies**

Blinking mode	Normal-power mode ratio	Power-saving mode ratio	Blink frequency
off	-	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{92160}$	$f_{blink} = \frac{f_{clk}}{15360}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{184320}$	$f_{blink} = \frac{f_{clk}}{30720}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{368640}$	$f_{blink} = \frac{f_{clk}}{61440}$	0.5 Hz

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink-select command (see [Table 13](#)).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display needs to be blinked at a frequency other than the nominal blink frequency, this can be done using the mode-set command to set and reset the display enable bit E at the required rate (see [Table 9](#)).

## 7.16 Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in [Figure 12](#).

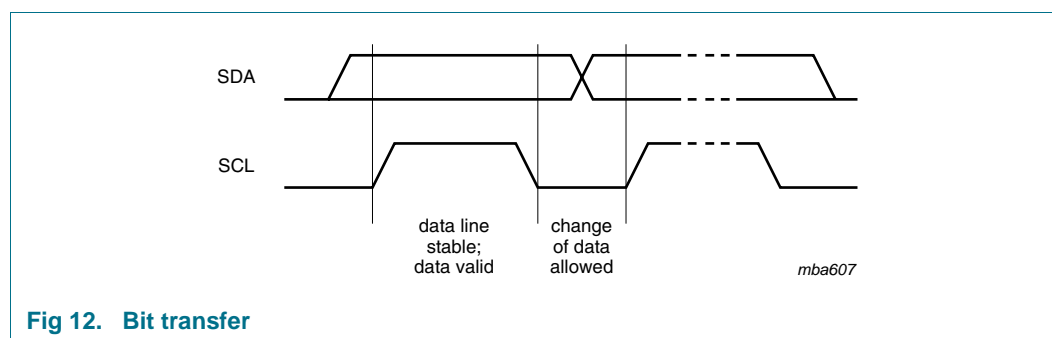


Fig 12. Bit transfer

### 7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in [Figure 13](#).

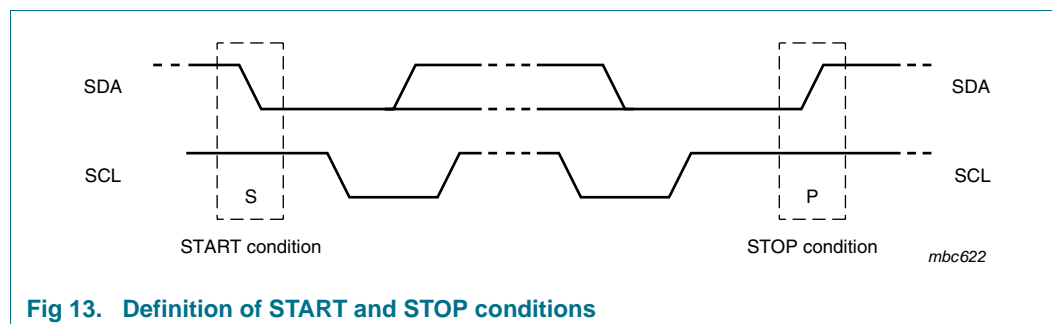


Fig 13. Definition of START and STOP conditions

### 7.16.3 System configuration

A device generating a message is a transmitter and a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is illustrated in [Figure 14](#).

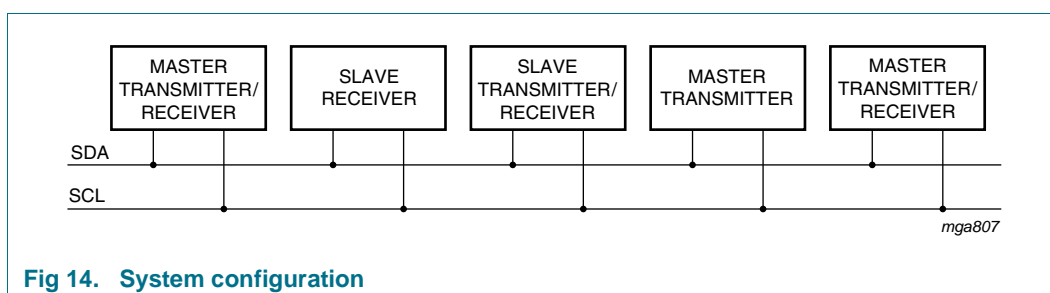


Fig 14. System configuration

### 7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I<sup>2</sup>C-bus is illustrated in [Figure 15](#).

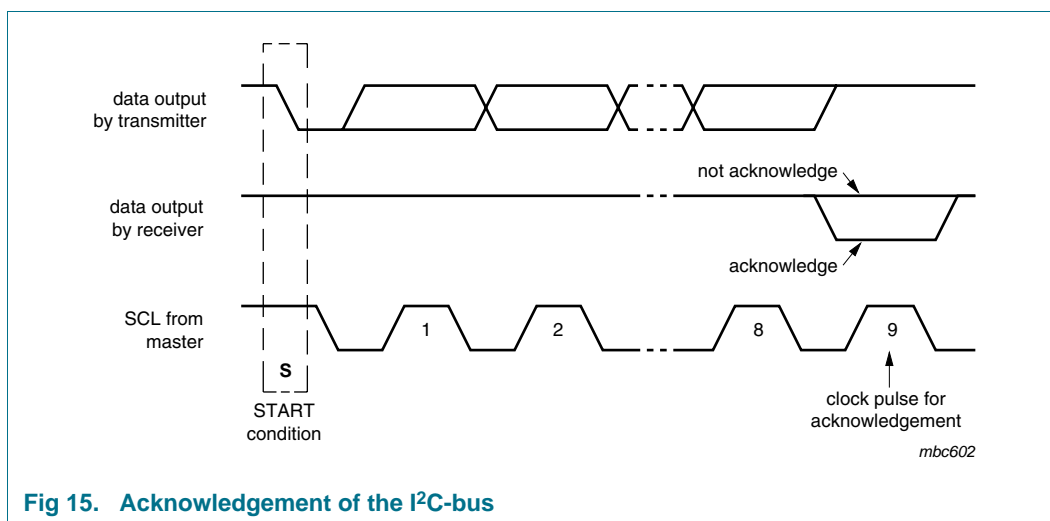


Fig 15. Acknowledgement of the I<sup>2</sup>C-bus

### 7.16.5 PCA8576C I<sup>2</sup>C-bus controller

The PCA8576C acts as an I<sup>2</sup>C-bus slave receiver. It does not initiate I<sup>2</sup>C-bus transfers or transmit data to an I<sup>2</sup>C-bus master receiver. The only data output from the PCA8576C are the acknowledge signals of the selected devices. Device selection depends on the I<sup>2</sup>C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1, and A2 are normally tied to V<sub>SS</sub> which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V<sub>SS</sub> or V<sub>DD</sub> using a binary coding scheme so that no two devices with a common I<sup>2</sup>C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCA8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCA8576C forces the SCL line LOW until its internal operations are completed. This is known as the clock synchronization feature of the I<sup>2</sup>C-bus and serves to slow down fast transmitters. Data loss does not occur.

### 7.16.6 Input filter

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

## 7.17 I<sup>2</sup>C-bus protocol

Two I<sup>2</sup>C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA8576C. The least significant bit of the slave address that a PCA8576C responds to is defined by the level tied at its input SA0. Therefore, two types of PCA8576C can be distinguished on the same I<sup>2</sup>C-bus which allows:

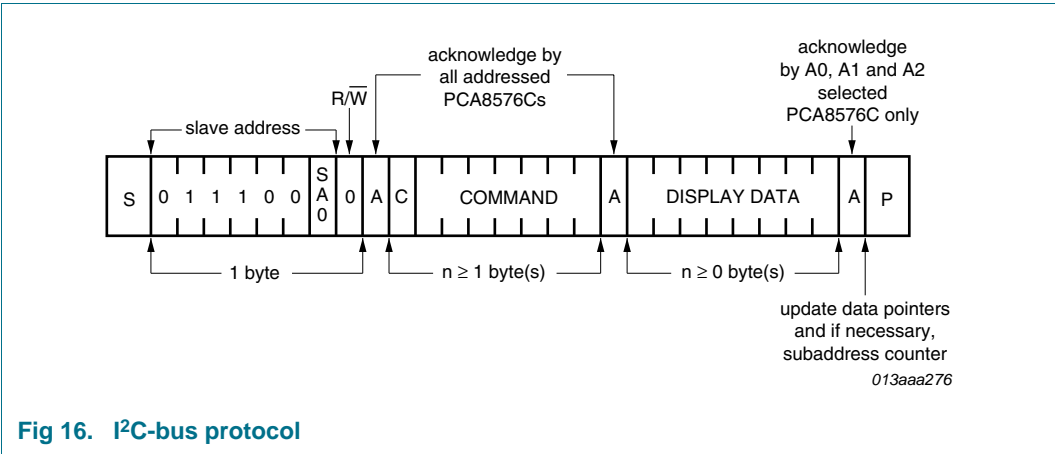
- Up to 16 PCA8576Cs on the same I<sup>2</sup>C-bus for very large LCD applications.
- The use of two types of LCD multiplex on the same I<sup>2</sup>C-bus.

The I<sup>2</sup>C-bus protocol is shown in [Figure 16](#). The sequence is initiated with a START condition (S) from the I<sup>2</sup>C-bus master which is followed by one of the two PCA8576C slave addresses available. All PCA8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCA8576Cs with the alternative SA0 level ignore the whole I<sup>2</sup>C-bus transfer.

After acknowledgement, one or more command bytes follow which define the status of the addressed PCA8576Cs.

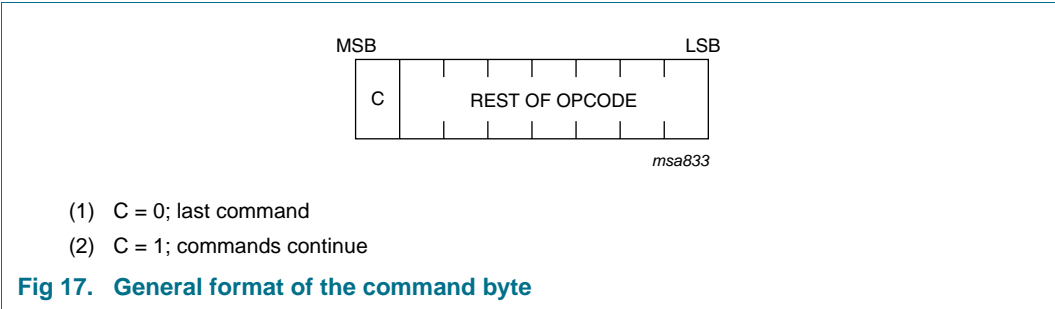
The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCA8576Cs on the bus.

After the last command byte, a series of display data bytes may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCA8576C device. The acknowledgement after each byte is made only by the (A0, A1, and A2) addressed PCA8576C. After the last display byte, the I<sup>2</sup>C-bus master issues a STOP condition (P).



### 7.18 Command decoder

The command decoder identifies command bytes that arrive on the I<sup>2</sup>C-bus. All available commands carry a continuation bit C in their most significant bit position as shown in [Figure 17](#). When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.



The five commands available to the PCA8576C are defined in [Table 8](#).

Table 8. Definition of PCA8576C commands

Command	Operation Code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	C	1	0	LP	E	B	M[1:0]		<a href="#">Section 7.18.1</a>
load-data-pointer	C	0	P[5:0]						<a href="#">Section 7.18.2</a>
device-select	C	1	1	0	0	A[2:0]			<a href="#">Section 7.18.3</a>
bank-select	C	1	1	1	1	0	I	O	<a href="#">Section 7.18.4</a>
blink-select	C	1	1	1	0	AB	BF[1:0]		<a href="#">Section 7.18.5</a>

### 7.18.1 Mode-set command

Table 9. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see <a href="#">Figure 17</a>
6 to 5	-	10	fixed value
4	LP		<b>power dissipation</b> (see <a href="#">Table 6</a> )
		0	normal-power mode
		1	power-saving mode
3	E		<b>display status</b>
		0	disabled <sup>[1]</sup>
		1	enabled
2	B		<b>LCD bias configuration</b> <sup>[2]</sup>
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		<b>LCD drive mode selection</b>
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Bit B is not applicable for the static LCD drive mode.

### 7.18.2 Load-data-pointer command

Table 10. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see <a href="#">Figure 17</a>
6	-	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses



### 7.18.3 Device-select command

Table 11. Device-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see <a href="#">Figure 17</a>
6 to 4	-	1100	fixed value
3 to 0	A[2:0]	000 to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

### 7.18.4 Bank-select command

Table 12. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	1:2 multiplex <sup>[1]</sup>
7	C	0, 1	see <a href="#">Figure 17</a>	
6 to 2	-	11110	fixed value	
1	I		<b>input bank selection</b> ; storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		<b>output bank selection</b> ; retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

### 7.18.5 Blink-select command

Table 13. Blink-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see <a href="#">Figure 17</a>
6 to 3	-	1110	fixed value
2	AB		<b>blink mode selection</b>
		0	normal blinking <sup>[1]</sup>
		1	alternate RAM bank blinking <sup>[2]</sup>
1 to 0	BF[1:0]		<b>blink frequency selection</b>
		00	off
		01	1
		10	2
		11	3

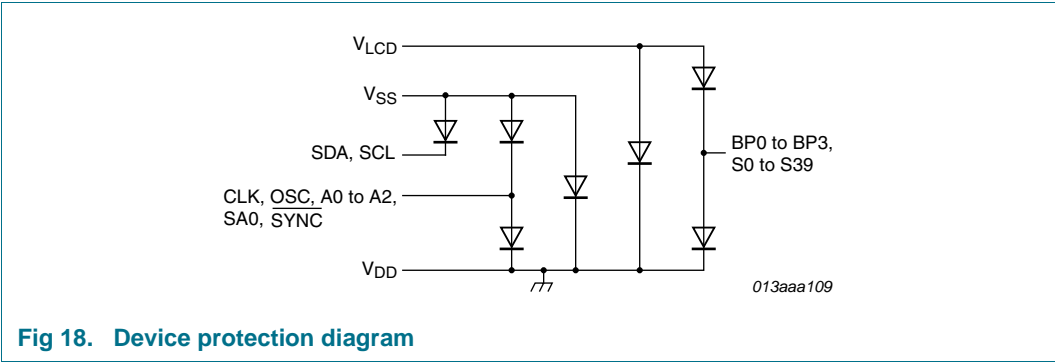
[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

## 7.19 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCA8576C and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

8. Internal circuitry



## 9. Limiting values

### CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage ( $V_{LCD}$ ) is on while the IC supply voltage ( $V_{DD}$ ) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts,  $V_{LCD}$  and  $V_{DD}$  must be applied or removed together.

**Table 14. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+8.0	V
$V_{LCD}$	LCD supply voltage		[1] $V_{DD} - 8.0$	$V_{DD}$	V
$V_I$	input voltage	on each of the pins SCL, SDA, CLK, SYNC, SA0, OSC and A0 to A2	-0.5	+8.0	V
$V_O$	output voltage	on each of the pins S0 to S39 and BP0 to BP3	[1] -0.5	+8.0	V
$I_I$	input current		-20	+20	mA
$I_O$	output current		-25	+25	mA
$I_{DD}$	supply current		-50	+50	mA
$I_{SS}$	ground supply current		-50	+50	mA
$I_{DD(LCD)}$	LCD supply current		-50	+50	mA
$P_{tot}$	total power dissipation		-	400	mW
$P_o$	output power		-	100	mW
$V_{ESD}$	electrostatic discharge voltage	HBM	[2] -	±4000	V
		MM	[3] -	±200	V
		CDM	[4]		
		all pins	-	500	V
		corner pins	-	1000	V
$I_{lu}$	latch-up current		[5] -	150	mA
$T_{stg}$	storage temperature		[6] -65	+150	°C
$T_{amb}$	ambient temperature	operating device	-40	+85	°C

[1] Values with respect to  $V_{DD}$ .

[2] Pass level; Human Body Model (HBM), according to [Ref. 5 "JESD22-A114"](#).

[3] Pass level; Machine Model (MM), according to [Ref. 6 "JESD22-A115"](#).

[4] Pass level; Charged-Device Model (CDM), according to [Ref. 7 "JESD22-C101"](#).

[5] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature ( $T_{amb(max)}$ ).

[6] According to the NXP store and transport requirements (see [Ref. 9 "NX3-00092"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

## 10. Static characteristics

**Table 15. Static characteristics**

$V_{DD} = 2.0\text{ V to }6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = V_{DD} - 6.0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		2.0	-	6.0	V
$V_{LCD}$	LCD supply voltage		[1] $V_{DD} - 6.0$	-	$V_{DD} - 2.0$	V
$I_{DD}$	supply current:	$f_{clk} = 200\text{ kHz}$	[2] -	-	120	$\mu\text{A}$
$I_{DD(lp)}$	low-power mode supply current	$V_{DD} = 3.5\text{ V}$ ; $V_{LCD} = 0\text{ V}$ ; $f_{clk} = 35\text{ kHz}$ ; A0, A1 and A2 connected to $V_{SS}$	-	-	60	$\mu\text{A}$
<b>Logic</b>						
$V_{IL}$	LOW-level input voltage	on pins CLK, $\overline{\text{SYNC}}$ , OSC, A0 to A2 and SA0	$V_{SS}$	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage	on pins CLK, $\overline{\text{SYNC}}$ , OSC, A0 to A2 and SA0	$0.7V_{DD}$	-	$V_{DD}$	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 0\text{ mA}$	-	-	0.05	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 0\text{ mA}$	$V_{DD} - 0.05$	-	-	V
$I_{OL}$	LOW-level output current	output sink current; $V_{OL} = 1.0\text{ V}$ ; $V_{DD} = 5.0\text{ V}$ ; on pins CLK and $\overline{\text{SYNC}}$	1	-	-	mA
$I_L$	leakage current	$V_I = V_{DD}$ or $V_{SS}$ ; on pins CLK, SCL, SDA, A0 to A2 and SA0	-1	-	+1	$\mu\text{A}$
$I_{L(OSC)}$	leakage current on pin OSC	$V_I = V_{DD}$	-1	-	+1	$\mu\text{A}$
$I_{pd}$	pull-down current	$V_I = 1.0\text{ V}$ ; $V_{DD} = 5.0\text{ V}$ ; on pins A0 to A2 and OSC	15	50	150	$\mu\text{A}$
$R_{\overline{\text{SYNC}}_N}$	$\overline{\text{SYNC}}$ resistance		20	50	150	$\text{k}\Omega$
$V_{POR}$	power-on reset voltage		[3] -	1.0	1.6	V
$C_I$	input capacitance		[4] -	-	7	pF
<b>I<sup>2</sup>C-bus; pins SDA and SCL</b>						
$V_{IL}$	LOW-level input voltage		$V_{SS}$	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	6.0	V
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; $V_{OH} = 4.0\text{ V}$ ; $V_{DD} = 5.0\text{ V}$	1	-	-	mA
$I_{OL(SDA)}$	LOW-level output current on pin SDA	output sink current; $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 5.0\text{ V}$	3	-	-	mA

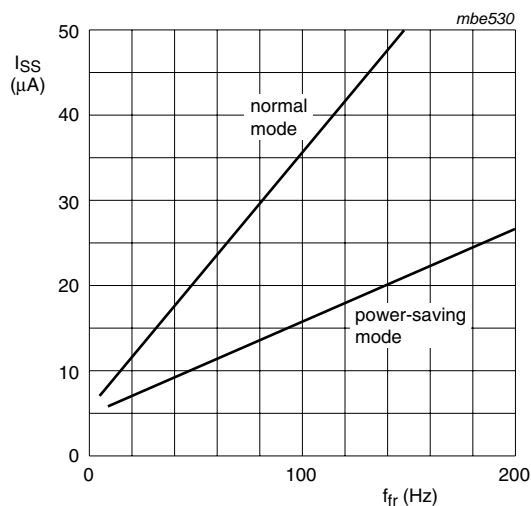
**Table 15. Static characteristics ...continued**

$V_{DD} = 2.0\text{ V}$  to  $6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = V_{DD} - 6.0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>LCD outputs</b>						
$V_{BP}$	voltage on pin BP	$C_{bpl} = 35\text{ nF}$ ; on pins BP0 to BP3	-20	-	+20	mV
$V_S$	voltage on pin S	$C_{sgm} = 5\text{ nF}$ ; on pins S0 to S39	-20	-	+20	mV
$R_{BP}$	resistance on pin BP	$V_{LCD} = V_{DD} - 5\text{ V}$ ; on pins BP0 to BP3 [5]	-	-	5	k $\Omega$
$R_S$	resistance on pin S	$V_{LCD} = V_{DD} - 5\text{ V}$ ; on pins S0 to S39 [5]	-	-	7.5	k $\Omega$

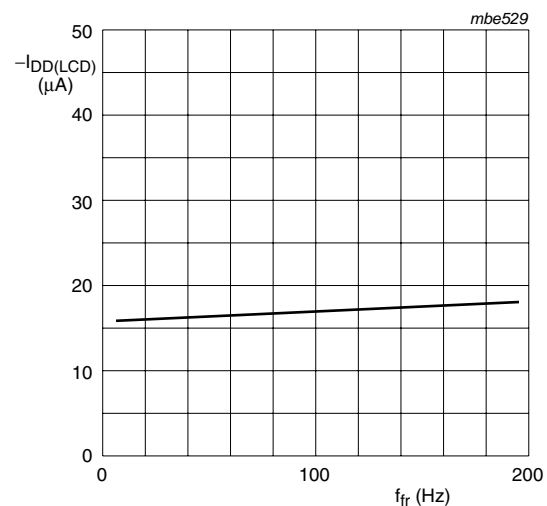
- [1]  $V_{LCD} \leq V_{DD} - 3\text{ V}$  for  $\frac{1}{3}$  bias.  
 [2] LCD outputs are open-circuit; inputs at  $V_{SS}$  or  $V_{DD}$ ; external clock with 50 % duty factor; I<sup>2</sup>C-bus inactive.  
 [3] Resets all logic when  $V_{DD} < V_{POR}$ .  
 [4] Periodically sampled, not 100 % tested.  
 [5] Outputs measured one at a time.

## 10.1 Typical supply current characteristics



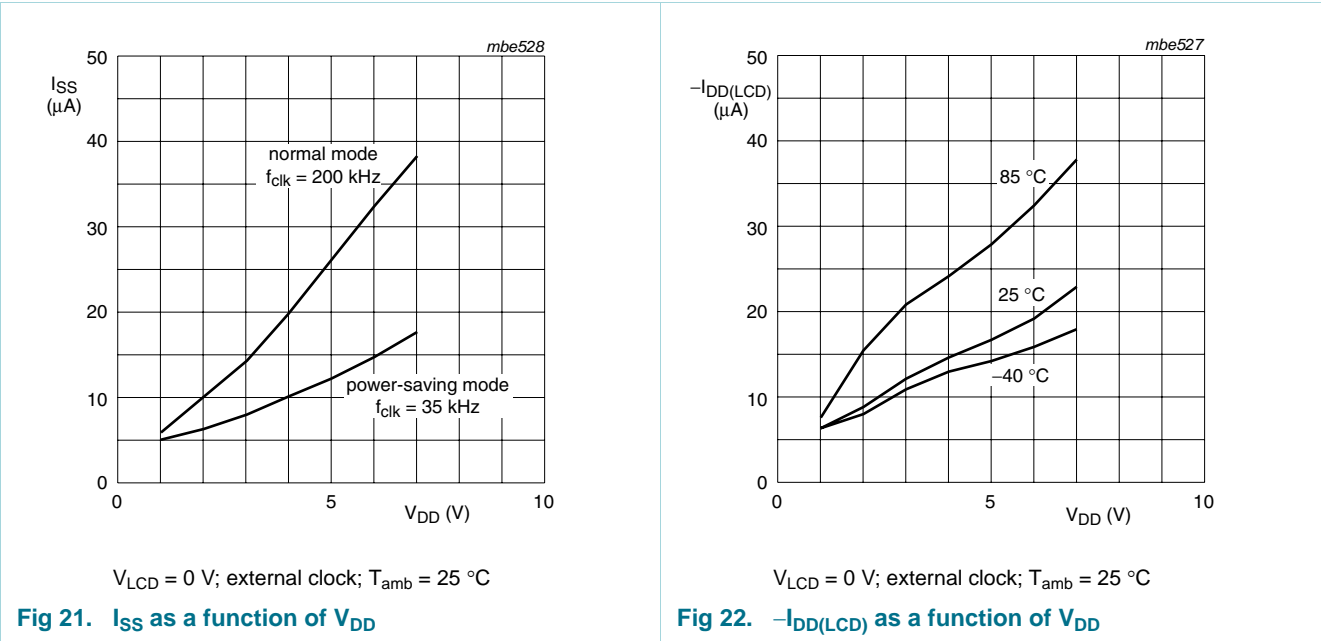
$V_{DD} = 5\text{ V}$ ;  $V_{LCD} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

**Fig 19.  $I_{SS}$  as a function of  $f_{fr}$**

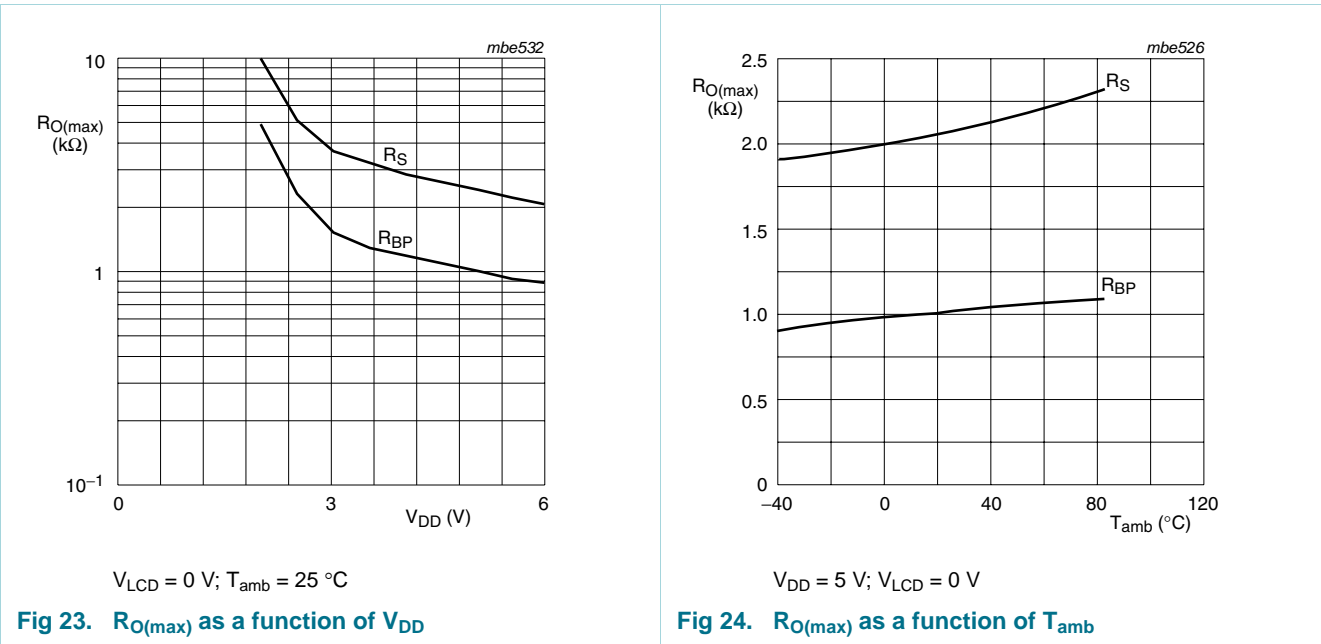


$V_{DD} = 5\text{ V}$ ;  $V_{LCD} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

**Fig 20.  $-I_{DD(LCD)}$  as a function of  $f_{fr}$**



10.2 Typical LCD output characteristics



## 11. Dynamic characteristics

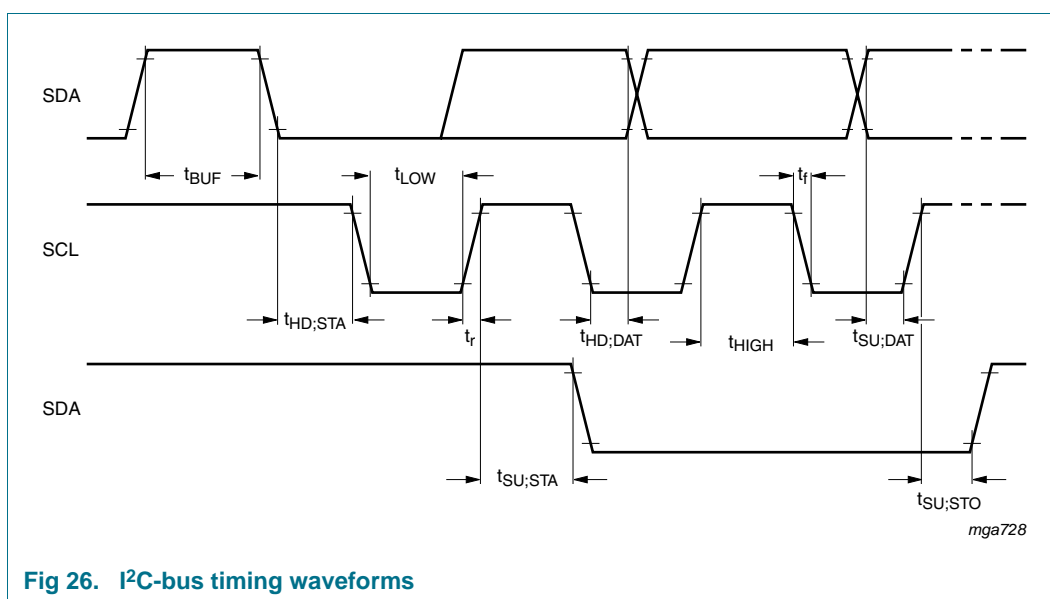
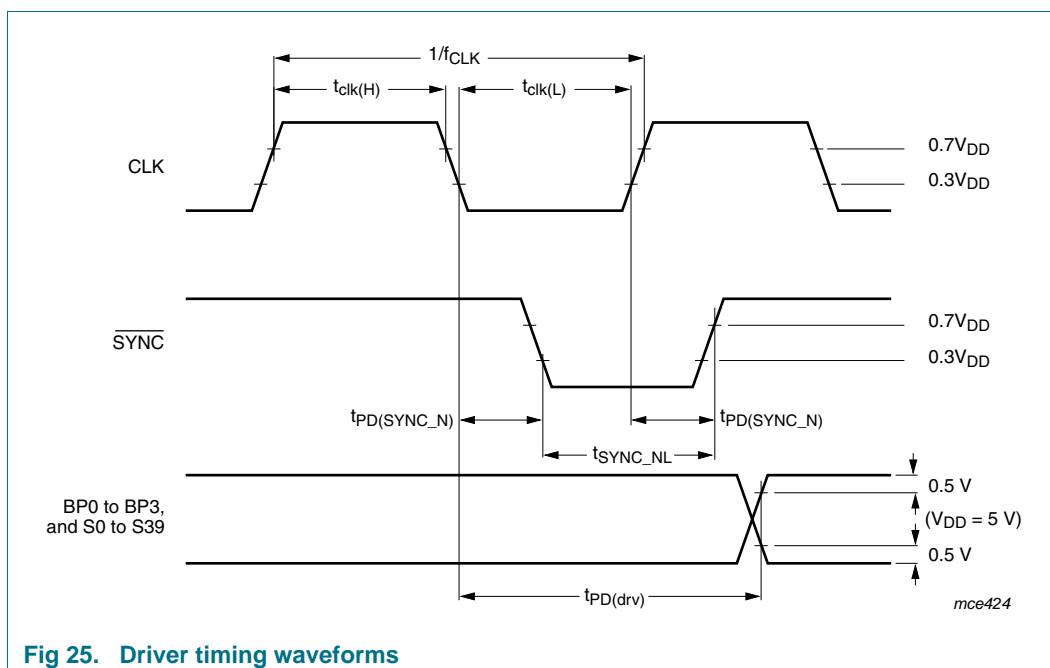
**Table 16. Dynamic characteristics**

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = 2.5\text{ V to }6.5\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Timing characteristics: driver timing waveforms (see Figure 25)</b>						
$f_{clk}$	clock frequency	normal-power mode; [1] $V_{DD} = 5\text{ V}$	125	200	315	kHz
		power-saving mode; $V_{DD} = 3\text{ V}$	21	31	48	kHz
$t_{clk(H)}$	clock HIGH time		1	-	-	$\mu\text{s}$
$t_{clk(L)}$	clock LOW time		1	-	-	$\mu\text{s}$
$t_{PD(SYNC\_N)}$	$\overline{\text{SYNC}}$ propagation delay		-	-	400	ns
$t_{SYNC\_NL}$	$\overline{\text{SYNC}}$ LOW time		1	-	-	$\mu\text{s}$
$t_{PD(drv)}$	driver propagation delay	$V_{LCD} = 5\text{ V}$	-	-	30	$\mu\text{s}$
<b>Timing characteristics: I<sup>2</sup>C-bus (see Figure 26)</b> [2]						
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	-	$\mu\text{s}$
$t_{HD,STA}$	hold time (repeated) START condition		4.0	-	-	$\mu\text{s}$
$t_{SU,STA}$	set-up time for a repeated START condition		4.7	-	-	$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		4.7	-	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	-	$\mu\text{s}$
$t_r$	rise time of both SDA and SCL signals		-	-	1	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals		-	-	0.3	$\mu\text{s}$
$C_b$	capacitive load for each bus line		-	-	400	pF
$t_{SU,DAT}$	data set-up time		250	-	-	ns
$t_{HD,DAT}$	data hold time		0	-	-	ns
$t_{SU,STO}$	set-up time for STOP condition		4.0	-	-	$\mu\text{s}$

[1]  $f_{clk} < 125\text{ kHz}$ , I<sup>2</sup>C-bus maximum transmission speed is derated.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .





## 12. Application information

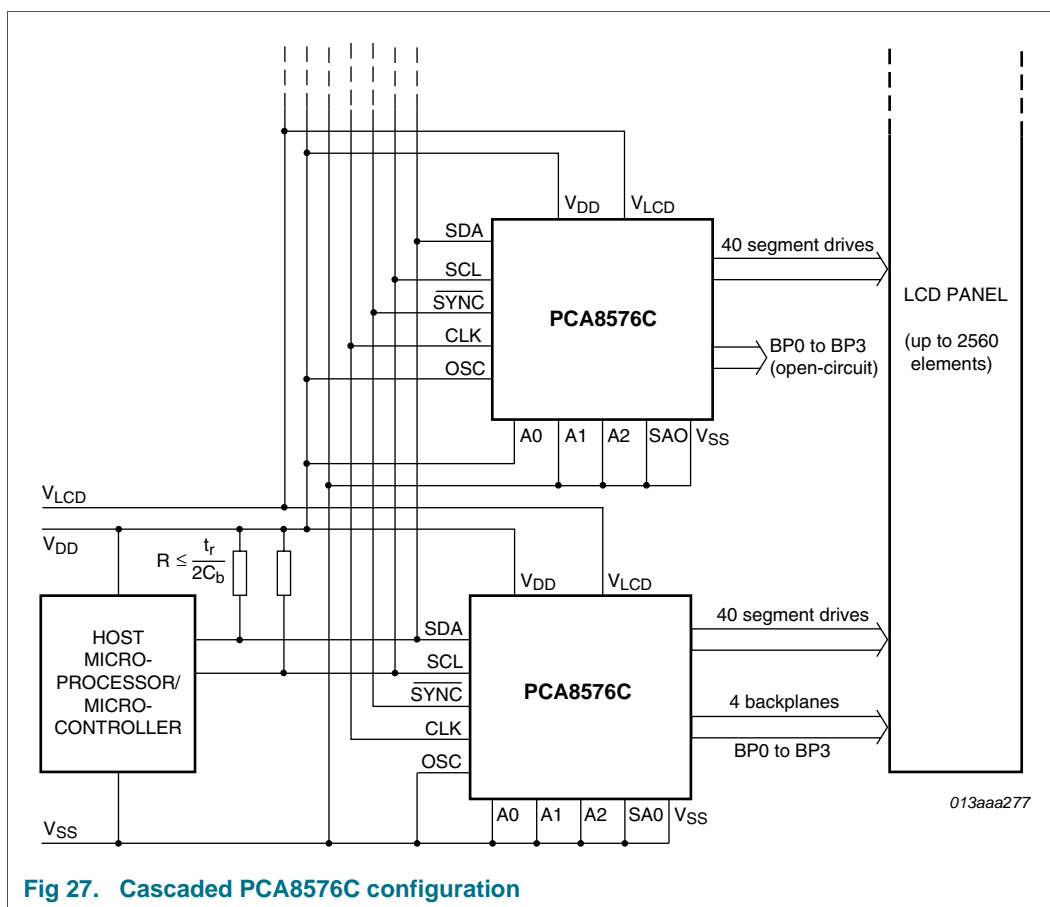
### 12.1 Cascaded operation

In large display configurations, up to 16 PCA8576Cs can be recognized on the same I<sup>2</sup>C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I<sup>2</sup>C-bus slave address (SA0).

**Table 17. Addressing cascaded PCA8576C**

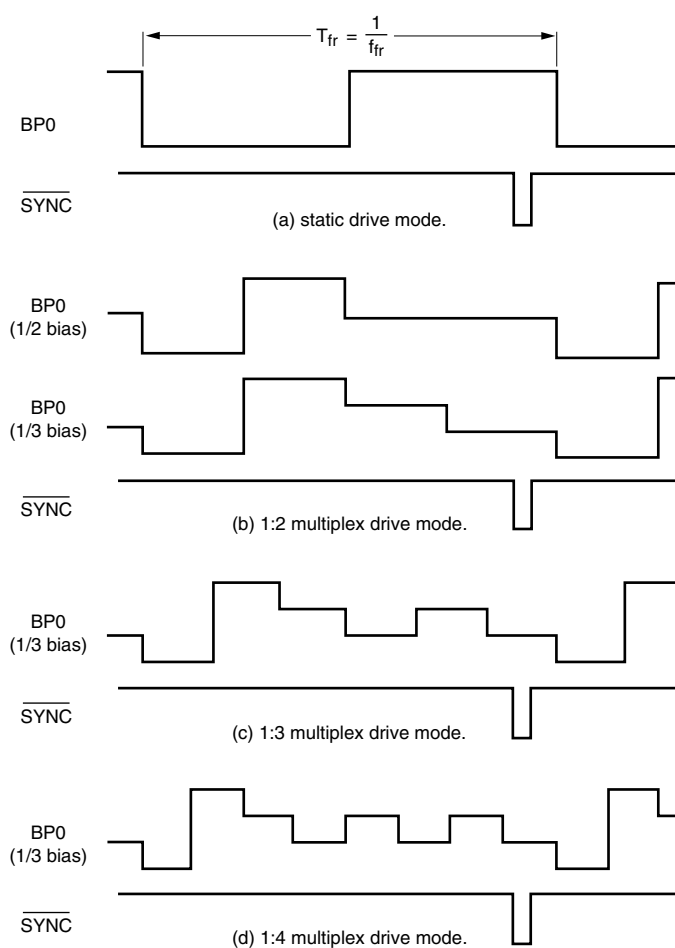
Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

Cascaded PCA8576Cs are synchronized. They can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCA8576Cs of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see [Figure 27](#)).



The SYNC line is provided to maintain the correct synchronization between all cascaded PCA8576Cs. This synchronization is guaranteed after the power-on reset. The only time that SYNC is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the defining a multiplex mode when PCA8576Cs with differing SA0 levels are cascaded).

SYNC is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCA8576C asserts the SYNC line and monitors the SYNC line at all other times. If synchronization in the cascade is lost, it is restored by the first PCA8576C to assert SYNC. The timing relationship between the backplane waveforms and the SYNC signal for the various drive modes of the PCA8576C are shown in [Figure 28](#).



mgl755

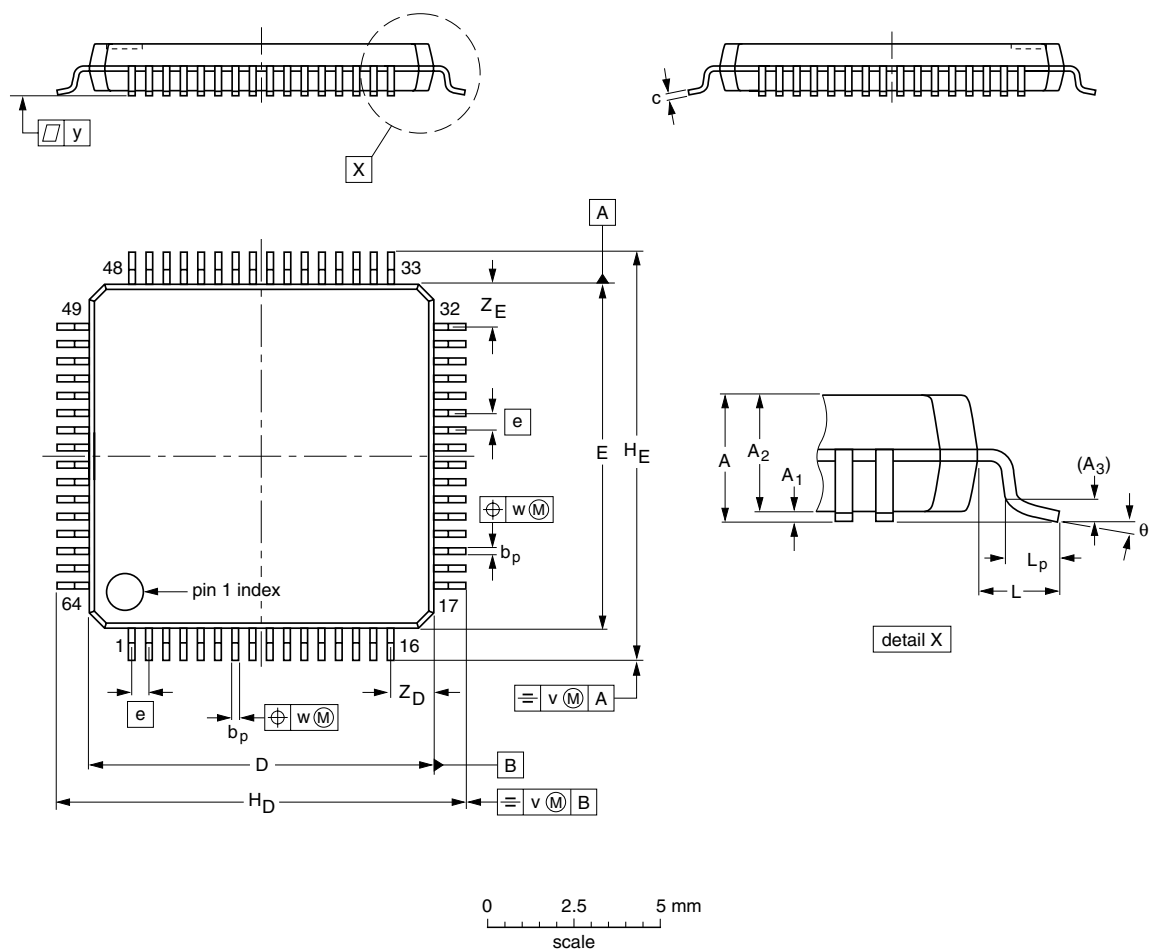
Excessive capacitive coupling between SCL or CLK and  $\overline{\text{SYNC}}$  will cause erroneous synchronization. If this is a problem you can increase the capacitance of the  $\overline{\text{SYNC}}$  line (e.g. by an external capacitor between  $\overline{\text{SYNC}}$  and  $V_{DD}$ .) Degradation of the positive edge of the  $\overline{\text{SYNC}}$  pulse can be countered by an external pull-up resistor.

**Fig 28. Synchronization of the cascade for the various PCA8576C drive modes**

13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>P</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>P</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

**Note**  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				00-01-19 03-02-25

Fig 29. Package outline SOT314-2 (LQFP64) of PCA8576CH

## 14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 30](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

**Table 18. SnPb eutectic process (from J-STD-020C)**

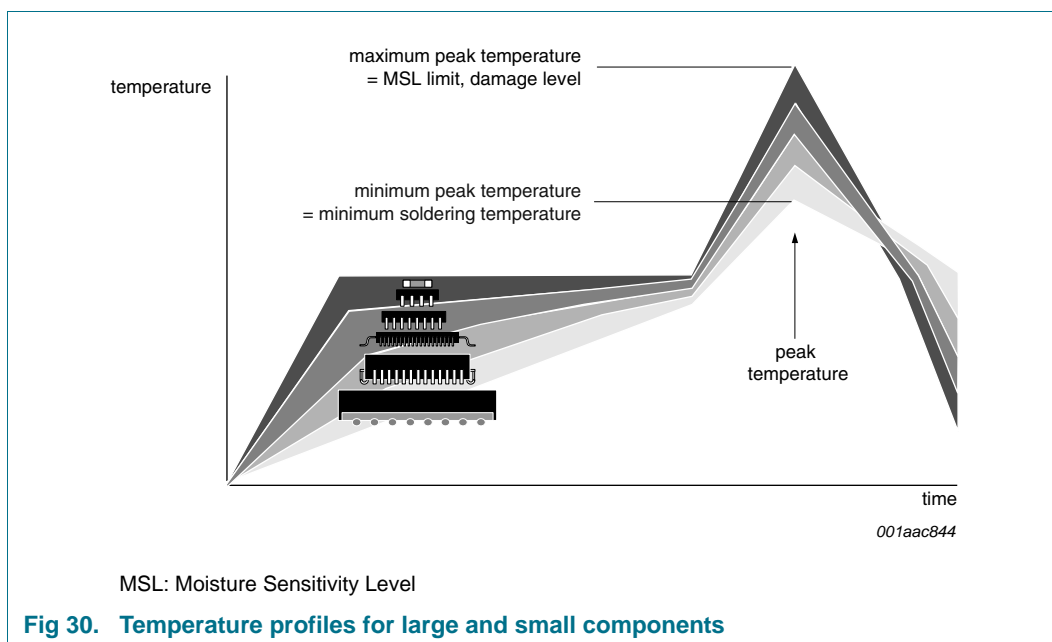
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 19. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 30](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

## 16. Abbreviations

**Table 20. Abbreviations**

Acronym	Description
AEC	Automotive Electronics Council
CDM	Charged-Device Model
DC	Direct Current
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal-Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial Clock Line
SDA	Serial DAta line
SMD	Surface-Mount Device



## 17. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [3] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [4] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [5] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [6] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [7] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [8] **JESD78** — IC Latch-Up Test
- [9] **NX3-00092** — NXP store and transport requirements
- [10] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [11] **UM10204** — I<sup>2</sup>C-bus specification and user manual

## 18. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8576C v.1	20100722	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 19.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 19.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be

suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

## 19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 20. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 21. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>8</b>	<b>Internal circuitry</b> . . . . .	<b>26</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	<b>9</b>	<b>Limiting values</b> . . . . .	<b>27</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>	<b>10</b>	<b>Static characteristics</b> . . . . .	<b>28</b>
<b>4</b>	<b>Marking</b> . . . . .	<b>2</b>	10.1	Typical supply current characteristics . . . . .	29
<b>5</b>	<b>Block diagram</b> . . . . .	<b>2</b>	10.2	Typical LCD output characteristics . . . . .	30
<b>6</b>	<b>Pinning information</b> . . . . .	<b>3</b>	<b>11</b>	<b>Dynamic characteristics</b> . . . . .	<b>31</b>
6.1	Pinning . . . . .	3	<b>12</b>	<b>Application information</b> . . . . .	<b>33</b>
6.2	Pin description . . . . .	4	12.1	Cascaded operation . . . . .	33
<b>7</b>	<b>Functional description</b> . . . . .	<b>5</b>	<b>13</b>	<b>Package outline</b> . . . . .	<b>36</b>
7.1	Power-On-Reset (POR) . . . . .	6	<b>14</b>	<b>Handling information</b> . . . . .	<b>37</b>
7.2	LCD bias generator . . . . .	6	<b>15</b>	<b>Soldering of SMD packages</b> . . . . .	<b>37</b>
7.3	LCD voltage selector . . . . .	7	15.1	Introduction to soldering . . . . .	37
7.4	LCD drive mode waveforms . . . . .	9	15.2	Wave and reflow soldering . . . . .	37
7.4.1	Static drive mode . . . . .	9	15.3	Wave soldering . . . . .	38
7.4.2	1:2 Multiplex drive mode . . . . .	10	15.4	Reflow soldering . . . . .	38
7.4.3	1:3 Multiplex drive mode . . . . .	12	<b>16</b>	<b>Abbreviations</b> . . . . .	<b>40</b>
7.4.4	1:4 multiplex drive mode . . . . .	13	<b>17</b>	<b>References</b> . . . . .	<b>41</b>
7.5	Oscillator . . . . .	14	<b>18</b>	<b>Revision history</b> . . . . .	<b>41</b>
7.5.1	Internal clock . . . . .	14	<b>19</b>	<b>Legal information</b> . . . . .	<b>42</b>
7.5.2	External clock . . . . .	14	19.1	Data sheet status . . . . .	42
7.6	Timing . . . . .	14	19.2	Definitions . . . . .	42
7.7	Display register . . . . .	15	19.3	Disclaimers . . . . .	42
7.8	Shift register . . . . .	15	19.4	Trademarks . . . . .	43
7.9	Segment outputs . . . . .	15	<b>20</b>	<b>Contact information</b> . . . . .	<b>43</b>
7.10	Backplane outputs . . . . .	15	<b>21</b>	<b>Contents</b> . . . . .	<b>44</b>
7.11	Display RAM . . . . .	15			
7.12	Data pointer . . . . .	18			
7.13	Sub-address counter . . . . .	18			
7.14	Bank selector . . . . .	19			
7.14.1	Output bank selector . . . . .	19			
7.14.2	Input bank selector . . . . .	19			
7.15	Blinker . . . . .	19			
7.16	Characteristics of the I <sup>2</sup> C-bus . . . . .	20			
7.16.1	Bit transfer . . . . .	20			
7.16.2	START and STOP conditions . . . . .	20			
7.16.3	System configuration . . . . .	21			
7.16.4	Acknowledge . . . . .	21			
7.16.5	PCA8576C I <sup>2</sup> C-bus controller . . . . .	22			
7.16.6	Input filter . . . . .	22			
7.17	I <sup>2</sup> C-bus protocol . . . . .	22			
7.18	Command decoder . . . . .	23			
7.18.1	Mode-set command . . . . .	24			
7.18.2	Load-data-pointer command . . . . .	24			
7.18.3	Device-select command . . . . .	25			
7.18.4	Bank-select command . . . . .	25			
7.18.5	Blink-select command . . . . .	25			
7.19	Display controller . . . . .	25			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 22 July 2010

Document identifier: PCA8576C