# PCA9616

## 3-channel Fast-mode Plus differential I²C-bus buffer with hot-swap logic

Rev. 1 — 2 October 2013 Preliminary data sheet

## 1. General description

The PCA9616 is a Fast-mode Plus (Fm+) SMBus/I²C-bus buffer that extends the normal single-ended SMBus/I²C-bus through electrically noisy environments using a differential SMBus/I²C-bus (dI²C) physical layer, which is transparent to the SMBus/I²C-bus protocol layer. It consists of single-ended to differential driver channels for the SCL (serial clock), SDA (serial data), and a third channel useful for INT or other signaling.

The use of differential transmission lines between identical dI²C bus buffers removes electrical noise and common-mode offsets that are present when signal lines must pass between different voltage domains, are bundled with hostile signals, or run adjacent to electrical noise sources, such as high energy power supplies and electric motors.

The SMBus/I²C-bus was conceived as a simple slow speed digital link for short runs, typically on a single PCB or between adjacent PCBs with a common ground connection. Applications that extend the bus length or run long cables require careful design to preserve noise margin and reject interference.

The dI²C-bus buffers were designed to solve these problems and are ideally suited for rugged high noise environments and/or longer cable applications, allow multiple slaves, and operate at bus speeds up to 1 MHz clock rate. Cables can be extended to at least three meters (3 m), or longer cable runs at lower clock speeds. The dI²C-bus buffers are compatible with existing SMBus/I²C-bus devices and can drive Standard, Fast-mode, and Fast-mode Plus devices on the single-ended side.

Signal direction is automatic, and requires no external control. To prevent bus latch up, the standard SMBus/I²C-bus side of the bus buffer, the PCA9616 employs static offset, care should be taken when connecting these to other SMBus/I²C-bus buffers that may not operate with static offset.

This device is a bridge between the normal single-ended wired-OR SMBus/I²C-bus and the dI²C-bus.

Additional circuitry allows the PCA9616 to be used for ‘hot swap’ applications, where systems are always on, but require insertion or removal of modules or cards without disruption to existing signals.

The PCA9616 operates over a system supply voltage range of 0.8 V to 5.5 V in two ranges, which are selected by the VDDA_SEL pin.

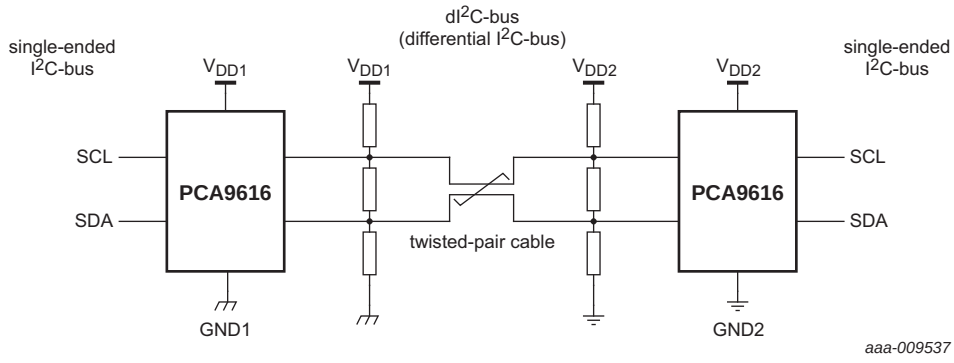



**Fig 1. SMBus/I²C-bus translation to dI²C-bus and back to SMBus/I²C-bus**

## 2. Features and benefits

- Hot swap allows insertion or removal of modules or card without disruption to bus data
- $\overline{\text{READY}}$ signal (PCA9616 output) indicates device is ready from a cold start
- EN signal (PCA9616 input) controls PCA9616 hot swap sequence
- Bus idle detect (PCA9616 internal function) waits for a bus idle condition before connection is made
- 3 channel dI²C (differential I²C-bus) to Fm+ single-ended buffer operating up to 1 MHz with 30 mA SDA/SCL > 2.2 V, or 3 mA SDA/SCL < 2.4 V
- Compatible with I²C-bus Standard/Fast-mode and Fast-mode Plus at 1 MHz
- Active HIGH (internal pull-up resistor) Enable disables the device to high-impedance state
- Single-ended I²C-bus on card side up to 540 pF >2.2 V and 400 pF <2.4 V
- Differential I²C-bus on cable side supporting multi-drop bus
  - Maximum cable length: 3 m (approximately 10 feet) (longer at lower frequency)
  - dI²C output: 3 V differential output (unloaded: ~5 V, loaded: ~1.5 V)
  - Differential line impedance (user defined): 100 Ω nominal suggested
  - Receive input sensitivity: ±200 mV
  - Hysteresis: ±30 mV typical
  - Input impedance: high-impedance (1 MΩ typical)
  - Receive input voltage range: −0.5 V to +5.5 V
- Lock-up free operation
- Supports arbitration and clock stretching across the dI²C-bus buffers
- Powered-off and powering-up high-impedance I²C-bus pins
- Operating supply voltage ($V_{DD(A)}$) range of 0.8 V to 5.5 V with single-ended side 5.5 V tolerant
- Differential I²C-bus operating supply voltage ($V_{DD(B)}$) range of 3.0 V to 5.5 V with 5.5 V tolerant. Best operation is at 5 V.
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offering: TSSOP16

# 3. Applications

- Any application with multiple power supplies and the potential for ground offsets up to 2.5 V
- Any application that requires long I²C-bus runs in electrically noisy environments
- Monitor remote temperature/leak detectors in harsh environment with interrupt back to master
- Control of power supplies in high noise environment
- Transmission of I²C-bus between equipment cabinets
- Commercial lighting and industrial heating/cooling control

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| PCA9616PW | PCA9616 | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature range |
|---|---|---|---|---|---|
| PCA9616PW | PCA9616PW,118 | TSSOP16 | Reel 13” Q1/T1 *standard mark SMD | 2500 | $T_{amb}$ = −40 °C to +85 °C |

## 5. Block diagram

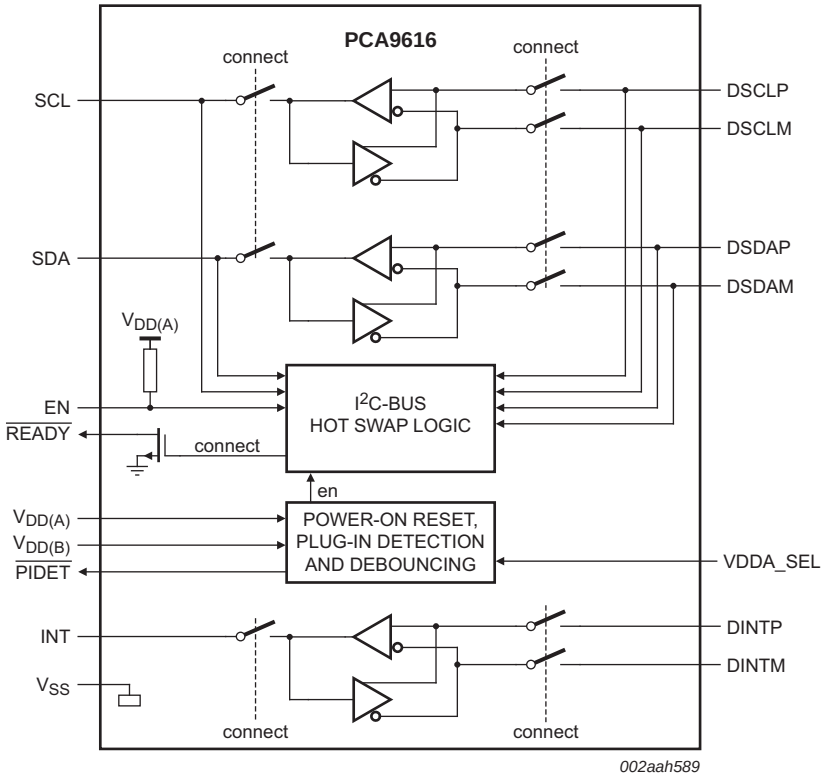



**Fig 2. Block diagram (level 0)**

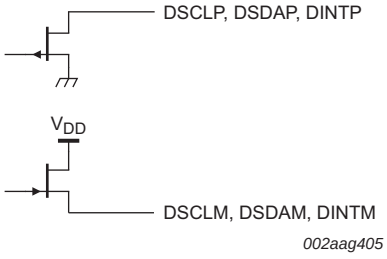



**Fig 3. Differential output driver simplified circuit**

# 6. Pinning information

## 6.1 Pinning

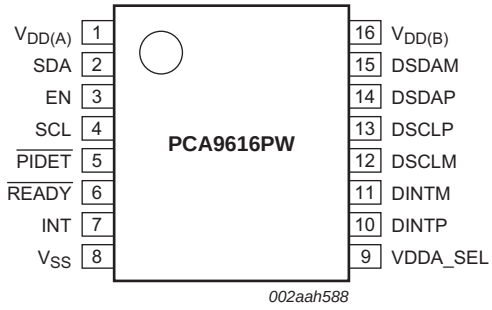



**Fig 4. Pin configuration for TSSOP16**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{DD(A)}$ | 1 | $I^2C$-bus side power supply.<br>2.3 V to 5.5 V for PCA9616 |
| SDA | 2 | card side open-drain serial data input/output |
| EN | 3 | enable input |
| SCL | 4 | card side open-drain serial clock input/output |
| $\overline{PIDET}$ | 5 | plug-in detection, open-drain output LOW to indicate that all hot-swap pins have been steady and reliably plugged into the backplane |
| $\overline{READY}$ | 6 | open-drain output that goes HIGH when SDA and SCL are disconnected from DSDA and DSCL, and pulls LOW when two sides are connected |
| INT | 7 | card side open-drain interrupt input/output |
| $V_{SS}$ | 8 | ground supply voltage (0 V) |
| VDDA_SEL | 9 | $V_{DD(A)}$ supply pin option input. Floating is not information of $V_{DD(A)}$ range. Recommend to be HIGH when $V_{DD(A)}$ > 2.3 V and be LOW when $V_{DD(A)}$ < 2.3 V through a resistor. |
| DINTP | 10 | line side differential open-drain interrupt plus input/output |
| DINTM | 11 | line side differential open-drain interrupt minus input/output |
| DSCLM | 12 | line side differential open-drain clock minus input/output |
| DSCLP | 13 | line side differential open-drain clock plus input/output |
| DSDAP | 14 | line side differential open-drain data plus input/output |
| DSDAM | 15 | line side differential open-drain data minus input/output |
| $V_{DD(B)}$ | 16 | differential side power supply (3.0 V to 5.5 V) |

# 7. Functional description

Refer to Figure 2.

The PCA9616 is used at each node of the dI²C-bus signal path, to provide conversion from the dI²C-bus signal format to conventional I²C-bus/SMBus, allowing the connection of existing I²C-bus/SMBus devices as slaves or the bus master. Because the signal voltages on the I²C-bus/SMBus bus side may be different from the dI²C-bus side, there are two power supply pins and a common ground. Static offset is employed by the I²C-bus/SMBus side to prevent bus latch up. Signal direction is determined by the I²C-bus/SMBus bus protocol, and does not require a direction signal, as these bus buffers automatically set signal flow direction. An enable pin (EN) is provided to disable the bus buffer, and is useful for fault finding, power-up sequencing, or reconfiguration of a large bus system by isolating sections not needed at all times.

Construction of the differential transmission line is not device dependent. PCB traces, open wiring, twisted pair cables or a combination of these may be used. Twisted pair cables offer the best performance. A typical twisted pair transmission line cable has a characteristic impedance of 'about 100 Ω' and must be terminated at both ends in 100 Ω to prevent unwanted signal reflections. Multiple nodes (each using a dI²C-bus buffer) may be connected at any point along this transmission line, however, the stub length will degrade the bus performance, and should therefore be minimized.

## 7.1 I²C-bus/SMBus side

The I²C-bus/SMBus side of the PCA9616 differential bus buffer is connected to other I²C-bus/SMBus devices and requires pull-up resistors on each of the SCL and SDA signals. The value of the resistor should be chosen based on the bus capacitance and desired data speed, being careful not to overload the driver current rating of 3 mA for Standard and Fast modes, 30 mA for Fast-mode Plus (Fm+). Note that at lower supply voltages the driver will not deliver the higher current (see Table 5 "Static characteristics"). The I²C-bus/SMBus side of the PCA9616 is powered from the $V_{DD(A)}$ supply pin.

## 7.2 dI²C-bus side differential pair

In previous I²C-bus/SMBus designs the nodes (Master and one or more Slaves) are connected by wired-OR in combination with a single pull-up resistor. This simple arrangement is not suited for long distances more than one meter (1 m) or about three feet (3 ft), due to ringing and reflections on the un-terminated bus. The use of a transmission line with correct termination eliminates this problem, and is further improved by differential signaling used in the dI²C-bus scheme. Each node acts as both a driver and a receiver to allow bidirectional signal flow, but not at the same time. Switching from transmit to receive is done automatically. The dI²C-bus side of the PCA9616 is powered from the $V_{DD(B)}$ supply pin.

The dI²C-bus is also biased to an idle state (D+ more positive than D–) to be compatible with the I²C-bus/SMBus wired-OR scheme, when not transmitting traffic (data). This allows every node to receive broadcast messages from the Master, and return ACK/NACK and data in response. Biasing is done with additional resistors, connected to $V_{DD(B)}$ and $V_{SS}$ (the local ground), as shown in Figure 5. The transmission line is terminated in the characteristic impedance of the cable, typically 100 Ω. This is the value defined by three resistors, the other two resistors providing the idle condition bias to the twisted pair.

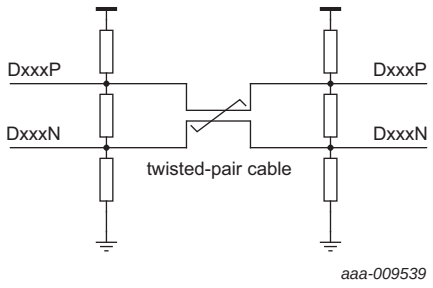



**Fig 5. dI²C-bus terminations**

### 7.2.1 Noise rejection

Impulse noise coupled into the I²C-bus/SMBus signals can prevent the I²C-bus/SMBus bus from operating reliably. The hostile signals may appear on the SCL line, SDA line, or both. Impulse noise may also enter the common ground connection, or be caused by current in the ground path caused by DC power supplies, or other signals sharing the common ground return path. This problem is removed by using a differential transmission line, in place of the I²C-bus/SMBus signal path. The dI²C-bus receiver (at each dI²C-bus node) subtracts the signals on the two differential lines (D+ and D−), and eliminates any common-mode noise that is coupled into the dI²C-bus. The receiver amplifies the signals which are also attenuated by the bulk resistance of the transmission line cable connection, and does not rely on a common ground connection at each node.

### 7.2.2 Rejection of ground offset voltage

Hostile signals interfere with the I²C-bus/SMBus bus through the common ground connection between each node. Current in this ground path will cause an offset that may cause false data or push the I²C-bus/SMBus signals outside of an acceptable range. Unwanted ground offset can be caused by heavy DC current in the ground path, or injection of ground current from AC signals, either of which may show up as false signals.

Because the dI²C-bus node's receiver responds only to the difference between the two dI²C-bus transmission lines, common-mode signals are ignored. There is no need to have a ground connection between each of the nodes, which may be powered locally. Nodes may also be powered by extra conductors (for $V_{DD}$ and ground) run with the dI²C-bus signals. Voltage offsets caused by DC current in these additional wires will be ignored by the dI²C-bus receiver, which subtracts the two differential signals (D+ and D−).

## 7.3 EN pin

Enable input. When the EN pin is LOW, the device will never connect to the bus, and/or disconnect the SCL/SDA from differential SCL/SDA, and assert $\overline{\text{READY}}$ pin HIGH. When EN is driven HIGH, and $V_{DD(A)}$ and $V_{DD(B)}$ are stable (indicated by $\overline{\text{PIDET}}$ goes LOW), the EN pin connects SDA/SCL to differential SDA/SCL after a stop bit or bus idle has been detected on differential line bus.

## 7.4 $\overline{\text{PIDET}}$ pin

Plug-in status output. This open-drain N-channel MOSFET output pulls LOW when the hot-swapped pins (differential SDA and SCL) have been steady and reliably plugged into the bus when $V_{DD(A)}$ and $V_{DD(B)}$ are powered. Connect a pull-up resistor, typically 10 kΩ, from this pin to $V_{DD(A)}$. Leave open or tie to $V_{SS}$ if unused.

## 7.5 $\overline{\text{READY}}$ pin

Connection ready status output. This open-drain N-channel MOSFET output goes HIGH when the input and output sides are disconnected. $\overline{\text{READY}}$ is pulled LOW when EN is HIGH, $\overline{\text{PIDET}}$ is LOW, and a connection has been established between the input and differential output. Connect a pull-up resistor, typically 10 kΩ, from this pin to $V_{DD(A)}$. Leave open or tie to $V_{SS}$ if unused.

## 7.6 VDDA_SEL pin

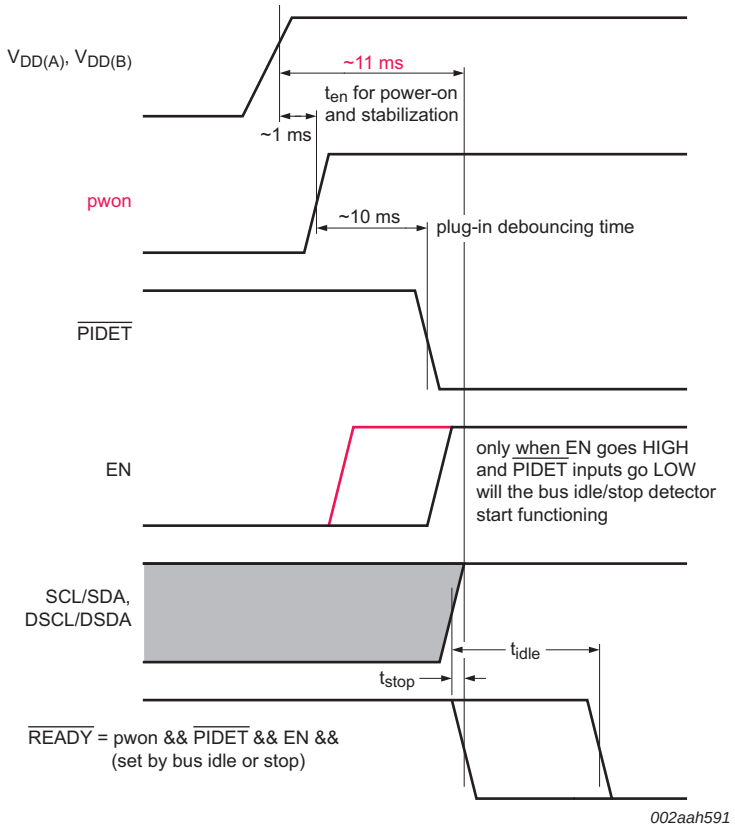
Enable input to select $V_{DD(A)}$ range. Tie to $V_{DD(B)}$ if $V_{DD(A)}$ is greater than 2.2 V and constant $V_{OL}$ on SCL/SDA (0.52 V) is desired, and tie to $V_{SS}$ if $V_{DD(A)}$ is less than 2.4 V and the ratio $V_{OL}$ ($0.2 \times V_{DD(A)}$) is desired. Or leave open to let the device automatically switch based on $V_{DD(A)}$ magnitude.

## 7.7 Hot swap and power-on reset functionality

During a power-on sequence, an initialization circuit holds the PCA9616 in a disconnected state, meaning all outputs — SDA, SCL and the differential pins DSCLP/DSCLM and DSDAP/DSDAM — are in a high-impedance state. As the power supply rises (either power-up or live insertion), the initialization circuit enters a state where the internal references are stabilized and an internal timer is triggered. After 1 ms power is applied to the rest of the circuitry and the PCA9616 detects the status on the differential DSCLP/DSCLM and DSDAP/DSDAM lines. When the differential lines are detected as connected to a bus with valid termination, that is, both DSCLM/DSDAM < $0.9 \times V_{DD(B)}$ and DSCLP/DSDAP > $0.1 \times V_{DD(B)}$, another timer is triggered. At the end of 10 ms, hot-swap logic (Figure 2) is enabled and the EN pin can detect a Stop Bit and Bus Idle condition. However, there is still no connection between SDA and DSDAP/DSDAM or between SCL and DSCLP/DSCLM. A successful EN pin sequence must occur for actual connection.

When the EN pin is set HIGH and the DSDAP and DSCLP pins have been HIGH for the bus idle time or when both the SCL and SDA pins are HIGH and a STOP condition has been seen on the differential bus (DSDAP/DSDAM and DSCLP/DSCLM pins), a connection is established between the differential and the single-ended buses. Whenever disconnected status is detected or the device is un-powered, the PCA9616 will disconnect the single-ended to differential buses, and the hot swap sequence will repeat again before the PCA9616 connects SDA to DSDAP/DSDAM and SCL to DSCLP/DSCLM.

**Remark:** Start-up process is the same for both PCA9616PW and PCA9615DP, except that $\overline{\text{PIDET}}$ and $\overline{\text{READY}}$ signals are only available in 16-pin package.




For PCA9616, the $\overline{\text{READY}}$ time is at least 11 ms (1 ms for power ready, 10 ms for plug-in debouncing delay), which means the device can only be in operation after 11 ms with $V_{DD(A)}$, $V_{DD(B)}$ ON and a bus idle/stop detected.

**Fig 6. Hot swap related timings**

# 8. Application design-in information

## 8.1 I²C-bus

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the single-ended buffered bus (standard open-drain configuration of the I²C-bus). The size of these pull-up resistors depends on the system. The device is designed to work with Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard-mode and Fast-mode I²C-bus and SMBus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple masters are possible.

When only Fast-mode Plus devices are used, then higher termination currents can be used due to their 30 mA sink capability. The sink capability varies from 3 mA at 0.8 V to 30 mA at 5.5 V with the cut-off between 30 mA and 3 mA at 2.3 V.

## 8.2 Differential I²C-bus application

See Figure 7 through Figure 9.

The simple application (Figure 7) shows an existing SMBus/I²C-bus being extended over a section of dI²C-bus transmission line, containing a dedicated twisted pair for SCL and SDA. At one end of the transmission line a resistor network (R1, R2, R3) terminates the twisted pair cable and biases D+ positive with respect to D−. An identical resistor network at the other end of the transmission line terminates the twisted pair cable. DC power for each end of the transmission line and the $V_{DD(B)}$ of each PCA9616 bus buffer can be from separate and isolated power supplies, or use the same supply and ground run in separate wires along the same path as the dI²C-bus signal twisted pairs.

Telecom category 5 (‘CAT 5’) data cable is well suited for this task, but loose wires may also be used, with a reduction in performance. Assuming $V_{DD(B)}$ is 5 V, and using CAT 5 cable, R2 is 120 Ω, R1 and R3 are 600 Ω. The parallel combination yields a termination of 100 Ω at each end of the twisted pairs.

Either side of the dI²C-bus buffer pair is connected to standard SMBus/I²C buses, which require their own pull-up resistors to $V_{DD(A)}$ of the PCA9616 bus buffers. $V_{DD(A)}$ and $V_{DD(B)}$ can be the same supply, however, making them different voltages enables the PCA9616 bus buffers to level translate between the SMBus/I²C-bus and dI²C-bus sections of the bus, or to have different supply voltages and level translate at either end of the dI²C-bus and SMBus/I²C-bus system.

For example, the left-hand bus master (and local slave) may operate on a 3.3 V supply and SMBus/I²C-bus while the dI²C-bus transmission lines are at 5 V, and the right-hand slave is operated from a different 3.3 V supply and SMBus/I²C-bus, or even a different bus voltage other than 3.3 V.

Depending upon the timing from the system master, clock toggle rates can vary from 10 kHz for the SMBus (or less for SMBus/I²C-bus protocol) up to 100 kHz (Standard mode), 400 kHz (Fast mode), or up to 1 MHz (Fast-mode Plus).

The bus path is bidirectional. Assume that the left side SMBus/I²C-bus becomes active. A START condition (SDA goes LOW while SDA is HIGH) is sent. This upsets the idle condition on the dI²C-bus section of the bus, because D+ was more positive than D− and

now they are reversed. The right side bus buffer sees the differential lines change polarity and in turn pulls SDA LOW on the SMBus/I²C-bus side of the bus buffer, transmitting the START condition to the slave on that section of the SMBus/I²C-bus.

If the data clocked out by the left side master contains a valid address of the right side slave, that slave responds by pulling SDA LOW on the ninth clock. This condition is transmitted across the dI²C-bus section that has now changed flow direction, and received by the left side bus buffer (again, D+ was more positive than D− and now they are reversed).

This sequence continues until the master sends the STOP condition (SCL HIGH while SDA goes HIGH), placing the active slave (on the right side) back to idle. When idle, the normal SMBus/I²C-bus (both left and right sections) are pulled up by their respective pull-ups. In turn, the dI²C-bus section of the bus rests with D+ more positive than D−.

The idle condition can be changed by any node on either SMBus/I²C-bus section or an additional dI²C-bus node, if present, on the dI²C-bus section of the system. This allows the existing SMBus/I²C-bus protocol to operate transparently over a mix of SMBus/I²C and dI²C bus segments.

Due to the SMBus/I²C-bus handshake protocol (ACK/NACK on the ninth clock pulse), the direction of the SMBus/I²C-bus is reversed often. The ‘time of flight’ for the signals to pass through each bus buffer and for the target slave to respond defines the maximum speed of the bus, regardless of how fast the clock toggles. The dI²C-bus section of the bus requires two additional PCA9616 bus buffers, further delaying the SMBus/I²C-bus traffic. If the dI²C-bus transmission line section is made longer, the bus will operate much slower, regardless of the clock toggle speed.

It is not necessary to have a ground connection between each end of the dI²C section of the bus. The dI²C-bus receiver responds to reversal of the polarity of the D+ and D− signals, and ignores the common-mode voltage that may be present.

Ideally, the common-mode voltage is the same at each end of the twisted pairs, and no current flows along the twisted pair when the bus is idle, because the D+ and D− dI²C-bus drivers are both high-impedance, the bus is biased by R1, R2 and R3 at each end. If the common-mode voltage is not 0 V, current will flow along the twisted pair, returning through the common ground or common power supply connection if present.

If both ends of the twisted pair are powered by the same $V_{DD(B)}$ supply and one end is remote, there will be a common-mode offset between them. This is ignored by the dI²C-bus receivers, which only respond to the difference between D+ and D−.

However, a large common-mode offset voltage will force the D+ and D− signals out of the range of the receiver, and data will be lost. The PCA9616 bus buffers use standard ESD protection networks to protect the external pins, and therefore should not be biased above or below the $V_{DD(B)}$ and $V_{SS}$ pins respectively. This limits the common-mode range to approximately $0.5 \times V_{DD(B)}$.

DC resistance of the transmission line will attenuate the signals, more so over longer distances. The loss of signal amplitude is made up by the gain of the dI²C-bus receiver. There is a limit to how long the dI²C-bus section can be made, as it is necessary for the driver to overcome the bias on the transmission line, in order to signal a polarity change (D+ and D− reversal) at the receiver end.

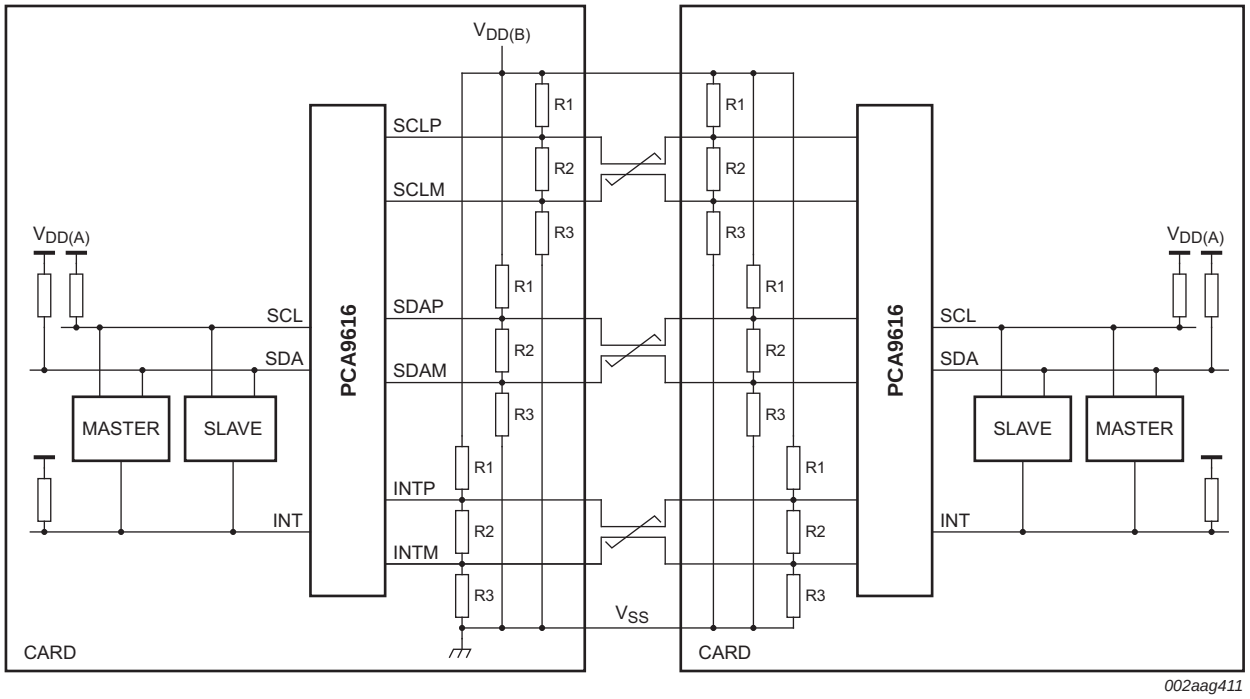



**Fig 7. Typical application for PCA9616**

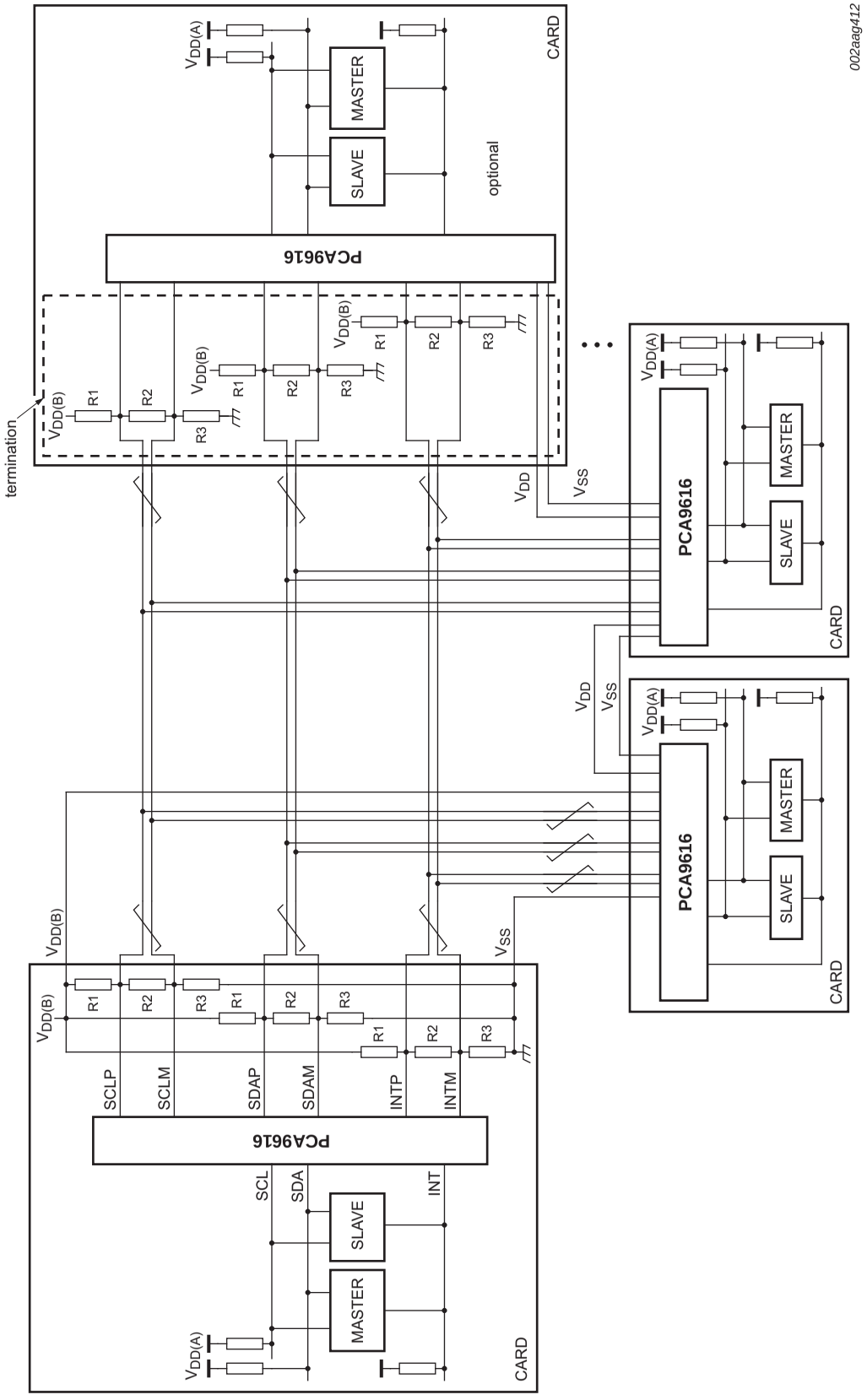



**Fig 8. PCA9616 application diagram; $V_{DD}$ and $V_{SS}$ are routed through the cable**

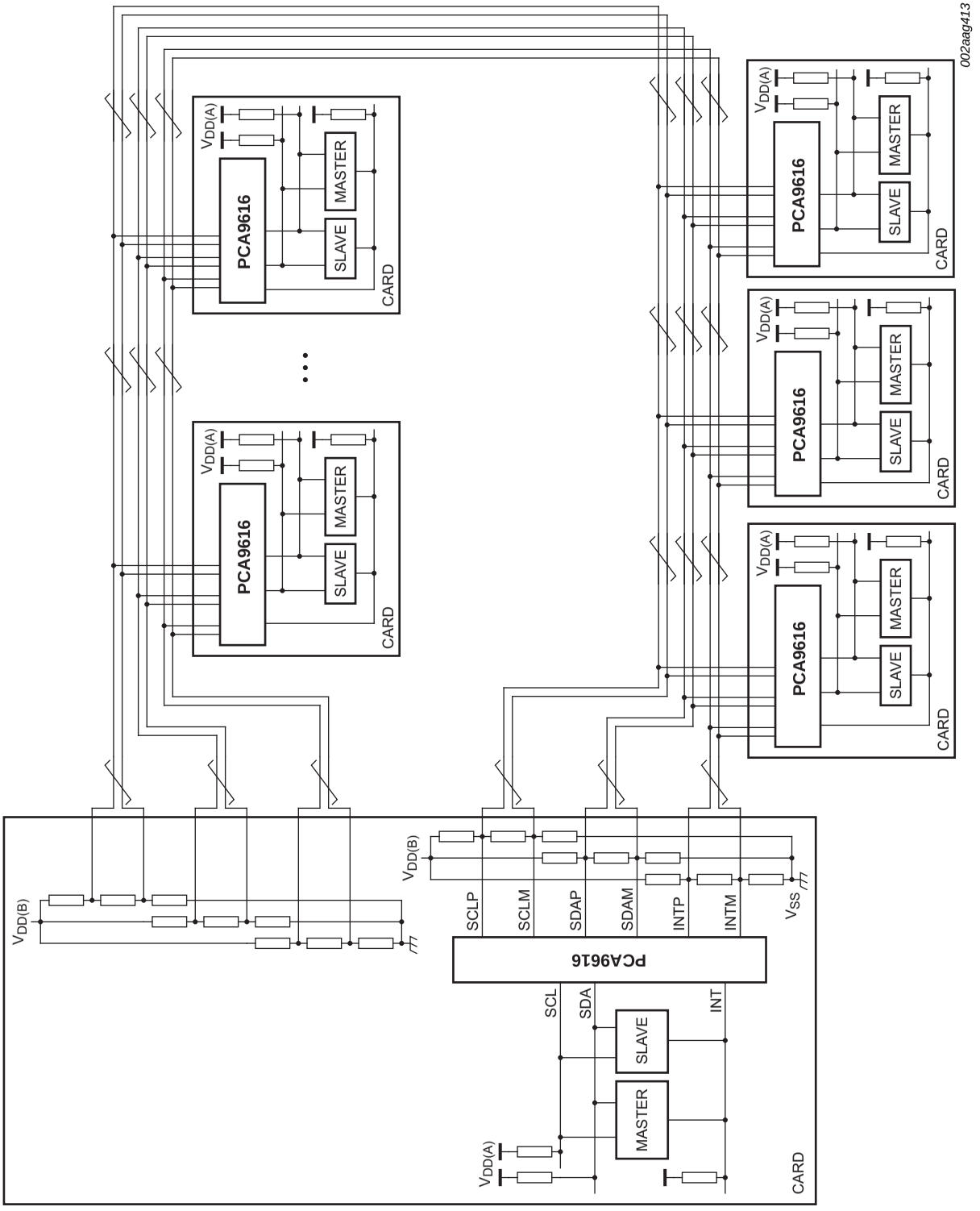



**Fig 9. PCA9616 application diagram; $V_{DD}$ and $V_{SS}$ are not routed through the cable**

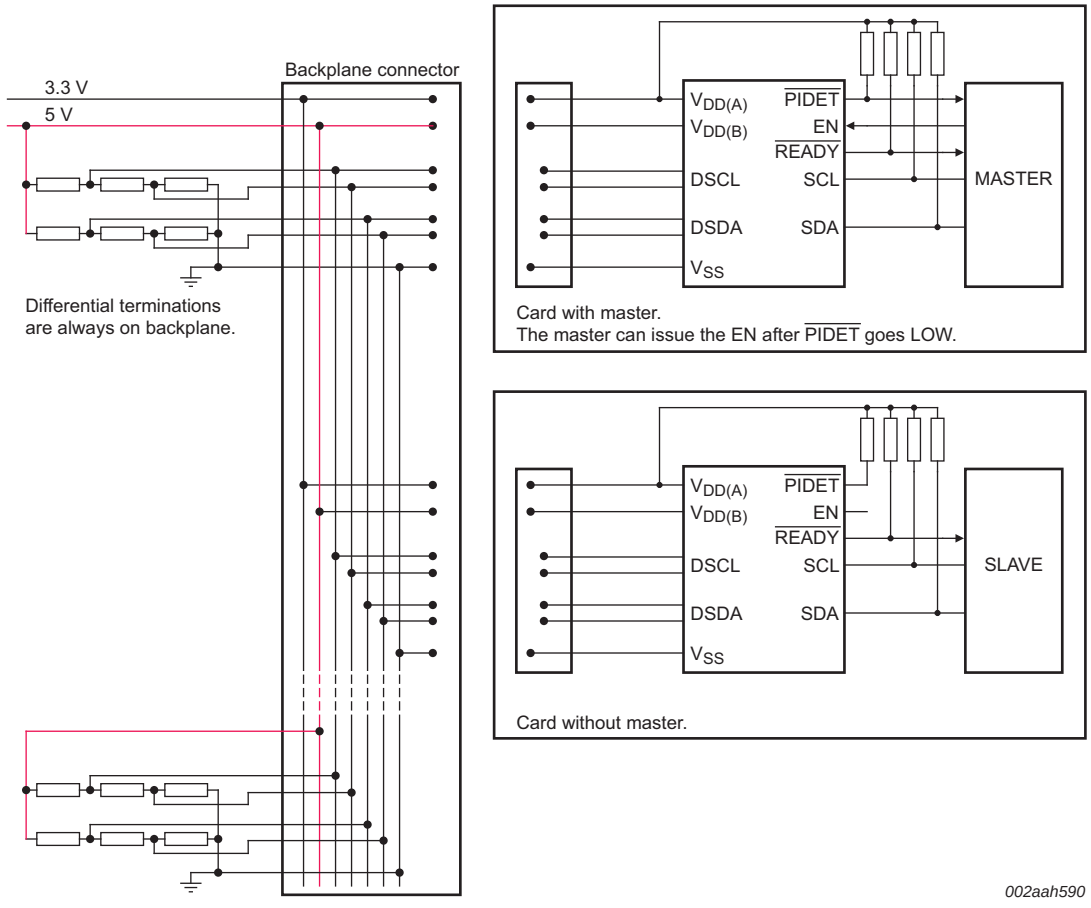



**Fig 10. Hot swap application**


**Fig 11. Differential bus waveform**

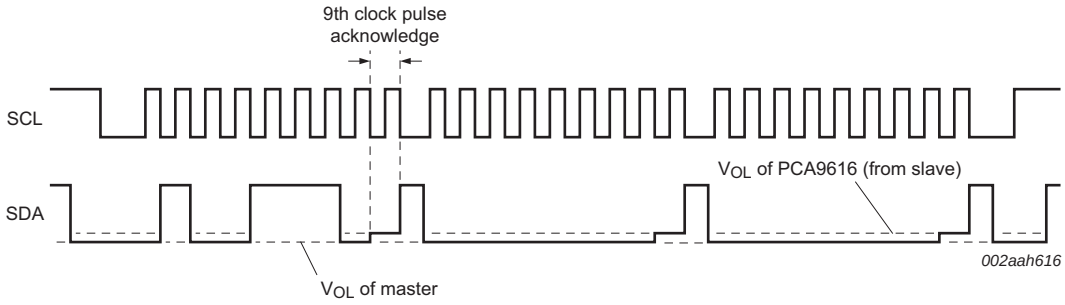



**Fig 12. Single-ended bus waveform (master side of bus)**

# 9. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD(B)}$ | supply voltage port B | differential bus; 3.0 V to 5.5 V | –0.5 | +6 | V |
| $V_{DD(A)}$ | supply voltage port A | single-ended bus | | | |
| | | 2.3 V to 5.5 V | –0.5 | +6 | V |
| | | 0.8 V to 2.3 V | –0.5 | +6 | V |
| $V_{O(dif)}$ | differential output voltage | | –0.5 | +6 | V |
| $V_{bus}$ | bus voltage | voltage on I²C-bus A side, or enable (EN) | –0.5 | +6 | V |
| $I_{DD}$ | supply current | DC current on any pin | - | 80 | mA |
| $I_{DD(B)}$ | supply current port B | | - | 160 | mA |
| $P_{tot}$ | total power dissipation | | - | 100 | mW |
| $T_{stg}$ | storage temperature | | –55 | +125 | °C |
| $T_{amb}$ | ambient temperature | operating in free air | –40 | +85 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |

# 10. Static characteristics

**Table 5. Static characteristics**

*$V_{DD(B)}$ = 3.0 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DD(B)}$ | supply voltage port B | differential bus | 3.0 | - | 5.5 | V |
| $V_{DD(A)}$ | supply voltage port A | single-ended bus [1] | 0.8 | - | 5.5 | V |
| $I_{DD(VDDA)}$ | supply current on pin $V_{DD(A)}$ | | - | - | 16 | µA |
| $I_{DDH(B)}$ | port B HIGH-level supply current | 3-channel; both channels HIGH; $V_{DD(B)}$ = 5.5 V; INT = SDAn = SCLn = $V_{DD(A)}$ = 5.5 V | - | 0.9 | 2.0 | mA |
| $I_{DDL(B)}$ | port B LOW-level supply current | 3-channel; both channels LOW; $V_{DD(B)}$ = 5.5 V; SDA and SCL = $V_{SS}$; differential I/Os open | - | 1.5 | 3.0 | mA |
| | | driving termination; 3 channels | - | 105 | 136 | mA |
| **Input and output SDA and SCL and INT** | | | | | | |
| $C_L$ | load capacitance | loading capacitance that single-ended I²C-bus on card side can drive | - | 540 | - | pF |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD(A)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | VDDA_SEL = 1 and $V_{DD(A)}$ > 2.2 V | –0.5 | - | +0.4 | V |
| | | VDDA_SEL = 0 and $V_{DD(A)}$ < 2.4 V | –0.5 | - | $+0.1V_{DD(A)}$ | V |
| $V_{IK}$ | input clamping voltage | $I_I$ = –18 mA | –1.5 | - | 0 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 5.5 V | - | - | ±2 | µA |
| $I_{IL}$ | LOW-level input current | SDA, SCL; $V_I$ = 0.2 V | - | - | 12 | µA |

**Table 5. Static characteristics** *…continued*

*$V_{DD(B)}$ = 3.0 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 μA or 30 mA ($V_{DD(A)}$ > 2.2 V and VDDA_SEL = 1) | 0.47 | 0.52 | 0.6 | V |
| | | $I_{OL}$ = 200 μA or 3 mA ($V_{DD(A)}$ < 2.4 V and VDDA_SEL = 0) | - | $0.2V_{DD(A)}$ | $0.3V_{DD(A)}$ | |
| $V_{OL}$–$V_{IL}$ | difference between LOW-level output and LOW-level input voltage | guaranteed by design | | | | |
| | | $I_{OL}$ = 200 μA or 30 mA ($V_{DD(A)}$ > 2.2 V and VDDA_SEL = 1) | - | - | 90 | mV |
| | | $I_{OL}$ = 200 μA or 3 mA ($V_{DD(A)}$ < 2.4 V and VDDA_SEL = 0) | - | $0.05V_{DD(A)}$ | $0.1V_{DD(A)}$ | |
| $I_{LOH}$ | HIGH-level output leakage current | $V_O$ = 5.5 V | - | - | 2 | μA |
| $C_{io}$ | input/output capacitance | $V_I$ = 3 V or 0 V; $V_{DD(A)}$ = 3.3 V disabled | - | 7 | - | pF |
| | | $V_I$ = 3 V or 0 V; $V_{DD(A)}$ = 0 V | - | 7 | - | pF |
| **Input and output DSDAP/DSDAM and DSCLP/DSCLM and DINTP/DINTM** | | | | | | |
| $V_{cm}$ | common-mode voltage | | 0 | - | 5.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 5.5 V | | | | |
| | | DSCLP, DSCLM, DSDAP, DSDAM pins | - | - | ±40 | μA |
| | | DINTP, DINTM | - | - | ±1 | μA |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.2 V | | | | |
| | | DSCLP, DSCLM, DSDAP, DSDAM pins | - | - | ±40 | μA |
| | | DINTP, DINTM | - | - | ±1 | μA |
| $R_{PU}$ | pull-up resistance | internal pull-up resistor on DSCLM and DSDAM connected to $V_{DD(B)}$ rail | - | 200 | - | kΩ |
| $R_{pd}$ | pull-down resistance | internal pull-down resistor on DSCLP and DSDAP connected to $V_{SS}$ rail | - | 200 | - | kΩ |
| $V_{th(dif)}$ | differential receiver threshold voltage | 0 V ≤ $V_{cm}$ ≤ 5.5 V | −200 | - | +200 | mV |
| $V_{I(hys)}$ | hysteresis of input voltage | receiver; 0 V ≤ $V_{cm}$ ≤ 5.5 V | <tbd> | <tbd> | <tbd> | mV |
| $V_{o(dif)p-p}$ | peak-to-peak differential output voltage | single-ended input LOW | | | | |
| | | no load | $-V_{DD(B)}$ | - | - | V |
| | | $R_L$ = 54 Ω at $V_{DD(B)}$ = 5 V | −5.0 | −1.5 | −1.0 | V |
| $C_{io}$ | input/output capacitance | $V_I$ = 3 V or 0 V disable | | | | |
| | | $V_{DD(B)}$ = 5.0 V | - | 7 | - | pF |
| | | $V_{DD(B)}$ = 0 V | - | 7 | - | pF |

**Table 5. Static characteristics** *…continued*

*$V_{DD(B)}$ = 3.0 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input EN** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD(A)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | $+0.3V_{DD(A)}$ | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD(B)}$ | −1 | - | +1 | μA |
| $I_{IL(EN)}$ | LOW-level input current on pin EN | $V_I$ = 0.2 V, EN; $V_{DD(A)}$ = 5.5 V | - | −10 | −54 | μA |
| $C_i$ | input capacitance | $V_I = V_{DD(A)}$ | - | 6 | 7 | pF |
| $R_{PU}$ | pull-up resistance | internal pull-up resistor connected to $V_{DD(A)}$ rail | - | 300 | - | kΩ |
| **Output $\overline{\text{PIDET}}$ and $\overline{\text{READY}}$** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 3 mA; $V_{DD(B)}$ = 3.0 V | −0.5 | - | +0.4 | V |
| $I_L$ | leakage current | $\overline{\text{READY}}$ and $\overline{\text{PIDET}}$ OFF; $V_{DD(A)} = V_{\overline{\text{PIDET}}}/V_{\overline{\text{READY}}}$ = 5.5 V | - | - | ±2 | μA |
| **Input VDDA_SEL** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD(B)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | $+0.3V_{DD(B)}$ | V |
| $I_{LI}$ | input leakage current | $V_{DD(B)}$ = 5.5 V; $V_I$ = 0 V for $V_{DD(A)}$ < 1.8 V, or $V_I = V_{DD(B)}$ for $V_{DD(A)}$ > 2.5 V | - | - | ±1 | μA |

[1] LOW-level supply voltage. Recommend VDDA_SEL = 1 for $V_{DD(A)}$ = 1.8 V to 2.4 V, and VDDA_SEL = 0 for $V_{DD(A)}$ = 2.2 V to 5.5 V.

# 11. Dynamic characteristics

**Table 6. Dynamic characteristics**

*$V_{DD}$ = 2.7 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*[1][2]

| Symbol | Parameter | Conditions | | Min | Typ[3] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW to HIGH propagation delay | single-ended side to differential side; Figure 15 | [4] | −140 | −120 | - | ns |
| $t_{PLH2}$ | LOW to HIGH propagation delay 2 | single-ended side to differential side; Figure 15 | | - | - | 100 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | single-ended side to differential side; Figure 13 | [5] | - | - | 120 | ns |
| $SR_r$ | rising slew rate | differential side; Figure 13 | | - | - | 1 | V/ns |
| $SR_f$ | falling slew rate | differential side; Figure 13 | [5] | - | - | 1 | V/ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | differential side to single-ended side; Figure 14 | [6] | - | - | 150 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | differential side to single-ended side; Figure 14 | [6] | - | - | 150 | ns |
| $SR_f$ | falling slew rate | single-ended side; Figure 14 | | - | - | 0.1 | V/ns |
| $t_{dis}$ | disable time | EN LOW to disable | [7] | - | - | 200 | ns |
| $t_{idle}$ | idle time | $\overline{\text{READY}}$ active after bus idle | | - | 100 | - | µs |
| $t_{stop}$ | stop time | $\overline{\text{READY}}$ active after bus stop | | - | - | 1 | µs |
| $t_{deb(bus)}$ | bus debounce time | | | 5 | - | 15 | ms |

[1] Times are specified with loads of 1.35 kΩ pull-up resistance and 50 pF load capacitance on the A side, and 50 Ω termination network resistance and 50 pF load capacitance on the B side. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

[2] Pull-up voltages are $V_{DD(A)}$ on the A side and termination network on the B side.

[3] Typical values were measured with $V_{DD(A)}$ = 3.3 V at $T_{amb}$ = 25 °C, unless otherwise noted.

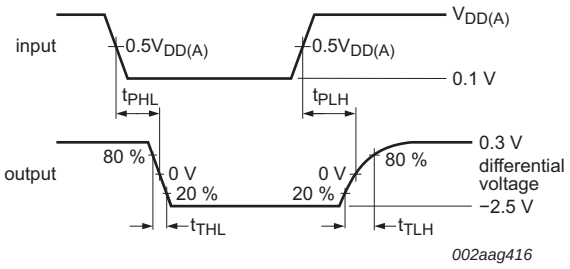
[4] The $t_{PLH}$ delay data from B side to A side is measured at 0 V differential on the B side to $0.5V_{DD(A)}$ on the A side.

[5] Typical value measured with $V_{DD(A)}$ = 3.3 V at $T_{amb}$ = 25 °C.

[6] The proportional delay data from A side to B side is measured at $0.5V_{DD(A)}$ on the A side to 0 V on the B side.

[7] The enable pin (EN) should only change state when the global bus and the repeater port are in an idle state.

## 11.1 AC waveforms

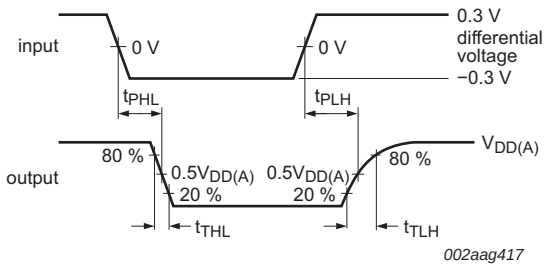



$V_{DD(A)}$ = 3.0 V.

$SR_f = 0.6 \times (V_{high} - V_{low}) / t_{THL}$

$SR_r = 0.6 \times (V_{high} - V_{low}) / t_{TLH}$

**Fig 13. Propagation delay and transition times; single-ended side to differential side**




$V_{DD(A)}$ = 3.0 V.

$SR_f = 0.6 \times V_{DD(A)} / t_{THL}$

**Fig 14. Propagation delay and transition times; differential side to single-ended side**

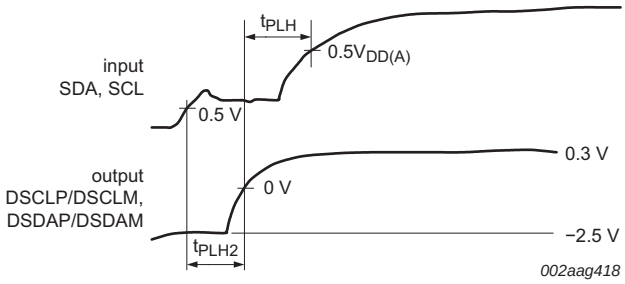
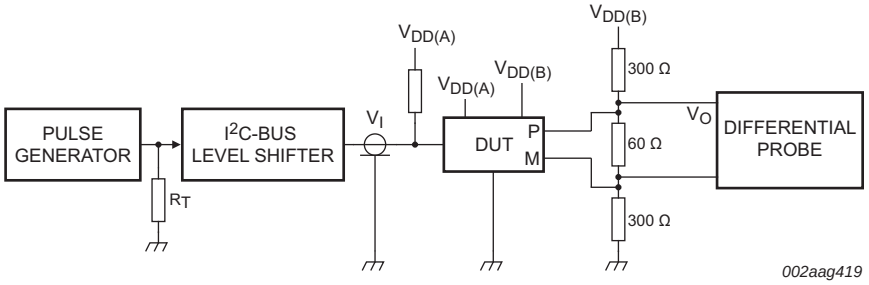



**Fig 15. Propagation delay**

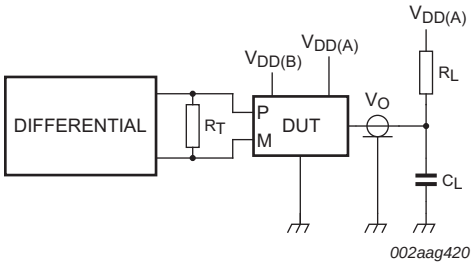
## 12. Test information




$R_L$ = load resistor; 1.35 kΩ on single-ended side.

$R_T$ = termination resistance should be equal to $Z_o$ of pulse generators.

**Fig 16. Test circuit for differential outputs**




$R_L$ = load resistor; 1.35 kΩ on single-ended side.

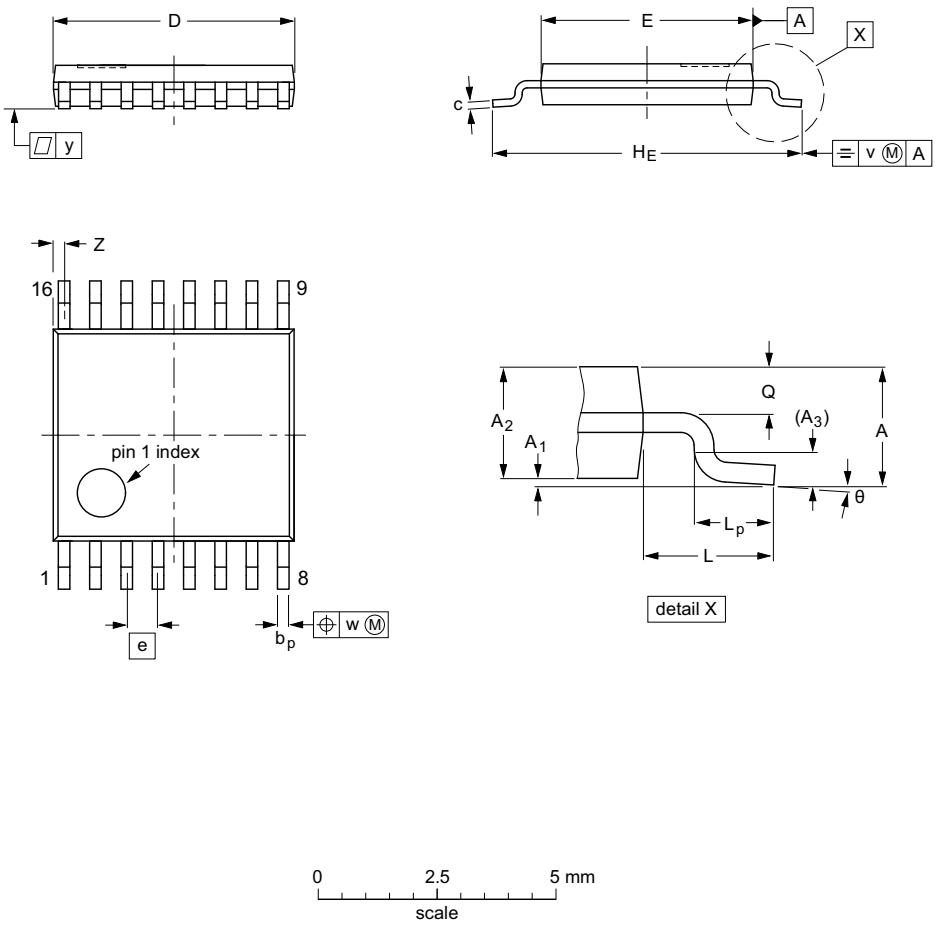
$C_L$ = load capacitance includes jig and probe capacitance; 50 pF.

$R_T$ = termination resistance should be equal to $Z_o$ of pulse generators.

**Fig 17. Test circuit for open-drain output**

## 13. Package outline

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 18. Package outline SOT403-1 (TSSOP16)**

# 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

**Table 7. SnPb eutectic process (from J-STD-020D)**

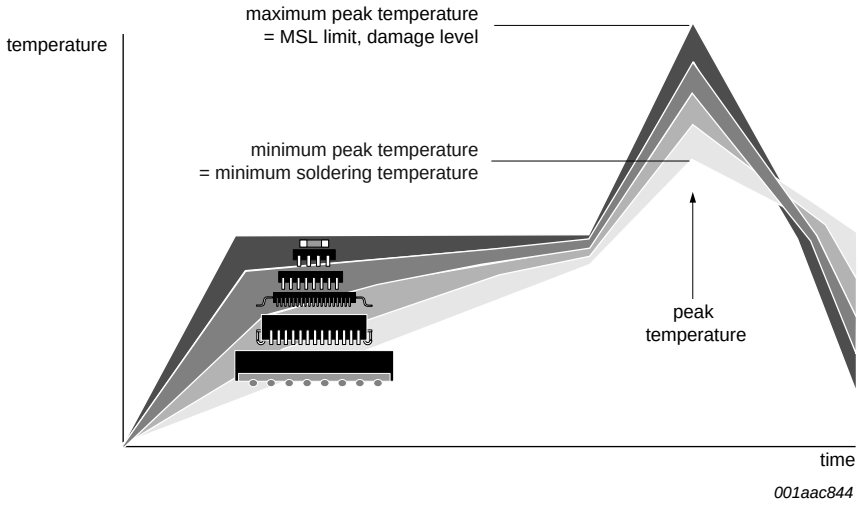
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 8. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



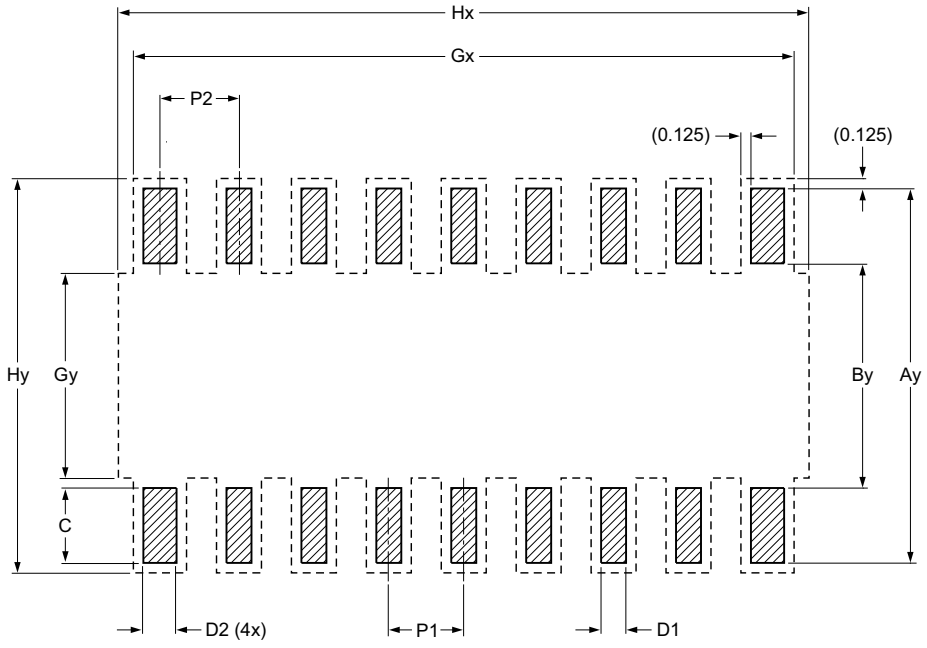

MSL: Moisture Sensitivity Level

**Fig 19. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15. Soldering: PCB footprints

**Footprint information for reflow soldering of TSSOP16 package** **SOT403-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.650 | 0.750 | 7.200 | 4.500 | 1.350 | 0.400 | 0.600 | 5.600 | 5.300 | 5.800 | 7.450 |

*sot403-1_fr*

**Fig 20. PCB footprint for SOT403-1 (TSSOP16); reflow soldering**

# 16. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged-Device Model |
| dI²C-bus | differential Inter-Integrated Circuit bus |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I²C-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| LED | Light Emitting Diode |
| SMBus | System Management Bus |

# 17. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9616 v.1 | 20131002 | Preliminary data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 19. Contact information

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