APPLICATION NOTE

Bus-Controlled Autosync Deflection Controller TDA4853/54

AN97072

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Application Note AN97072

Abstract

In this application note a pin by pin description of the new Bus-Controlled Autosync Deflection Controller TDA4853 and TDA4854 is given. One can find a summary of its specification and the internal pin specification, function description and drawings to illustrate the text. Also some layout and application proposals are given.

Purchase of Philips I^2C components conveys a license under the I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

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Bus-Controlled Autosync Deflection Controller TDA4853/54

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Summary

In this application note the new Bus-Controlled Autosync Deflection Controller TDA4853 and TDA4854 are described.
The TDA4853 is intended for 14” and 15” monitors. The TDA4854 is intended for 17” up to 21” monitors where also dynamic focus wave forms are required.
Basically the TDA4853 and TDA4854 are the successors of the successful TDA4858 and TDA4855. Besides the integration of the I^2C bus with its internal DAC’s also some extra functions are incorporated like extended geometry control, line parabola, size modulation etc.

The IC is described pin by pin.
For each pin a summary of its specification and the internal pin specification is given. Furthermore the purpose and functioning of this pin is described by some text, there where useful a drawing is given in illustrating the text.
For some pins an application proposal is given.
As performance greatly depends on a good layout, recommendations are given where necessary.

With the aid of this IC a monitor that combines high performance to low cost can be build. One example is the SLE promotion monitor CCM420 described in application note AN97032.

CONTENTS

1. INTRODUCTION

The bus-controlled autosync monitor deflection controllers TDA4853/54 (bus-ASDC) are the successor types of autosync deflection controllers TDA4855/58 (ASDC). Main differences of the bus-ASDC, compared to the ASDC, are:

- I^2C-bus driven extended geometry adjustments and functions, including stand-by mode;
- horizontal frequency range extended to 15-130kHz; vertical frequency range is 50-160Hz;
- combined horizontal/vertical focus section;
- moiré cancellation;
- TV/VCR mode.

The IC pinning (32-pin shrink-DIL) of both TDA4853 and TDA4854 are shown in Figure 1.1 and Figure 1.2, with positive and negative current directions indicated.

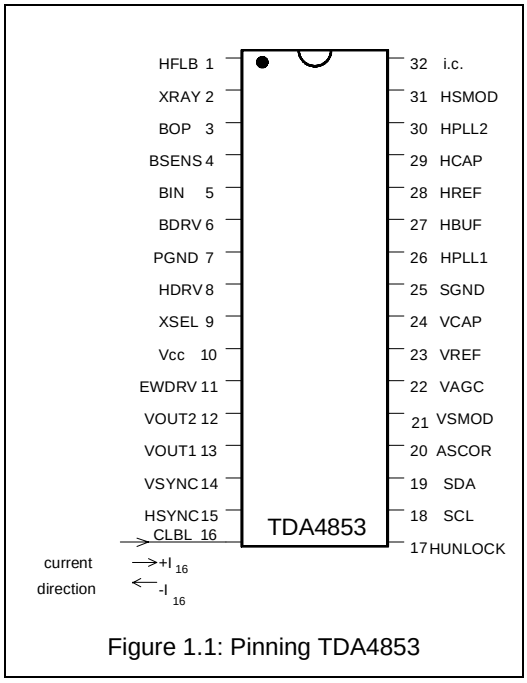


Figure 1.1: Pinning TDA4853

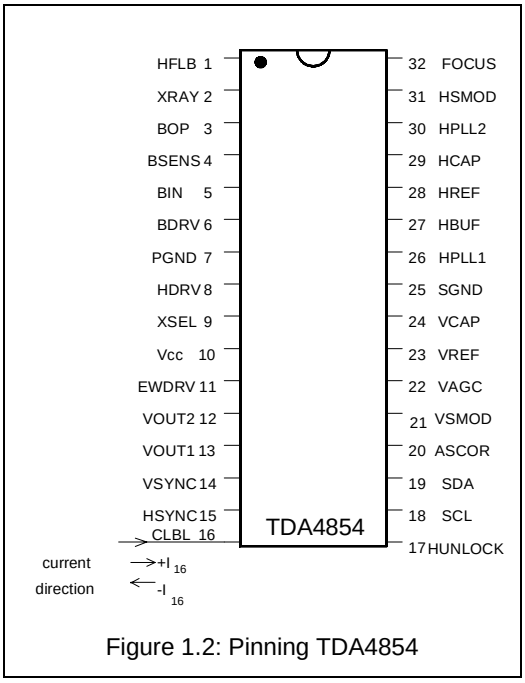


Figure 1.2: Pinning TDA4854

All IC references are from its data sheet of 1997 April 25.

2. PIN 1: HFLB

2.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{HFLB} positive clamping level	I_{HFLB} = 5 mA	-	5.5	-	V
V_{HFLB} negative clamping level	I_{HFLB} = -1 mA	-	-0.75	-	V
I_{HFLB} positive clamping current		-	-	6	mA
I_{HFLB} negative clamping current		-	-	-2	mA
V_{HFLB} slicing level	I_{HFLB} = 5 mA	-	2.8	-	V

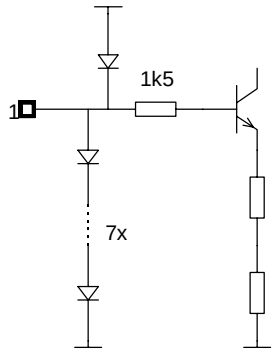


Figure 2.1: Internal pin configuration HFLB

2.2 Description

The horizontal flyback input HFLB is used for the PLL2 phase detector, that compares the flyback pulse to the horizontal oscillator's saw-tooth voltage. The PLL2 detector compensates for the delay in the external deflection circuit by adjusting the phase of the horizontal drive output pulse (HDRV).

2.3 Application

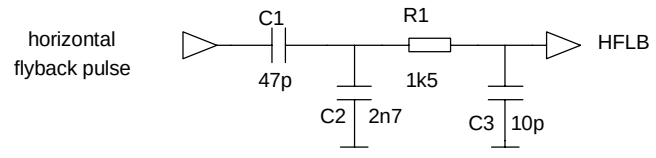


Figure 2.2: Application HFLB

HFLB is connected to a converted horizontal flyback pulse of about 15 V_{pp}. Figure 2.2 shows the application of HFLB. The conversion of about 1100 V_{pp} to 15 V_{pp} is done by the fraction C1\C2. Resistor R1 limits the current and C3 is applied for high frequency filtering.

3. PIN 2/9: XRAY

3.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{XRAY} slicing level		6.22	6.39	6.56	V
$t_{W(XRAY)}$ minimum trigger pulse width		20	-	-	µs
$R_{in(XRAY)}$	$V_{XRAY} < 6.38\ V + V_{BE}$	500	-	-	kΩ
	$V_{XRAY} > 6.38\ V + V_{BE}$	-	5	-	kΩ

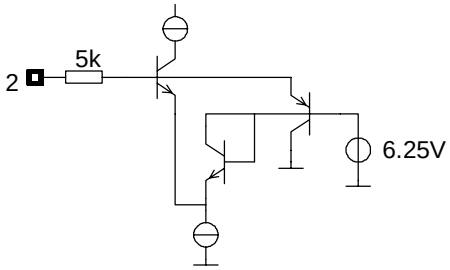


Figure 3.1: Internal pin configuration XRAY

3.2 Description

The XRAY protection input consists of a voltage detector with a precise threshold. If this threshold is exceeded for a certain time, control bit SOFTST is reset and the IC goes into protection mode. In this mode, the following states are defined:

1. HUNLOCK (pin 17) is floating;
2. Capacitor at HPLL2 (pin 30) is discharged;
3. HDRV (pin 8) is floating;
4. BDRV (pin 6) is floating;
5. VOUT1 and VOUT2 (pin 12 and 13) are floating;
6. CLBL (pin 16) provides continuous blanking.

The possibility to reset the internal XRAY latch via I2C bus depends on the application of pin 9:

a) Pin 9 open or grounded : Same function as TDA4854 V1D (XRAY is reset via control bit SOFTST)

b) with an external resistor from Pin 9 to Pin 10 (VCC):
- No XRAY reset via I2C bus possible
- State of internal XRAY latch is kept for Vcc > 4V
- XRAY latch is reset for Vcc < 1V

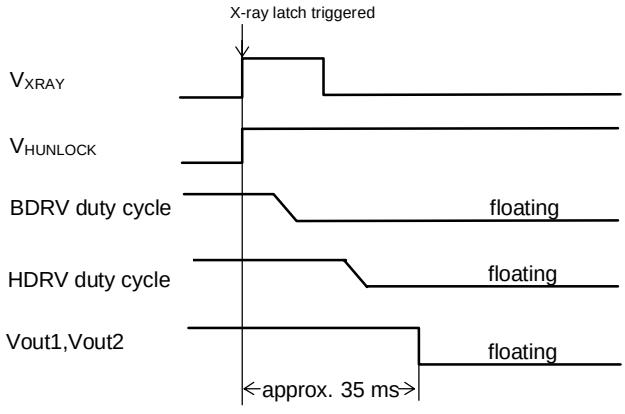


Figure 3.2: Activation of soft-down sequence via pin XRAY

3.3 Application

For XRAY protection, the EHT must be limited to the tube's specification. The flyback pulse from the LOT can be rectified and fed to XRAY via a divider, because it is proportional to the EHT. This principle is shown in Figure 3.3. The value for R1 should be dimensioned in such a way that the divider voltage crosses the XRAY threshold if the EHT has reached the specified upper limit. This upper EHT limit is usually 30 kV.

If the XRAY input is not used, it should be grounded.

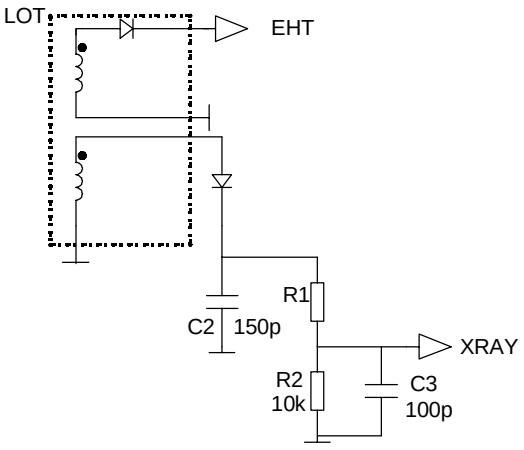


Figure 3.3: XRAY application

4. PIN 3 / 4 / 5 / 6: BOP / BSENS / BIN / BDRV

4.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transconductance amplifier BOP and BIN					
V_{BIN}		0	-	5.25	V
$I_{BIN(max)}$		-	-	± 1	µA
V_{ref} internal non-inverting input OTA		2.37	2.5	2.58	V
V_{BOP}	comparator inv. input voltage range	0	-	5	V
$V_{BOP(min)}$		-	0.4	-	V
$V_{BOP(max)}$	I_{BOP} < 1 mA (internal prot. circuit clamp level)	5.0	5.3	5.6	V
$I_{BOP(max)}$		-	± 500	-	µA
g_{OTA}	first pole at 5 MHz (second pole if OTA operates as integrator)	30	50	70	mS
$G_{open, DC}$ (V_{BOP}\V_{BIN})	C_{BOP} = 4.7 nF, no resistive load	-	86	-	dB
$C_{BOP(min)}$		4.7	-	-	nF
Voltage Comparator BSENS					
V_{BSENS}	comparator noninv. input voltage range and OTA output	0	-	5	V
$V_{BSENS, stop}$	capacitive load; I_{BSENS} = 0.5 mA.	0.85	1.0	1.15	V
IBSENS, discharge	V_{BSENS} > 2.5 V	4.5	6.0	7.5	mA
$V_{BSENS, restart}$	fault condition	1.2	1.3	1.4	V
$C_{BSENS(min)}$		2	-	-	nF
$I_{BSENS(max)}$	discharge disabled (leakage current)	-	-	-2	µA
Open Collector Output Stage BDRV					
$I_{BDRV(max)}$		20	-	-	mA
$I_{BDRV, leak}$	V_{BDRV} = 16 V	-	-	3	µA
$V_{BDRV, sat}$	I_{BDRV} < 20 mA	-	-	300	mV
$t_{off(min)}$	.	-	250	-	ns
$t_{d, BDRV}$	V_{HDRV} = 3 V; V_{BDRV} = 3 V.	-	500	-	ns

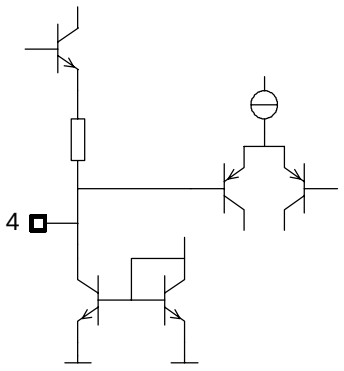


Figure 4.1: Internal pin configuration BSENS

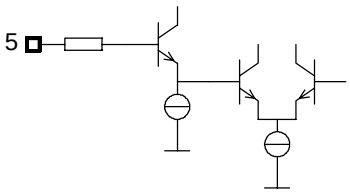


Figure 4.2: Internal pin configuration BIN

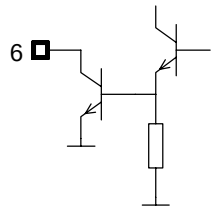


Figure 4.3: Internal pin configuration BDRV

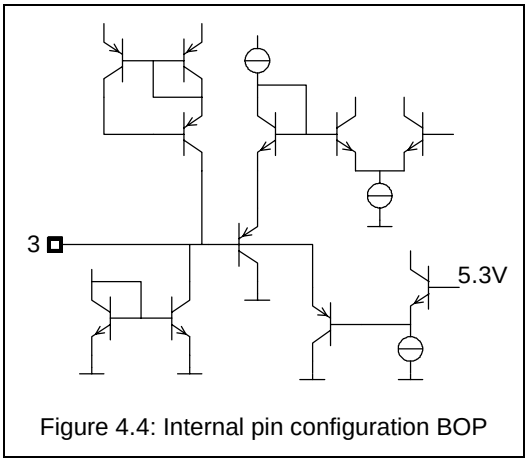


Figure 4.4: Internal pin configuration BOP

4.2 Description

The B+ function block is built up as shown in Figure 4.5. BIN is fed to the inverting input of the OTA. The OTA output is connected to BOP. An internal clamp diode (5.3V) prevents BOP from too high voltages. Also, the output is compared to BSENS. The output of this comparator sets the flip-flop that drives the open collector stage for BDRV. The flip-flop is reset by HDRV. The flip-flop is an edge-triggered device. The recommended value for the load resistor for BDRV is 470Ω.

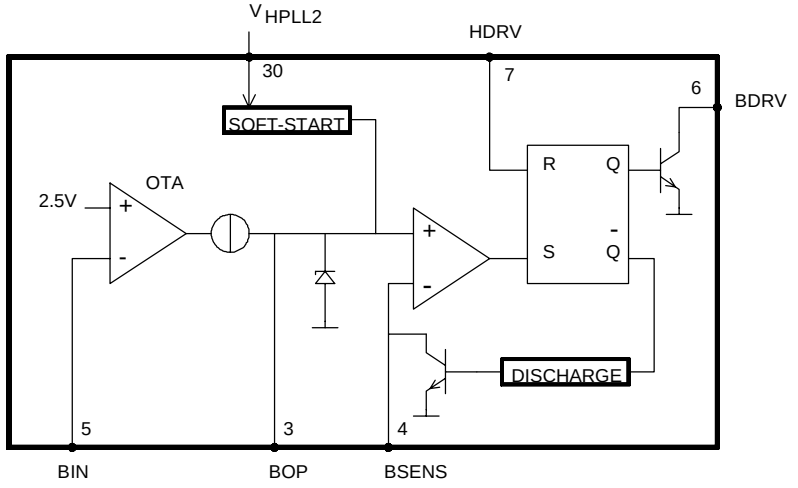


Figure 4.5: Internal diagram B+ control block

4.3 Application

The B+ function block can be used for many different deflection topologies. Two common applications are the combined deflection/EHT circuit for 14”/15” monitors (Figure 4.6) and the deflection generator with buck-converter (Figure 4.7). Another application is the deflection generator with boost-convertor, however this application is not tested (Figure 4.8). For a more detailed description and other applications, see Application Note AN96052: ‘B+ Converter Topologies for Horizontal Deflection and EHT Generators’ (see ref. 6).

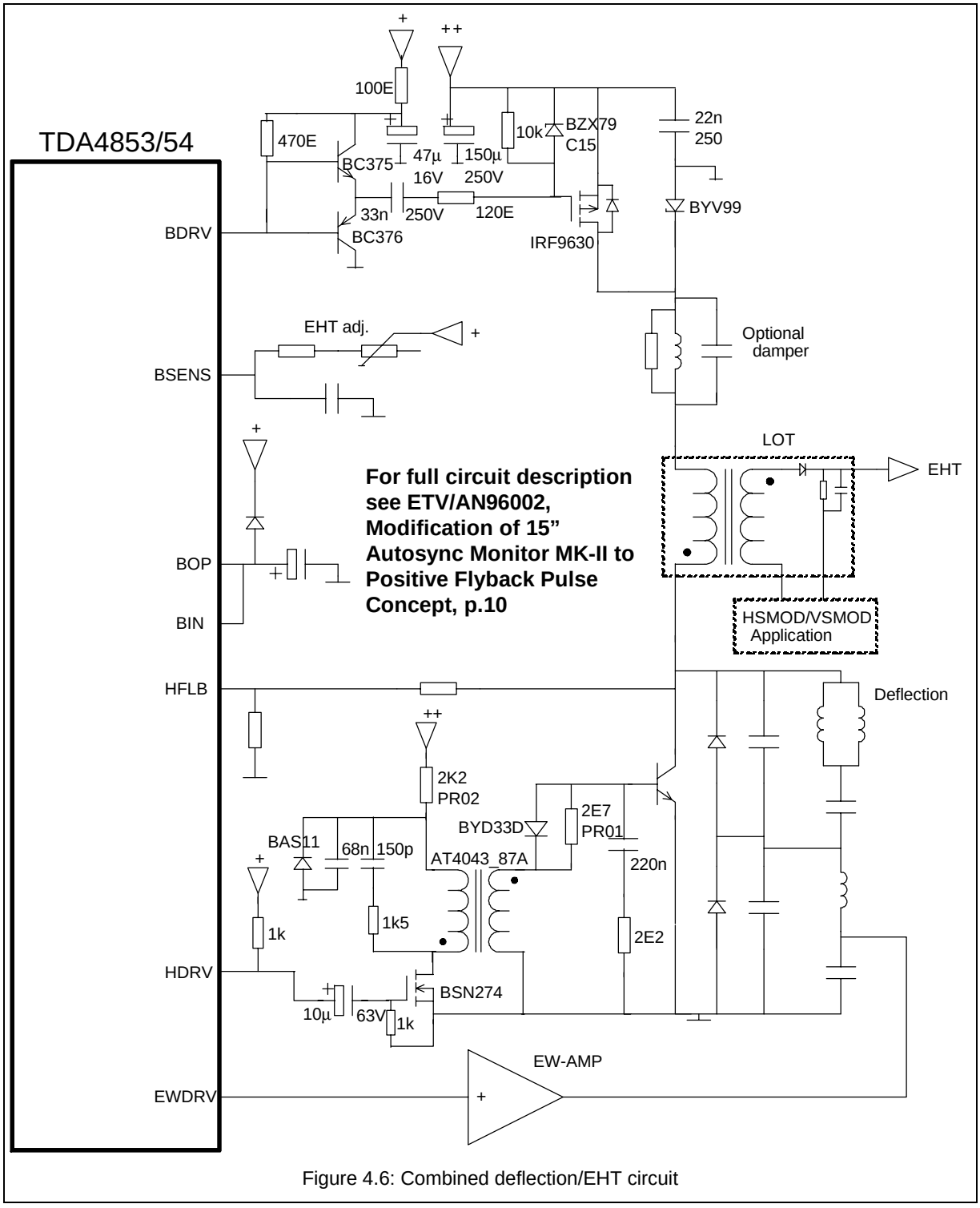


Figure 4.6: Combined deflection/EHT circuit

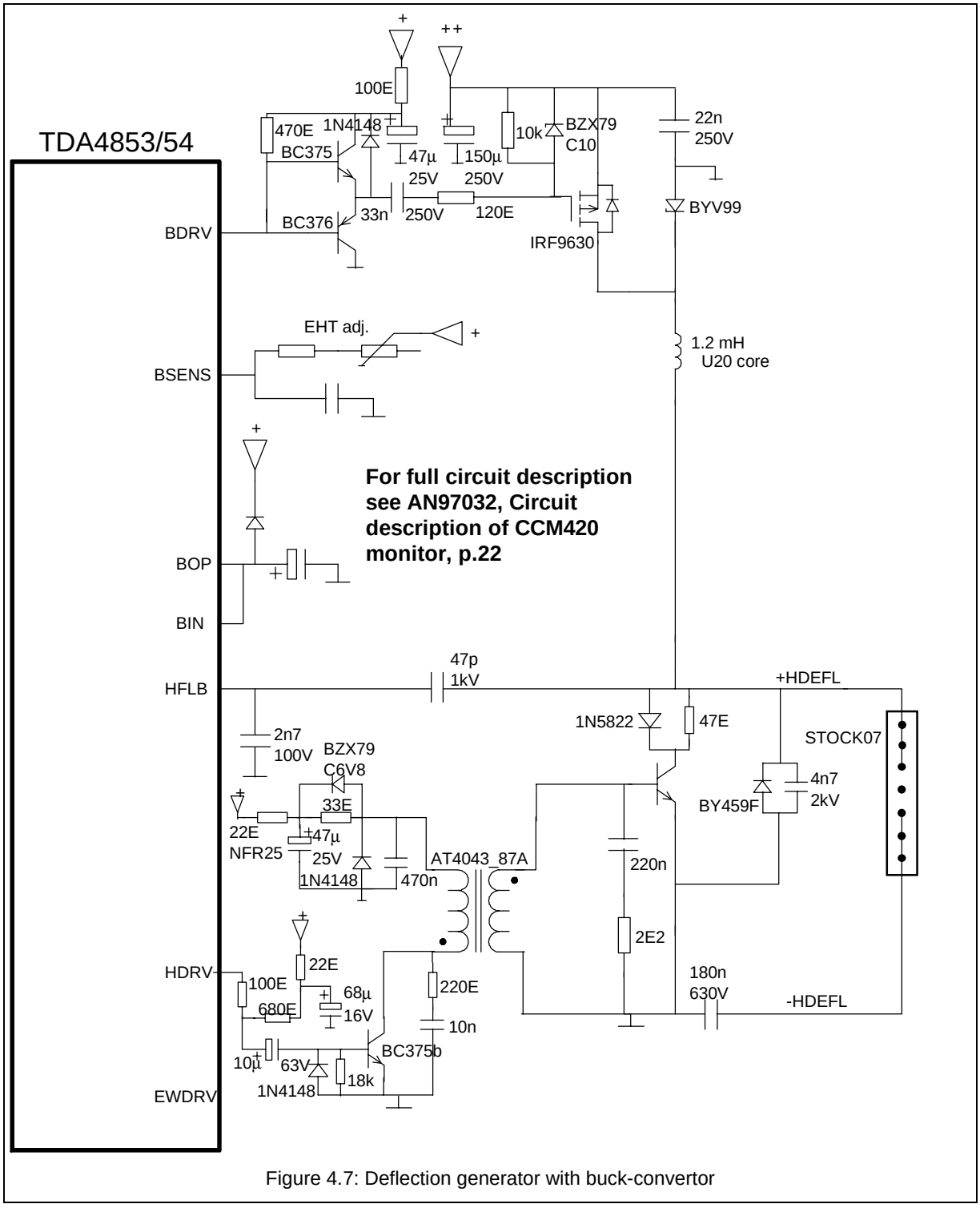


Figure 4.7: Deflection generator with buck-convertor

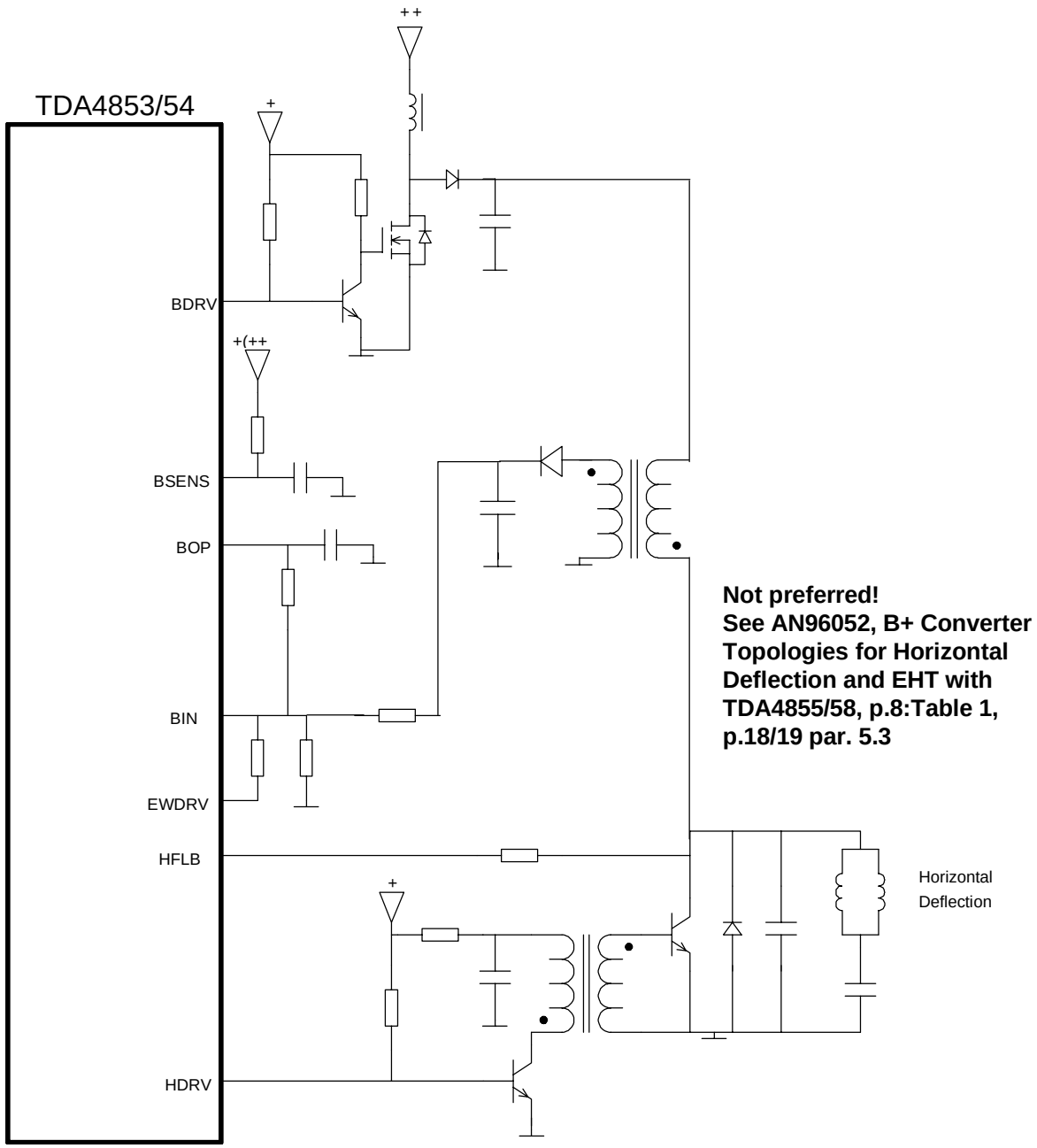


Figure 4.8: Deflection generator with boost-converter

4.4 Lay-out

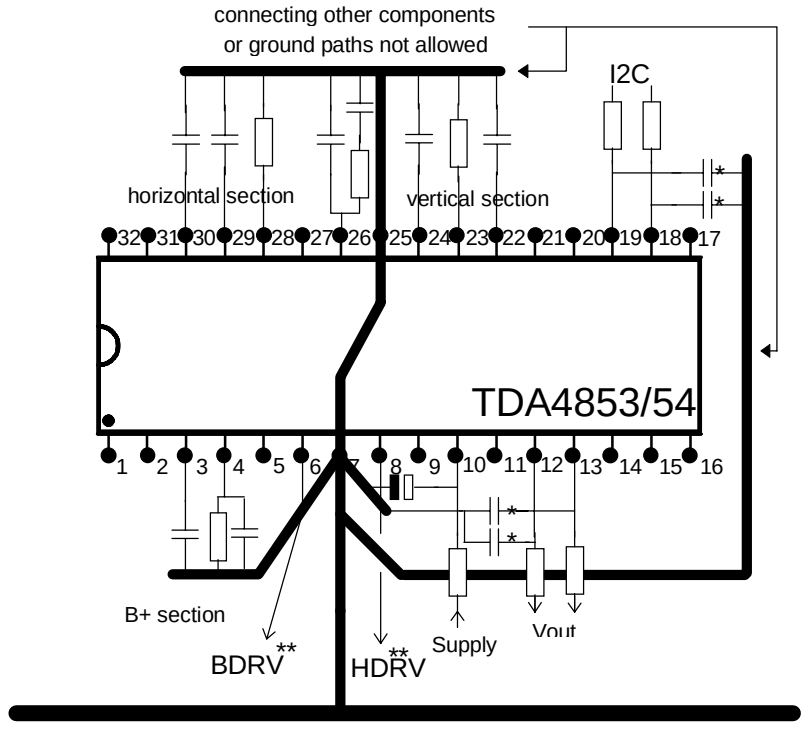
The PCB track that is connected to BIN should be as short as possible in order to limit EMI. This means that, if a resistor is connected to BIN, this resistor should be as close to pin BIN as possible.

5. PIN 7/25: PGND/SGND

5.1 Description

Power ground PGND is connected to the substrate and signal ground SGND must be connected externally to PGND.

5.2 Application / Lay-out



* Optional EMS capacitors

** To avoid crosstalk PCB-tracks of BDRV and HDRV must not “see” each other.

Figure 5.1: Ground lay-out

For optimum performance, ground tracks should be routed as shown in Figure 5.1. Only one connection to other ground tracks of the PCB is allowed.

6. PIN 8: HDRV

6.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{HDRV, sat}$	I_{HDRV} = 20 mA	-	-	0.3	V
	I_{HDRV} = 60 mA	-	-	0.8	V
$I_{HDRV,leak}$	V_{HDRV} = 16 V	-	-	10	µA
$t_{HDRV,off}$ / t_H	I_{HDRV} = 20 mA, f_H = 31.45 kHz	42	45	48	%
	I_{HDRV} = 20 mA, f_H = 58 kHz	45.5	48.5	51.5	%
	I_{HDRV} = 20 mA, f_H = 110 kHz	49	52	55	%

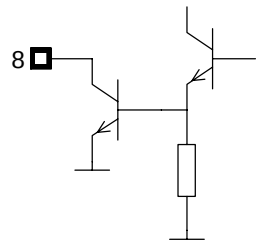


Figure 6.1: Internal pin configuration HDRV

6.2 Description

The horizontal drive pulse (HDRV) is an open collector output that can directly drive the driver transistor. Optimised drive conditions are achieved over the whole frequency range by the slightly frequency-dependent duty cycle. The output duty cycle will decrease if the supply voltage V_{HPLL2} drops below 3 V and passes into a floating state if V_{HPLL2} decreases to 1.7 V.

6.3 Application

A typical 17” application is shown in Figure 6.2. For a more detailed description of this horizontal drive application, see application note AN96091: ‘Low Power and Low Cost Horizontal Drive Circuits with U15 Core’ (see ref. 5).

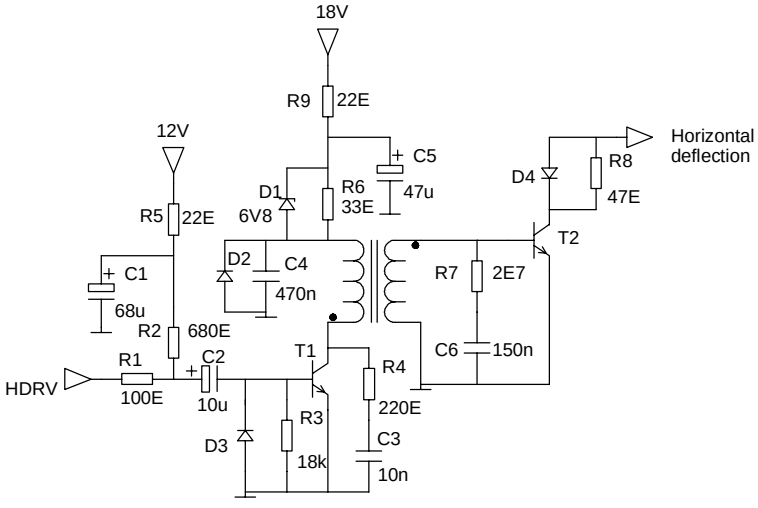


Figure 6.2: Application HDRV

7. PIN 10: V_{cc}

7.1 Characteristics / Internal Configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{cc} normal mode		9.2	-	16	V
V_{cc} activation continuous blanking mode	V_{cc} decreasing from 12 V	8.2	8.6	9.0	V
$V_{cc(min)}$ continuous blanking mode	V_{cc} decreasing from 12 V	2.5	3.5	4.0	V
V_{cc} disable HDRV, BDRV, VOUT1/2 and HUNLOCK, SOFTST set	V_{cc} decreasing from 8.2 V typ. via SOFTST	7.7	8.1	8.5	V
V_{cc} enable HDRV, BDRV, VOUT1/2 and HUNLOCK	V_{cc} increasing from 8 V typ. via SOFTST	7.9	8.3	8.7	V
I_{Vcc}		-	60	-	mA
$I_{Vcc, stand-by}$	SOFTST is reset; $V_{PLL2} < 1$ V; 3.5 V < V_{CC} < 16 V.	-	9	-	mA

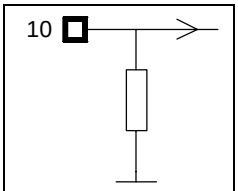


Figure 7.1: Internal pin configuration Vcc

7.2 Description

The internal voltage stabilizer provides all internal references with a stabilised voltage. If V_{cc} drops below (typically) 8.3V or no I^2C-data has been received after power-up, internal soft-start and protection functions disable HDRV, BDRV, VOUT1/VOUT2 and HUNLOCK. Also, the internal I^2C-bus will not generate an acknowledge and SOFTST is reset, forcing the IC into stand-by mode. Figure 7.2 and Figure 7.3 show this shut-down and start-up sequence.

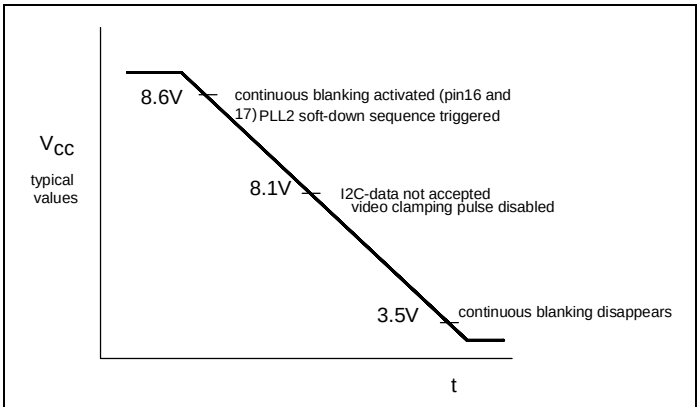


Figure 7.2: Shut-down sequence

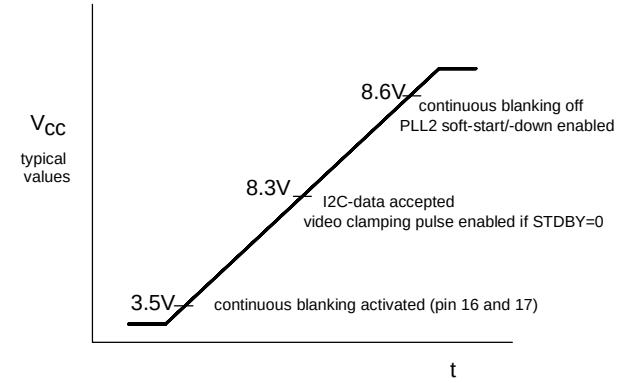


Figure 7.3: Start-up sequence

If, during normal operation, V_{cc} drops below (typically) 8.1 V, protection mode is activated and HUNLOCK passes into protection status (floating). This mode protects the deflection stages and tube during start-up, shut-down and fault conditions. The table at the right shows the measures how the normal mode can be entered after protection has occured. If the soft-start procedure is activated via I^2C-bus, protection actions will be performed in a well-defined sequence. This is the same sequence as pulling HPLL2 to ground, see HPLL2 (pin 30).

EVENT	ACTION
Low supply voltage	increase supply voltage; reload registers; soft start via I^2C-bus.
Power dip (V_{cc} < 8.1V)	reload registers; soft start via I^2C-bus.
XRAY (pin 2) triggered	reload registers; soft start via I^2C-bus.
HPLL2 (pin 30) externally pulled to ground	release HPLL2 (pin 30)

If protection mode is active, several pins are forced into a defined state:

1. HUNLOCK (pin 17) is floating;
2. Capacitor at HPLL2 (pin 30) is discharged;
3. HDRV (pin 8) is floating;
4. BDRV (pin 6) is floating;
5. VOUT1 and VOUT2 (pin 12 and 13) are floating;
6. CLBL (pin 16) provides continuous blanking.

Protection mode can be changed into normal operation by setting bit SOFTST=1.

7.3 Application

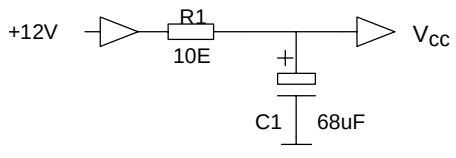


Figure 7.4: Input filter Vcc

The supply pin is connected by a series resistor and must be decoupled by an electrolytic capacitor of about 68uF, as close as possible to the pin itself (see Figure 7.4).

8. PIN 11: EWDRV

8.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{EWDRV,const}$ bottom output Internally stabilised	register HPIN = 0_{DEC} register HCOR = 04_{DEC} register HTRAP = 08_{DEC} register HSIZE = 255_{DEC}	1.05	1.2	1.35	V
$V_{EWDRV(max)}$ maximum output	Clipping if control bit VOVSCN=1 and VPOS is extreme. Corner clipping if vertical saw-tooth > 110% of nominal value	7.0	-	-	V
V_{EWDRV} parabola	Frequency tracking from 15 to 80 kHz control bit FMULT=1, f_H = 31.45 kHz	-	0.72	-	V
	Frequency tracking from 15 to 80 kHz control bit FMULT=1, f_H = 70 kHz	-	1.42	-	V
	Frequency tracking disabled control bit FMULT=0	-	1.42	-	V
δV_{EWDRV} parabola	Linearity error with frequency tracking (FMULT=1)	-	-	8	%
values for V_{HPIN} , V_{HCOR} V_{HTRAP}, V_{HSIZE} below	Nominal vertical settings (unless specified otherwise): *VSIZE=127_{DEC} and VOVSCN=0, VSMOD=0µA, VPC=1, VSC=1, VLC=1, HPC=1.*				
V_{HPIN}	Register HPIN=0_{DEC}	-	0.04	-	V
	Register HPIN=63_{DEC}	-	1.42	-	V
V_{HCOR}	Register HCOR=0_{DEC} control bit VSC=0	-	0.08	-	V
	Register HCOR=31_{DEC} control bit VSC=0	-	-0.64	-	V

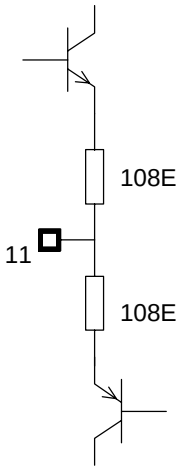


Figure 8.1: Internal pin configuration EWDRV

	Register HCOR=X_{DEC} control bit VSC=1	-	0	-	V
V_{HTRAP}	Register HTRAP=0_{DEC} Control bit VPC=0	-	0.33	-	V
	Register HTRAP=15_{DEC} Control bit VPC=0	-	-0.33	-	V
	Register HTRAP=X_{DEC} Control bit VPC=1	-	0	-	V
V_{HSIZE}	Register HSIZE=0_{DEC}	-	3.6	-	V
	Register HSIZE=255_{DEC}	-	0.13	-	V
V_{HSMOD}	I_{HSMOD} = -120 µA	-	0.69	-	V
	I_{HSMOD} = 0 µA	-	0.02	-	V

8.2 Description

The parabola wave-form of the EW-drive output is controlled by I2C-registers horizontal pincushion (HPIN), horizontal size (HSIZE), corner correction (HCOR) and trapezium correction (HTRAP), as well as analogue input horizontal size modulation (HSMOD). HTRAP can be set/reset by control bit VPC and HCOR by control bit VSC. HPIN, HCOR and HTRAP track with both vertical and horizontal size (VSIZE/HSIZE), vertical position (VPOS) and analogue modulation input HSMOD.

Two modes of EWDRV operation can be chosen via control bit FHMULT:

1. FMULT=1: the EWDRV wave-form tracks with horizontal frequency, used for driving EW diode modulator stages which require a voltage, proportional to line frequency.
2. FMULT=0: EWDRV wave-form does not track with horizontal frequency, used for EW modulators that need a voltage, independent on line frequency (e.g. B+ converter circuits).

Figure 8.2 to Figure 8.5 show the effect of register values on the EWDRV voltage wave-form.

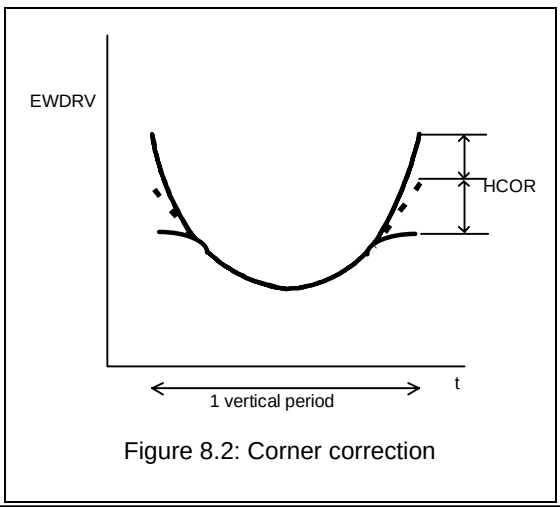


Figure 8.2: Corner correction

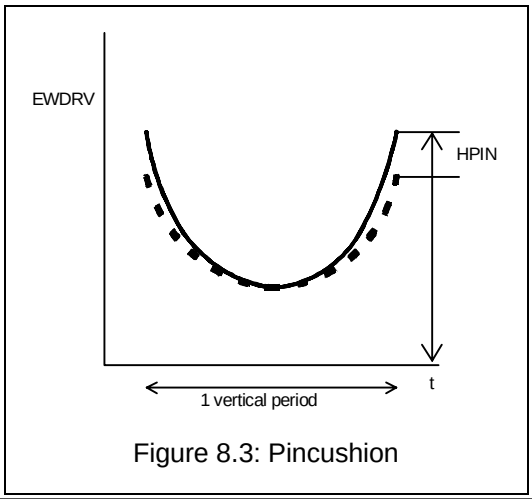


Figure 8.3: Pincushion

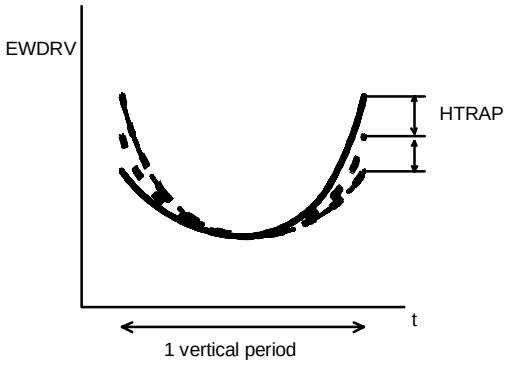


Figure 8.4: Trapezium correction

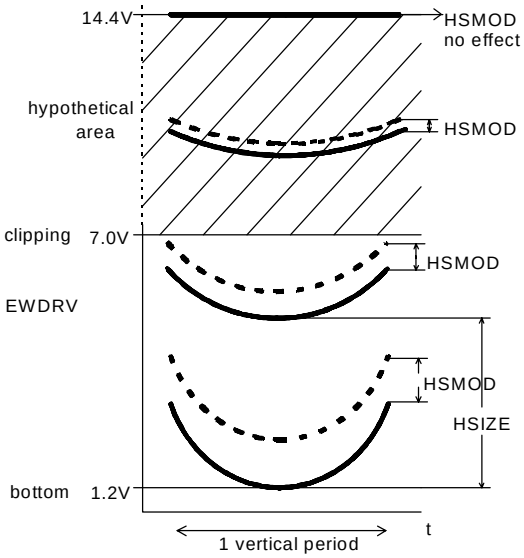


Figure 8.5: Size adjustment and effect of HSMOD

8.3 Application

EWDRV can be used in two modes:

1. With line frequency tracking: FMULT=1, EWDRV is used to feed the amplifier that controls the amplitude of horizontal deflection. This option is used in combined EHT/deflection applications that use the diode modulator. The application is shown in Figure 8.6. This is also described in Application Note 'Modification of 15" Autosync Monitor MK-II to Positive Feedback-Pulse Concept', ETV/AN96002 (see ref. 1), which is an update of Application Note AN95086 (see ref. 2).

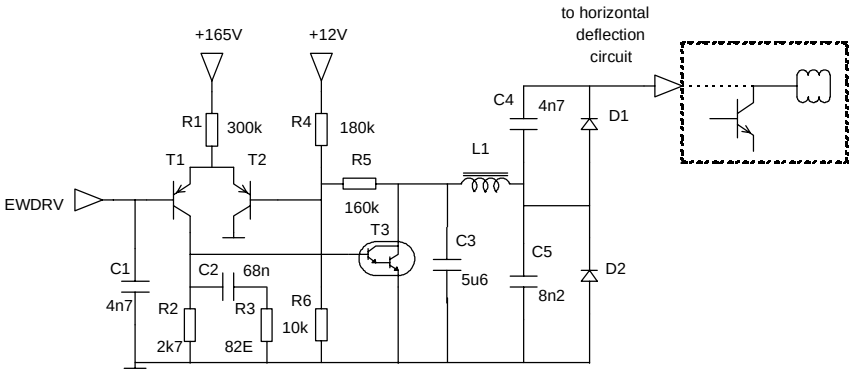


Figure 8.6: Application EWDRV with frequency tracking

2. Without line frequency tracking: FMULT=0, this is used in separate EHT/deflection systems. In this case, the application consists of a resistor to BIN (pin 5), see Figure 8.7. The value for resistor R is typically 56kΩ. For other applications, see Application Notes:
   - 'B+ Topologies for Horizontal Deflection and EHT with TDA4855/58', AN96052, see ref. 6.
   - 'Circuit Description of CCM420 Monitor', AN97032, see ref. 7.

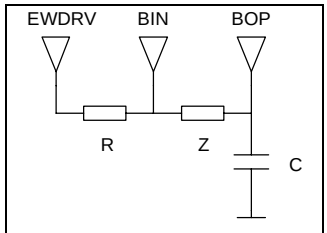


Figure 8.7: Application EWDRV without frequency tracking

9. PIN 12 / 13: VOUT2 / VOUT1

9.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔI_{VOUT} = I_{vout1} - I_{vout2} (peak-peak value)	Nominal vertical settings: *VSIZE=127_{DEC} and VOVSCN=0, VSMOD=0µA, VPC=1, VSC=1, VLC=1, HPC=1.*	0.76	0.85	0.94	mA
$I_{vout1(max)}$, $I_{vout2(max)}$	Control bit VOVSCN=1	0.54	0.6	0.66	mA
V_{VOUT1}, V_{VOUT2}	allowed voltage	0	-	4.2	V
δV_{offset}	Nominal vertical settings	-	-	±2.5	%
$\delta V_{linearity}$	Nominal vertical settings	-	-	±1.5	%
vertical size	Nominal vertical settings; register VSIZE = 0_{DEC}, bit VOVSC = 0.	-	60	-	%
	Nominal vertical settings; register VSIZE = 127_{DEC}, bit VOVSC = 0.	-	100	-	%
vertical size	Nominal vertical settings; register VSIZE = 0_{DEC}, bit VOVSC = 1.	-	70	-	%
	Nominal vertical settings; register VSIZE = 127_{DEC}, bit VOVSC = 1.	115.9	116.8	117.7	%
vertical size	I_{VSMOD} = 0 µA	-	100	-	%
	I_{VSMOD} = -120 µA	-	93	-	%
vertical shift, referred to vertical size of 100%	register VPOS = 0_{DEC}, bit VPC = 0	-	-11.5	-	%
	register VPOS = 127_{DEC}, bit VPC = 0	-	11.5	-	%
	register VPOS = X_{DEC}, bit VPC = 1	-	0	-	%

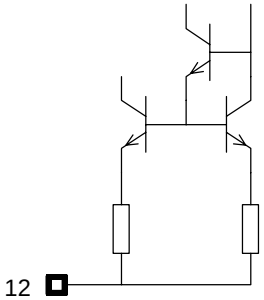


Figure 9.1: Vertical current outputs

9.2 Description

The vertical outputs VOUT1 and VOUT2 are differential current outputs, superimposed on a common bias current source of 300 µA. The amplitude can be adjusted by register VSIZE and modulation input VSMOD for EHT compensation, see Figure 9.2. For the VGA350 mode, the register VOVSCN can activate an increase of 17% in vertical size.

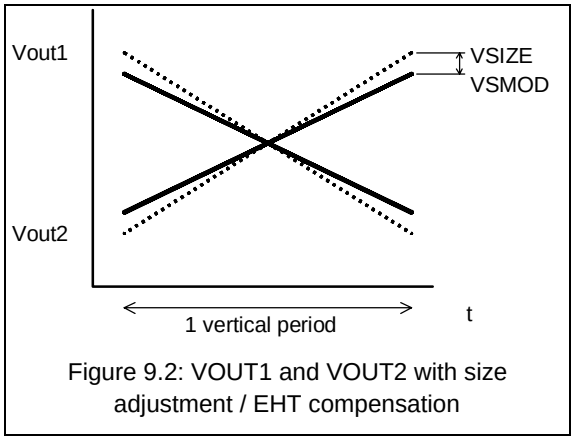


Figure 9.2: VOUT1 and VOUT2 with size adjustment / EHT compensation

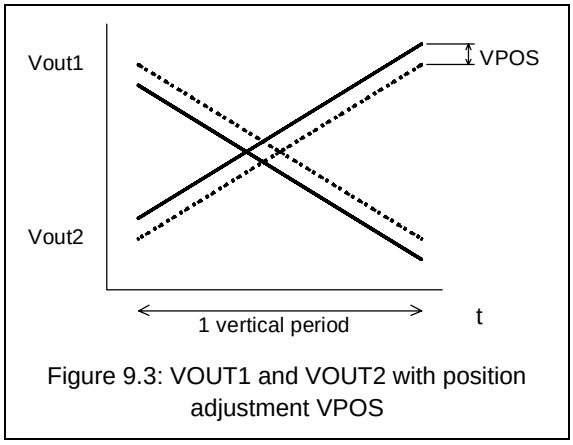


Figure 9.3: VOUT1 and VOUT2 with position adjustment VPOS

Vertical position is adjusted via register VPOS, depicted in Figure 9.3. The vertical size and position also affect the EWDRV output, focus parabola, vertical linearity and vertical linearity balance. In this way, re-adjustment of these parameters is not necessary after altering vertical size or position.

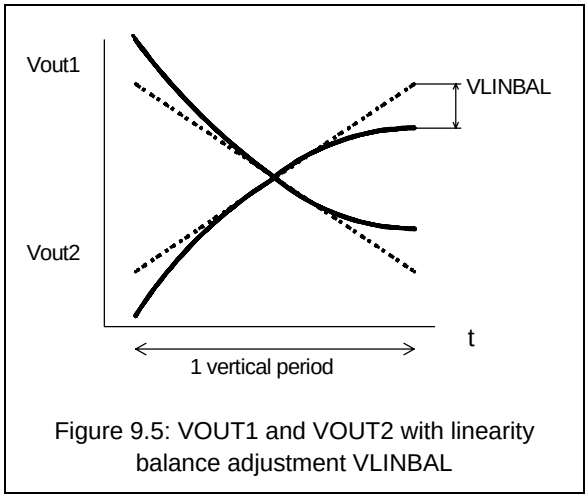


Figure 9.5: VOUT1 and VOUT2 with linearity balance adjustment VLINBAL

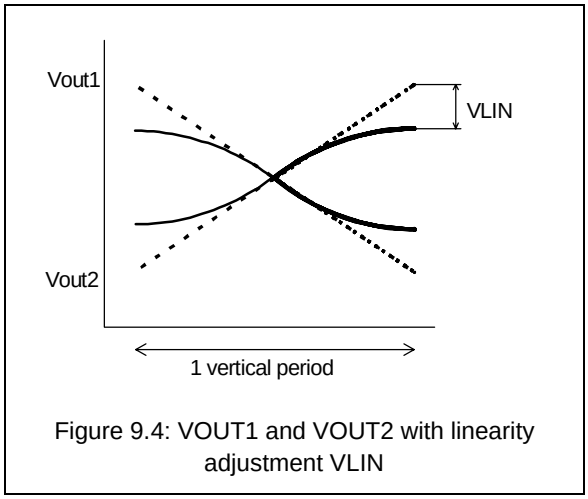


Figure 9.4: VOUT1 and VOUT2 with linearity adjustment VLIN

Vertical linearity is adjustable by register VLIN (see Figure 9.4) and can be switched off by control bit VSC. The same holds for vertical S-correction unbalance, adjusted by register VLINBAL (see Figure 9.5) and switched on/off by control bit VLC.

9.3 Application

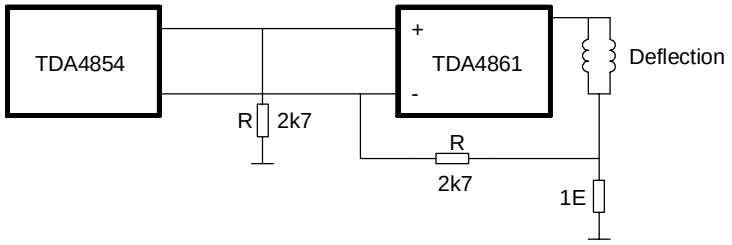


Figure 9.6: Interface VOUT1 and VOUT2 with vertical booster

The differential output currents VOUT1 and VOUT2 can be directly coupled to the vertical deflection boosters with differential current inputs, such as TDA8354 or TDA4866. Other boosters which have the traditional op-amp configuration (e.g. TDA4861) need an interface as shown in Figure 9.6.

9.4 Lay-out

PCB tracks should be as short as possible. The loop area, formed by tracks from VOUT1, VOUT2, BOOSTER_IN1 and BOOSTER_IN2, should be as small as possible. This means that the tracks from VOUT1 to BOOSTER_IN1 and VOUT2 to BOOSTER_IN2 should be as close as possible to one another. If tracks longer than approximately 10 cm are used, both outputs of the TDA4853/54 as well as inputs of the booster should be filtered for EMI prevention.This is shown in Figure 9.7 for a booster with current inputs and in Figure 9.8 for a booster with voltage inputs. C1 and C2 should be as close to the IC's pins as possible.

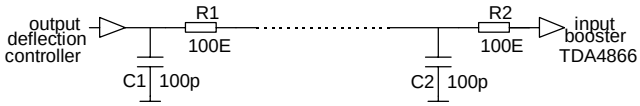


Figure 9.7: EMI prevention with booster current inputs

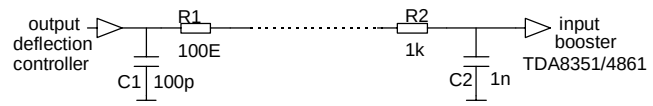


Figure 9.8: EMI prevention with booster voltage inputs

10. PIN 14: VSYNC

10.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{VSYNC}	input signal	1.7	-	-	V
	slicing level	1.2	1.4	1.6	V
I_{VSYNC}	$0 < V_{SYNC} < 5.5V$	-	-	±10	mA
$t_{VSYNC(max)}$		-	-	400	µs
$t_{delay(VPOL)}$	polarity change	0.45	-	1.8	ms

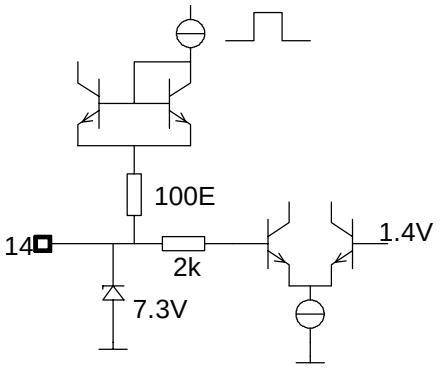


Figure 10.1: Internal pin configuration VSYNC

10.2 Description

Vertical synchronisation input (VSYNC) slices TTL signals at 1.4V. The output of the vertical sync slicer goes into a polarity normaliser. Then it is OR-ed with the vertical sync pulses generated by the vertical integrator which extracts vertical sync from composite sync applied on pin 15, H/C-sync. The output of this OR-function is fed to the vertical oscillator.

10.3 Application

VSYNC is connected directly to the vertical sync input or to the vertical sync output of the microcontroller via a series resistor. Tracks should be kept as short as possible. If tracks are longer than approximately 10 cm, an input filter should be implemented, as shown in Figure 10.2.

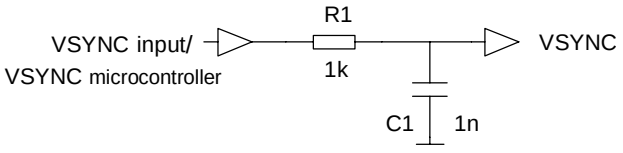


Figure 10.2: Input filter VSYNC

11. PIN 15: HSYNC

11.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HSYNC(max)} \setminus T_{horizontal}$		-	-	25	%
$t_{delay(HPOL)}$		0.3	-	1.8	ms
DC-coupled TTL signals					
V_{HSYNC}	input signal	1.7	-	-	V
	slicing level	1.2	1.4	1.6	V
I_{HSYNC}	V_{HSYNC} = 0.8V	-	-	-200	µA
	V_{HSYNC} = 5.5V	-	-	10	µA
$t_{W\_HSYNC(min)}$		0.7	-	-	µs
t_{rise_HSYNC}		10	-	500	ns
t_{fall_HSYNC}		10	-	500	ns
AC-coupled video signals					
V_{HSYNC}	input signal	-	300	-	mV
	slicing level (50Ω source)	90	120	150	mV
V_{clamp_HSYNC}	top sync clamping level	1.1	1.28	1.5	V
I_{charge_HSYNC}	$V_{HSYNC} > V_{clamp\_HSYNC}$	1.7	2.4	3.4	µA
$t_{W\_HSYNC(min)}$		0.7	-	-	µs
$R_{source(max)}$	duty cycle = 7%	-	-	1500	Ω
r_{diff_HSYNC}	during sync	-	80	-	Ω

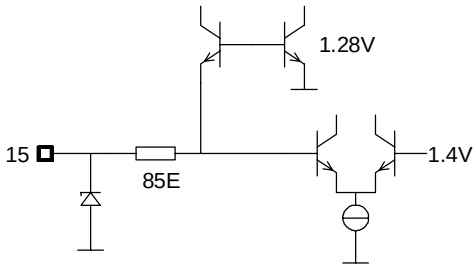


Figure 11.1: Internal pin configuration HSYNC

11.2 Description

Horizontal sync input (HSYNC) can handle both DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signals. DC-coupled TTL signals are sliced at 1.4 V and have a limited input current. AC-coupled syncs are clamped to 1.28 V and sliced at 1.4 V, resulting in a fixed absolute slicing level of 120mV, see Figure 11.2. For both input signals, the separated sync signal is integrated and polarity is normalised. Normalised horizontal sync pulses are fed to the

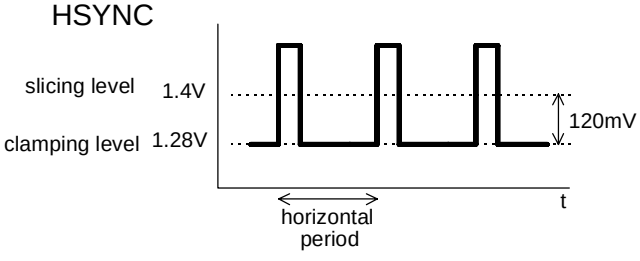


Figure 11.2: HSYNC with AC-coupled input

vertical sync integrator, PLL1 phase detector and frequency locked loop. Equalisation pulses are prohibited for correct functioning of the PLL1 phase detector.

11.3 Application

HSYNC is connected directly to the horizontal sync input, to the horizontal sync output of the microcontroller via a series resistor or to the green colour channel for a Sync-On-Green (SOG) application. Tracks should be kept as short as possible. If tracks are longer than approximately 10 cm, an input filter should be implemented, as shown in Figure 11.3.

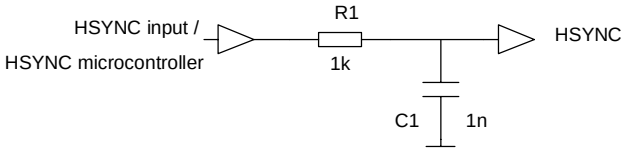


Figure 11.3: Input filter HSYNC

12. PIN 16: CLBL

12.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{clamp}	top level	4.32	4.75	5.23	V
t_{clamp}	V_{CLBL} = 3 V	0.6	0.7	0.8	µs
slope clamp pulse	R_L= 1 MΩ; C_L = 20pF	-	50	-	ns\V
t_{delay_clamp}	trailing edge horizontal sync; control bit CLAMP = 0; V_{CLBL} = 3 V.	-	130	-	ns
$t_{clamp(max)}$	trailing edge horizontal sync; control bit CLAMP = 0; V_{CLBL} = 3 V.	-	-	1.0	µs
$t_{clamp(max)}$	leading edge horizontal sync; control bit CLAMP = 1; V_{CLBL} = 3 V.	-	-	0.15	µs
t_{delay_clamp}	leading edge horizontal sync; control bit CLAMP = 1; V_{CLBL} = 3 V.	-	300	-	ns
V_{CLBL_blank}	top level	1.7	1.9	2.1	V
$t_{CLBL\ blank}$ (also at HUNLOCK)	control bit VBLK = 0	220	260	300	µs
$t_{CLBL\ blank}$ (also at HUNLOCK)	control bit VBLK = 1	300	340	380	µs
V_{CLBL_vscan}	I_{CLBL} = 0	0.59	0.63	0.67	V
I_{CLBL_sink}		2.4	-	-	mA
I_{CLBL_source}		-	-	-3.0	mA

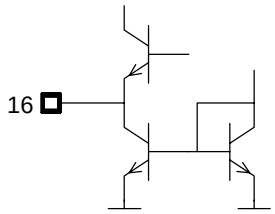


Figure 12.1: Internal pin configuration CLBL

12.2 Description

The video clamping/vertical blanking signal CLBL is a sand-castle pulse which is especially suitable for video controllers, such as the TDA488x-family, but also for direct application to video output stages. The signal consists of two levels (see Figure 12.2):

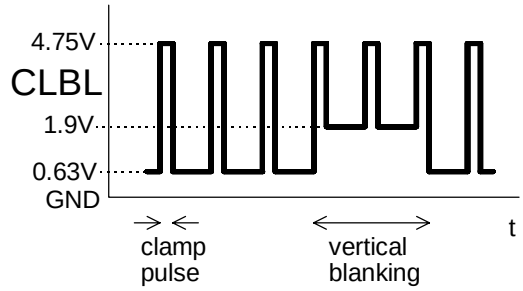


Figure 12.2: Timing diagram CLBL

1. The upper level (4.75 V) is video clamping, triggered by the trailing or leading edge of the horizontal sync pulse (I^2C-selectable by control bit CLAMP). Pulse width is determined by an internal monoflop.
2. The lower level (1.9 V) is vertical blanking, derived directly from the internal oscillator wave-form.

Continuous blanking will be activated if one of the following conditions is true:

1. Soft start of horizontal and B+ drive (HPLL2 (pin 30) pulled down, externally or via I^2C-bus);
2. Frequency-locked loop is in search mode (PLL1 unlocked);
3. No horizontal flyback pulses at HFLB (pin 1);
4. X-ray protection is activated;
5. Supply voltage V_{CC} (pin 10) is below 3.5 V.

Horizontal unlock blanking can be switched off via control bit BLKDIS while vertical blanking and protection blanking remain.

12.3 Application

The CLBL output can be used in two applications:

1. Coupled to the clamping/blanking inputs of video controller TDA488x via a series resistor of 100Ω. These video controllers can extract the vertical blanking with negligible delay. However, if (additional) vertical blanking on grid 1 is wanted, the CLBL is less suitable because of the delay that is caused by filtering out the 4.75V clamping pulses. In this case it is recommended to use the HUNLOCK signal (pin 17).
2. Directly to the output amplifier for black level stabilisation.

13. PIN 17: HUNLOCK

13.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{HUNLOCK}$ low level	internal sink current = 1 mA saturation voltage with locked PLL1	-	-	250	mV
$V_{HUNLOCK,BLANK}$ vertical blanking	internal sink current = 2 mA	0.9	1	1.1	V
$I_{HUNLOCK}$ sink/source current	$V_{HUNLOCK}$ = 1 V	-	-	±2	mA
$I_{HUNLOCK,LEAK}$	$V_{HUNLOCK}$ = 5 V, with PLL1 unlocked and/or protection active	-	-	±5	µA

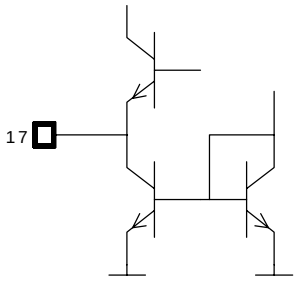


Figure 13.1: Internal pin configuration HUNLOCK

13.2 Description

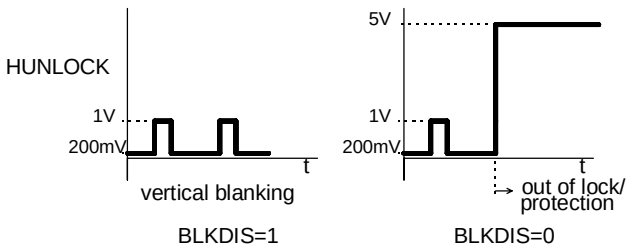


Figure 13.2: HUNLOCK wave-forms

HUNLOCK indicates an out of lock situation of PLL1. This can occur in either search/protection mode or an out of range situation. It can be detected by the microcontroller if an external pull-up resistor is applied to +5V, because HUNLOCK will be floating in case of an out of lock situation. Additionally, HUNLOCK will generate fast vertical blanking signals of 1V. Unlock blanking can be switched off by control bit BLKDIS, while vertical blanking remains. This is necessary for enabling on-screen display in case of missing/wrong sync. HUNLOCK signals are depicted in Figure 13.2.

13.3 Application

The HUNLOCK pin can be used for three purposes:

1. fast vertical blanking at grid1 during normal operation. The 1 V pulse is fed via R3 + R4 and amplified by transistor T1. Note: in this situation transistor T2 is fully conducting.
2. protection blanking ; HUNLOCK is floating and pulled up by R2. The output voltage of 5V is determined by the ratio of R2 and R3+R4. In this situation transistor T2 is blocked and consequently Vg1 will drop quickly to -200 Volt, blanking any picture completely.
3. Information to the microprocessor. Note: The vertical blanking of 1Volt will not be recognized by an input of the microprocessor. Note: If the microprocessor needs 3.3V on its input, the dashed connection should be used.

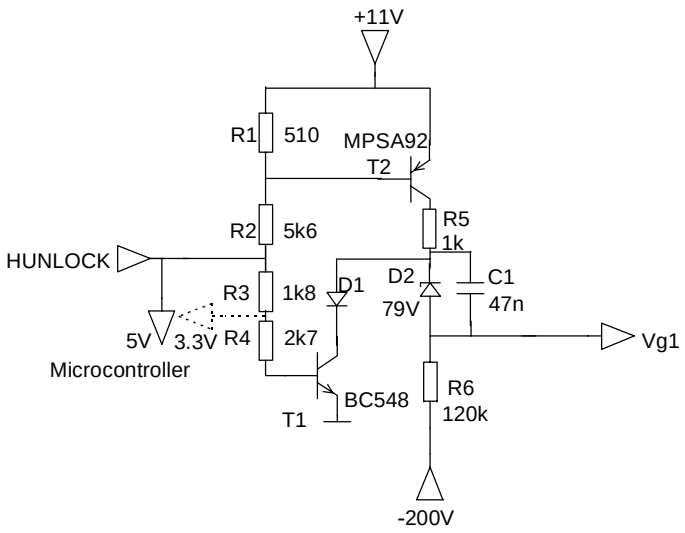


Figure 13.3: HUNLOCK application with Vg1

Full grid1 blanking will also occur when the 11 Volt supply is lowered. For good spot suppression at power switch off, it is recommended to connect the supply of the circuit in Figure 13.3 to the supply of the vertical output stage, because this 11V disappears quicker than the supply voltage of the TDA4853/54.

14. PIN 18 / 19: SCL / SDA

14.1 Internal configuration

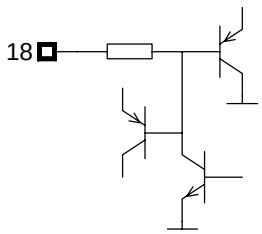


Figure 14.1: Internal pin configuration SCL

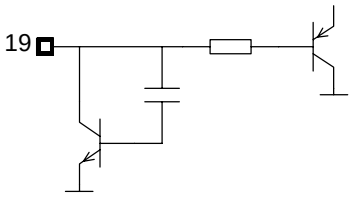


Figure 14.2: Internal pin configuration SDA

14.2 Description

The characteristics and application of I^2C-bus clock input (SCL) and data input (SDA) are described in detail in the Philips data handbook IC12: 'I^2C Peripherals' (see ref. 3).

14.3 Application

The I^2C inputs are connected via a series resistor to the SDA/SCL lines of the master. If the I^2C-bus is controlled by a PC, software and an interface-board are necessary. This software and interface are described in Laboratory Report ETV8835: 'User's Guide to I^2C-bus Control Programs' (see ref. 4).

If register contents are changed during the vertical scan, this might result in a visible interference on the screen. The cause for this interference is the abrupt change of picture geometry which takes effect at random locations within the visible picture. To avoid this kind of interference, at least the adjustment of the critical geometry parameters HSIZE, HPOS, VSIZE and VPOS should be synchronized with the vertical flyback. This should be done in such a way, that the adjustment change takes effect during the vertical blanking time. For very slow I2C bus interfaces, it might be neccessary to delay the transmission of the last byte (or only the last bit) of a I2C message until the start of V-sync or V-blanking.

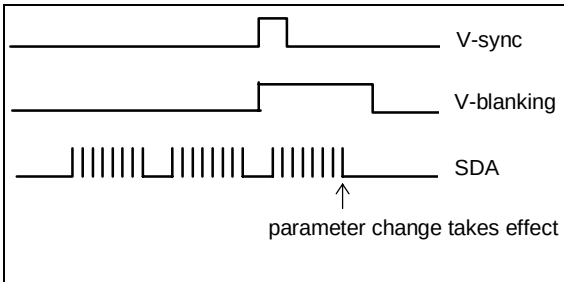


Figure 14.3: I2C-control

15. PIN 20: ASCOR

15.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ASCOR} maximum output		-	6.5	-	V
V_{ASCOR} centre output		-	4.0	-	V
$V_{ASCOR.min}$ minimum output		-	1.9	-	V
V_{ASCOR} maximum output swing		-	4	-	V_{pp}
I_{ASCOR} maximum output current		-	-1.5 +0.05	-	mA
V_{HPARAL} $V_{HPINBAL}$ values below	Nominal vertical settings (unless specified otherwise): *VSIZE=127$_{DEC}$ and VOVSCN=0, VSMOD=0µA, VPC=1, VSC=1, VLC=1, HPC=1.*				
$\Delta V_{ASCOR,HPARAL}$ vertical saw-tooth	Register HPARAL=0_{DEC} control bit HPC=0	-	-0.825	-	V_{pp}
	Register HPARAL=15_{DEC} control bit HPC=0	-	0.825	-	V_{pp}
	Register HPARAL=X_{DEC} control bit HPC=1	-	0.05	-	V_{pp}
$\Delta V_{ASCOR,HPINBAL}$ vertical parabola	Register HPINBAL=0_{DEC} Control bit HBC=0	-	-1.0	-	V_{pp}
	Register HPINBAL=15_{DEC} Control bit HBC=0	-	1.0	-	V_{pp}
	Register HPINBAL=X_{DEC} Control bit HBC=1	-	0.05	-	V_{pp}

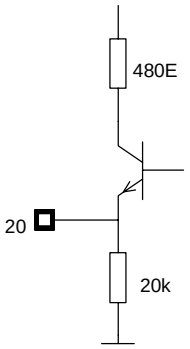


Figure 15.1: Internal pin configuration ASCOR

15.2 Description

Asymmetric EW-correction (ASCOR) is a voltage output for superimposed wave-forms of vertical parabola and saw-tooth. Amplitude and polarity can be controlled by horizontal parallelogram (register HPARAL) and horizontal pin unbalance (register HPINBAL). Figure 15.2 and Figure 15.3 show ASCOR with adjustment of registers HPARAL for parallelogram correction and HPINBAL for vertical centre-line adjustment.

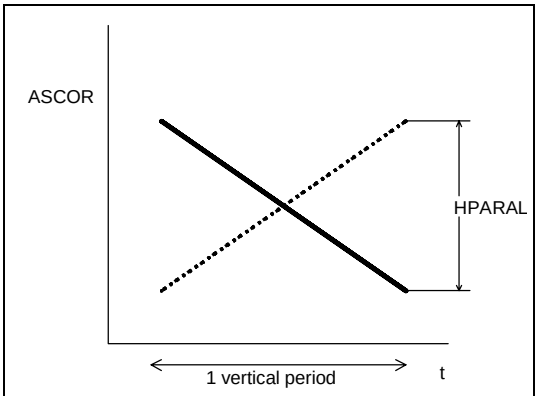


Figure 15.2: ASCOR with parallelogram correction

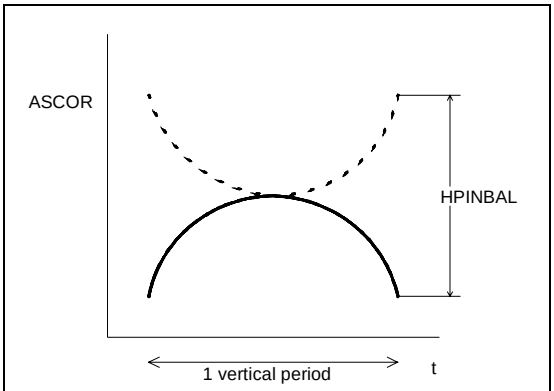


Figure 15.3: ASCOR with pin unbalance correction

Asymmetric correction can be achieved by internal modulation of the PLL2 horizontal phase (control bit ACD=1) or by external DC-shift of horizontal deflection (control bit ACD=0). If a tube is used that does not need asymmetric corrections, ASCOR can also serve other purposes.

15.3 Application

Three different applications for ASCOR are possible:

1. Control bit ACD=0: asymmetric correction is achieved by feeding ASCOR to the DC-amplifier that controls DC-shift of horizontal deflection by means of a DC-shift transformer.
2. Control bit ACD=1: asymmetric correction is achieved by internal modulation of PLL2 horizontal phase. ASCOR pin is left unused, because the correction is performed internally. In this case, the control range of HPARAL and HPINBAL can be increased by the application in Figure 15.4. Start values are: R=330kΩ and C=100nF. Increase R for a smaller adjustment range. The soft-start time is increased to about 400 ms with the values mentioned. **Note**: If bending of the top of the vertical line occurs at maximum HPARAL amplitude, reduce the 12 nF capacitor value until a minimum of 4n7 Farad.
3. Control bit ACD=0: asymmetric correction is not used. If the tube does not need parallelogram or pin unbalance correction, ASCOR pin may be used for other applications, e.g. convergence or vertical focus.

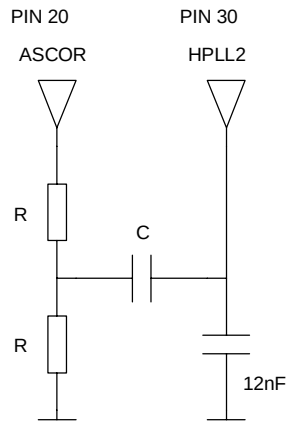


Figure 15.4: Increase HPARAL/HPINBAL control range

16. PIN 21: VSMOD

16.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
vertical size	I_{VSMOD} = 0 µA	-	100	-	%
	I_{VSMOD} = -120 µA	-	93	-	%
$V_{ref(VSMOD)}$		-	5.0	-	V
R_{VSMOD}		300	-	500	Ω
B_{VSMOD}		1	-	-	MHz

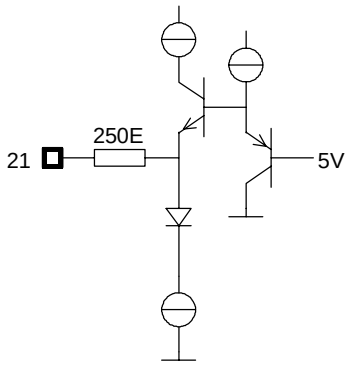


Figure 16.1: Internal pin configuration VSMOD

16.2 Description

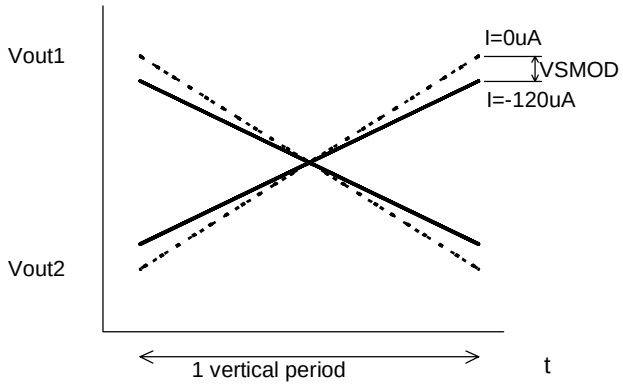


Figure 16.2: Vertical Output Currents as a function of VSMOD

Vertical size modulation (VSMOD) is an analogue modulation input for size compensation with changing EHT. In case of a combined EHT/deflection application, it is used to compensate for load variations. Modulation at this pin will result in a vertical size reduction of 0 - 7%.

Note: The polarity of VSMOD (and HSMOD) is inverted, compared to VAMP (and EWWID) of the TDA4855.

Size reduction is achieved by correcting the differential output currents at VOUT1 and VOUT2. It does not affect EW wave-forms, vertical focus, pin unbalance or parallelogram corrections. Figure 16.2 shows the vertical current outputs as a function of modulation at VSMOD in case of a full white picture on screen.

16.3 Application

If the load of an unstabilized EHT increases, the EHT voltage will decrease and thus, vertical size will increase. This increased size can be compensated for by sinking current from VSMOD. Variation in current at VSMOD from 0 to -120μA will result in a vertical size variation of 0 to -7% of the actual size in the differential output currents. Load variations in the EHT can be compensated for via two possible applications:

1- A parallel capacitor and bleeder are present in the EHT transformer. With a divider and buffer, EHT information can be transferred to VSMOD. This is the best solution, because the signal does not lag in phase. The application at VSMOD can be implemented as shown in Figure 16.3.

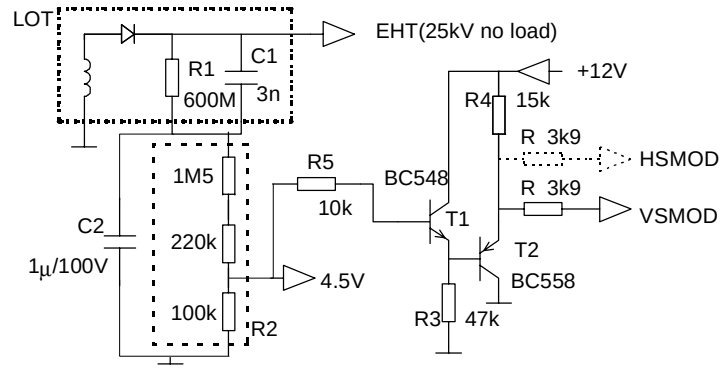


Figure 16.3: VSMOD application with EHT divider

This divider creates a T1 base voltage of 4.8 V, within the range of the voltage at HSMOD. A decrease of EHT voltage will result in a voltage over R, sinking current from HSMOD. The time constants of the divider (C1*R1 and C2*R2) should be equal. The values for R2 and C2 should be recalculated if the LOT contains other component values for R1 or C1. C2 should have a low leakage current (< 0.1 μA). For a full VSMOD control range with a EHT voltage drop of 10% (2.5kV), the value for R will be 3k9.

For an optimised dimensioning of R, follow the next steps:

- Adjust HSMOD application values;
- Display a white bar (about 80% width and 80% height), flashing on/off at about 1Hz, and a white border line for reference (see Figure 16.4);
- Adjust R to an optimised vertical size correction (no displacement in border line on screen) and apply this value as a fixed resistor.

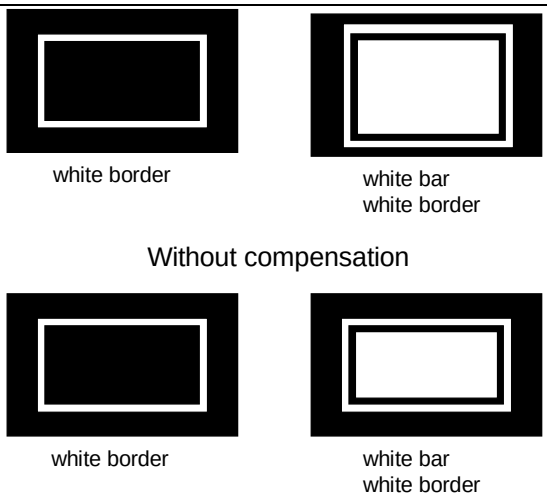


Figure 16.4: Screen view effect VSMOD

2: The footpoint of the EHT transformer (not grounded) can be used for EHT information via a resistor. This solution will, however, result in a VSMOD phase lag and therefor, geometry compensation will not be optimal. The application of VSMOD in this case is depicted in Figure 16.5.

The footpoint of the LOT is set to 5 V, equal to the voltage of HSMOD. A variation in beam current from 0 to 700µA will result in a voltage drop over R1 of 700µ*5k6 = 4V. Now, the value for R2 can be calculated, because an equal voltage drop over R2 should sink 120µA from HSMOD: R2 = 4\120µ = 33kΩ. The time constant τ_1, created by R1* C1, should be between horizontal and vertical period ($\tau_1 \approx 0.5$ ms).

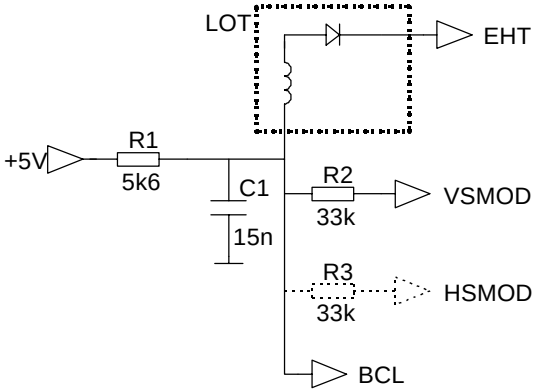


Figure 16.5: Application VSMOD via EHT Current Sense

For an optimised dimensioning of R2, follow the next steps:

- Adjust HSMOD application values;
- Display a white bar (about 80% width and 80% height), flashing on/off at about 1 Hz, and a white border line for reference (see Figure 16.4);
- Adjust R2 to an optimised vertical size correction (no displacement in border line on screen) and apply this value as a fixed resistor.

A slight interaction from VSMOD to HSMOD and vice versa is possible. This VSMOD/HSMOD application concept can also be used for beam current limiting (BCL).

16.4 Lay-out

In both applications, tracks should be as short as possible, especially the track from resistor to VSMOD. This resistor is 'R' in Figure 16.3 and R2 in Figure 16.5. If these tracks are longer then approximately 2 cm, input filtering will be necessary in order to eliminate possible EMI problems. This is done by an input filter, shown in Figure 16.6, where R1 and C1 should be as close as possible to the input pin.

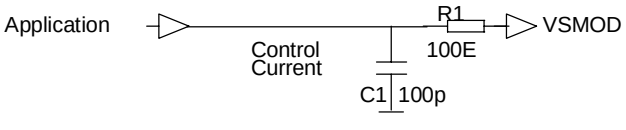


Figure 16.6: EMI filtering VSMOD

17. PIN 22 / 23 / 24: VAGC / VREF / VCAP

17.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{V,\ free\text{-}running}$	R_{VREF} = 22 kΩ C_{VCAP} = 100 nF	40	42	43.3	Hz
$f_{V,\ catching\ range}$	R_{VREF} = 22 kΩ	50	-	160	Hz
$t_{scan\ delay}$ between trigger pulse and start VCAP ramp	control bit VBLK = 0	220	260	300	µs
$t_{scan\ delay}$	control bit VBLK = 1	300	340	380	µs
V_{VREF}		-	3.0	-	V
C_{VAGC}		150	-	220	nF
I_{VAGC}	control bit AGDIS = 0	120	200	300	µA
	control bit AGDIS = 1	-	0	-	µA

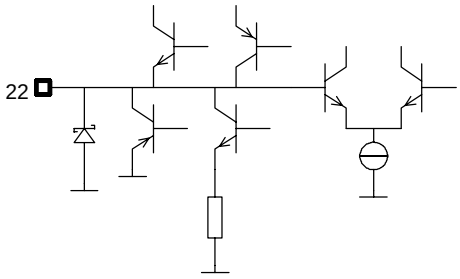


Figure 17.1: Internal pin configuration VAGC

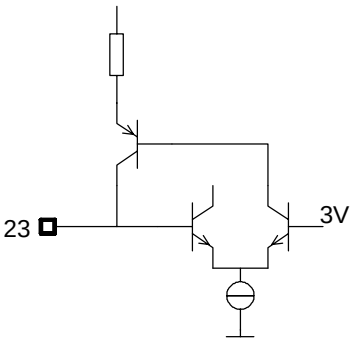


Figure 17.2: Internal pin configuration VREF

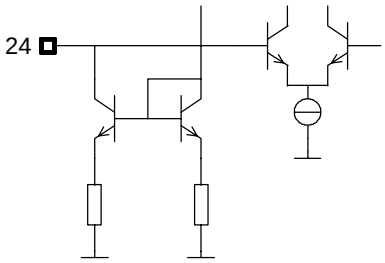
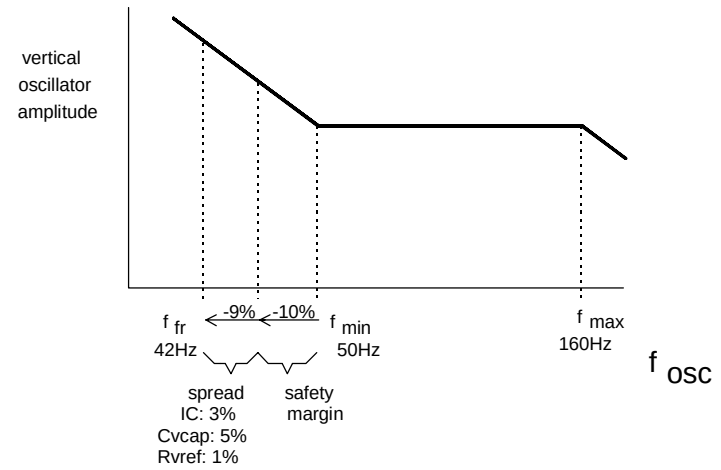


Figure 17.3: Internal pin configuration VCAP

17.2 Description

Vertical automatic gain control is done at VAGC, which can be disabled by resetting control bit AGCDIS. The vertical reference input VREF determines the vertical free-running frequency by connecting a resistor to ground, together with capacitor C_{VCAP} at VCAP.

17.3 Application



$$Cvcap = \frac{1}{10.8*Rvref*f_{fr}} = \frac{1}{10.8*22k*42}$$

$$= 100nF$$

Figure 17.4: Vertical (free-running) frequency

The capacitor C_{VCAP} connected to vertical capacitor VCAP input determines the free-running vertical frequency, together with resistor R_{VREF} (22 kΩ) at VREF. Figure 17.4 shows how to determine the value for C_{VCAP}.

Note: For stable internal references as well as optimised noise and linearity performance, always apply a value of 22kΩ at VREF.

The application of vertical automatic gain control VAGC consists of a capacitor with a value of 150 nF to 220 nF to ground. VAGC should not be loaded externally in order to avoid non-linearities in vertical size. Application of VAGC, VREF and VCAP is shown in Figure 17.5.

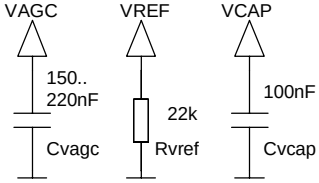


Figure 17.5: Application VAGC/VREF/VCAP

18. PIN 26 / 27 / 28 / 29: HPLL1 / HBUF / HREF / HCAP

18.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HPLL1,lock}$		-	40	80	ms
I_{HPLL1}	level 1 locked mode	-	15	-	µA
	level 2 locked mode	-	145	-	µA
V_{HBUF}	$f_{H(min)}$	-	2.5	-	V
	$f_{H(max)}$	-	0.5	-	V
V_{HREF}		2.43	2.55	2.68	V
$f_{free-running}$ for testing only	R_{HBUF} = ∞; R_{HREF} = 2.4kΩ; C_{HCAP} = 10nF.	30.53	31.45	32.39	kHz
$f_{H(max)}$		-	-	130	kHz

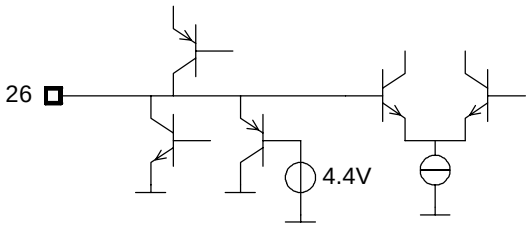


Figure 18.1: Internal pin configuration HPLL1

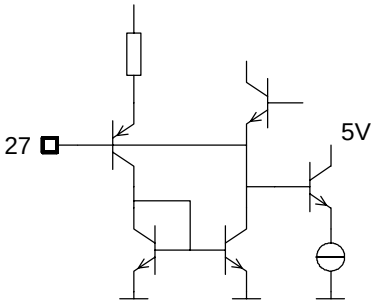


Figure 18.2: Internal pin configuration HBUF

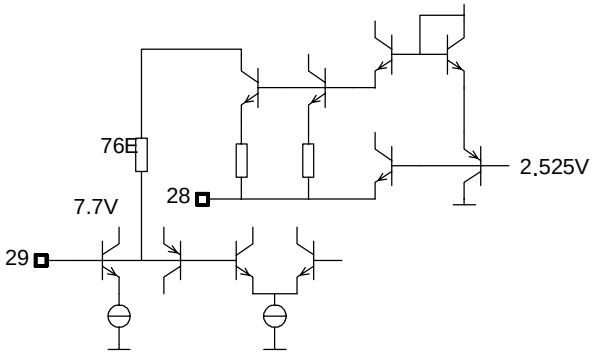


Figure 18.3: Internal pin configuration HREF/HCAP

18.2 Description

HPLL1 is the loop filter input of the horizontal phase locked loop PLL1, that synchronises the horizontal oscillator with HSYNC. If the oscillator frequency deviates more than 4% of HSYNC, PLL1 goes into search mode. After tuning the horizontal oscillator, PLL1 goes into soft-lock mode during $^1/_3$ of a vertical period and then passes into normal PLL operation.

The minimum horizontal frequency is determined by the capacitor at HCAP and resistor at HREF. Because the capacitor value is fixed (10 nF), the minimum frequency is actually determined by resistor R_{HREF} only. Horizontal frequency range is determined by resistor R_{HBUF} from HBUF to HREF. Figure 18.4 shows how to determine minimum and maximum frequency for calculating R_{HREF} and R_{HBUF}. TV-mode is centred around f_{min} (pin HBUF is floating) with a control range of ±10%. This mode is only allowed between 15.625 and 35 kHz.

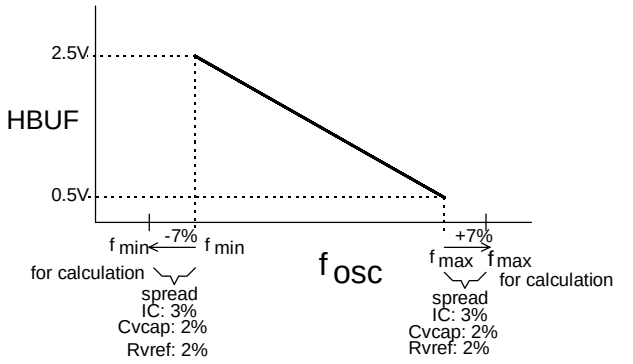


Figure 18.4: Determination minimum/maximum frequency

18.3 Application

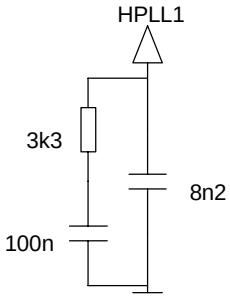


Figure 18.5: Application HPLL1

The PLL1 loop filter is connected to HPLL1 (see Figure 18.5). These values are optimised for low jitter. The scan time for search mode is determined by the 100nF capacitor. It is not allowed to load HPLL1 externally. The application of HBUF/HREF/HCAP is shown in Figure 18.6.

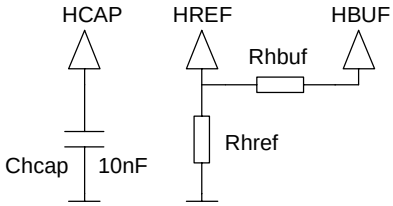


Figure 18.6: Application HREF/HBUF/HCAP

The equations below show how to calculate R_{HBUF} and R_{HREF}.

$$R_{HREF} = \frac{78 * kHz * k\Omega}{f_{min} + 0.0012 * f_{min}^{2}\ [kHz]}$$

$$R_{HBUF} = \frac{R_{HREF} * \frac{78 * kHz * k\Omega}{f_{max} + 0.0012 * f_{max}^{2}\ [kHz]}}{R_{HREF} - \frac{78 * kHz * k\Omega}{f_{max} + 0.0012 * f_{max}^{2}\ [kHz]}} * 0.8$$

Some common values for maximum/minimum frequencies and corresponding values for R_{HBUF} and R_{HREF} are shown in the table at the right.

R_{HREF} [Ω]	f_{min} [kHz]	R_{HBUF} [Ω]	f_{max} [kHz]
5k28	15.625	1k26	56
		900	72
		673	90
3k4	24	1k51	56
		1k02	72
		738	90
2k56	31.45	1k85	56
		1k16	72
		811	90

19. PIN 30: PLL2

19.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ϕ_{PLL2} advance horizontal drive w.r.t. middle horizontal flyback	maximum advance; register HPINBAL=07_{DEC}; register HPARAL=$07_{DEC.}$	36	-	-	%
	minimum advance; register HPINBAL=07_{DEC}; register HPARAL=$07_{DEC.}$	-	7	-	%
I_{PLL2}		-	+75	-	µA
s_{PLL2} (relative sensitivity ϕ_{PLL2}, w.r.t. horizontal period)		-	28	-	mV/%
$V_{HPLL2(max)}$	protection/soft start	-	4.4	-	V
$I_{PLL2,charge}$		-	1	-	µA
Capacity		4.7	12		nF

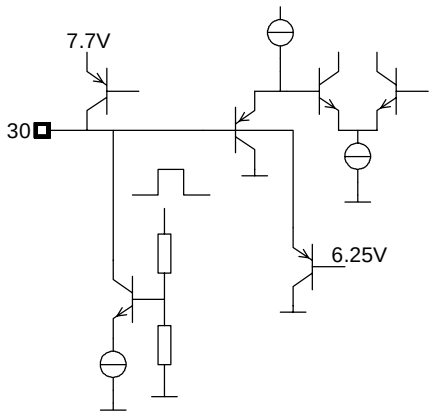


Figure 19.1: Internal pin configuration HPLL2

19.2 Description

The PLL2 phase detector compares the HFLB input to the oscillator's saw-tooth voltage and adjusts the phase of HDRV, compensating for the delay in the external horizontal deflection circuit (e.g. storage time variations). HPLL2 can be used for soft-start, protection and power-down modes by pulling HPLL2 to ground, externally by a DC-current or internally by resetting register SOFTST. Figure 19.2 and Figure 19.3 show the soft-start and soft-down sequences. A soft-start is only performed if the supply voltage is at least 8.2 V.

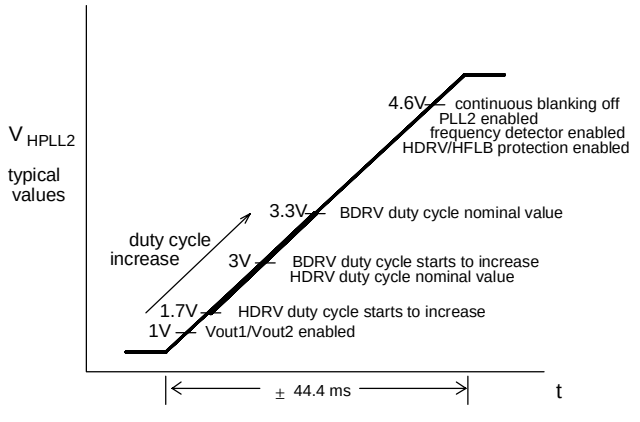


Figure 19.2: Soft-start sequence

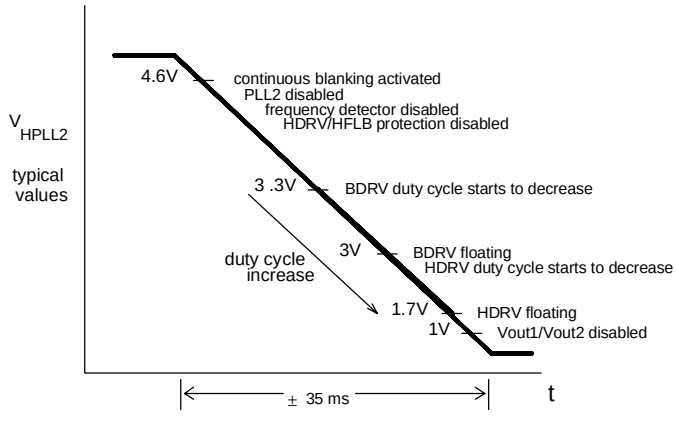


Figure 19.3: Soft-down sequence

19.3 Application

The application of HPLL2 consists of a capacitor of 12 nF to ground, which should not be changed for optimal internal functionality. This filter capacitor determines the soft-start timing.

20. PIN 31: HSMOD

20.1 Characteristics / Internal configuration

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{EWDRV,const}$	I_{HSMOD} = 0 µA HSIZE=255_{DEC}	-	0.02	-	V
	I_{HSMOD} = -120 µA HSIZE=255_{DEC}	-	0.69	-	V
$V_{ref(HSMOD)}$		-	5.0	-	V
R_{HSMOD}		300	-	500	Ω
B_{HSMOD}		1	-	-	MHz

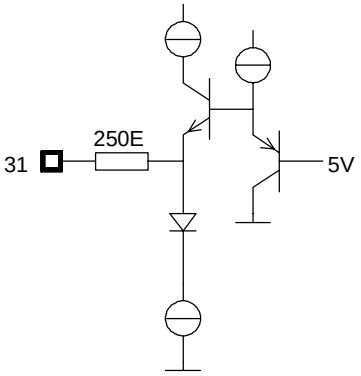


Figure 20.1: Internal pin configuration HSMOD

20.2 Description

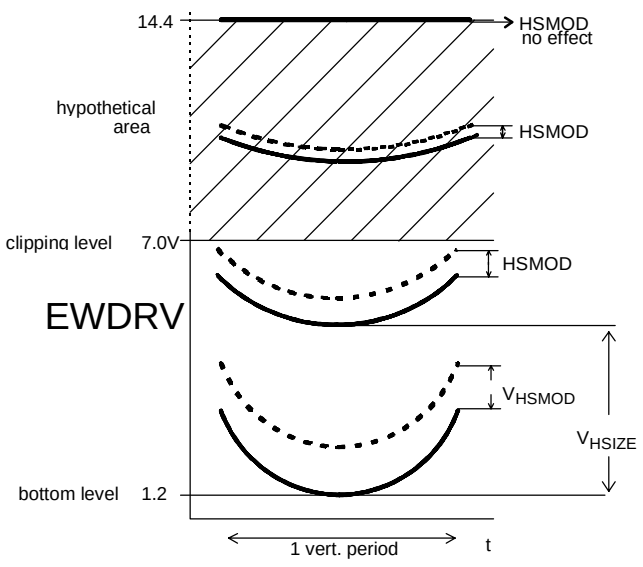


Figure 20.2: EWDRV with modulation at HSMOD

Horizontal size modulation (HSMOD) is an analogue input for horizontal deflection correction. It is used in combined EHT/deflection systems to compensate for ripple in EHT and deflection supply, caused by load variations. Modulation at this input will result in a linear variation at the EW drive output (EWDRV). The control range of this input tracks with the actual value of I^2C-controlled register HSIZE.

Note: The polarity of HSMOD (and VSMOD) is inverted, compared to EWWID (and VAMP) of the TDA4855.

Figure 20.2 shows the EWDRV output as a function of the HSMOD input, depending on the DC-component of EWDRV.

Figure 20.3 shows a screen view, displaying a white bar. The corresponding EWDRV wave-form with EHT compensation via HSMOD is depicted in Figure 20.4.

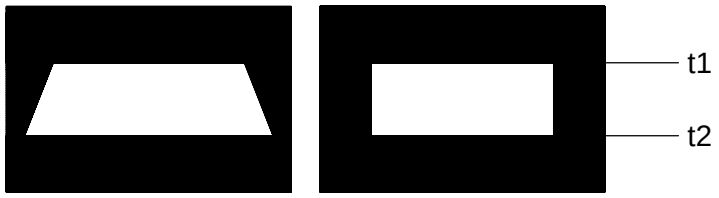


Figure 20.3: White bar on screen without and with compensation at HSMOD

$$V_{HSMOD} = \frac{I_{HSMOD}}{120\mu A} \cdot 0.69V \cdot \left(1 - \frac{V_{HSIZE}}{14.4}\right) \text{;FHMULT=0}$$

$$V_{HSMOD} = \frac{I_{HSMOD}}{120\mu A} \cdot 0.69V \cdot \left(1 - \frac{V_{HSIZE}}{14.4}\right) \cdot \frac{I_{HREF}}{2.36mA} \text{ ;FHMULT=1}$$

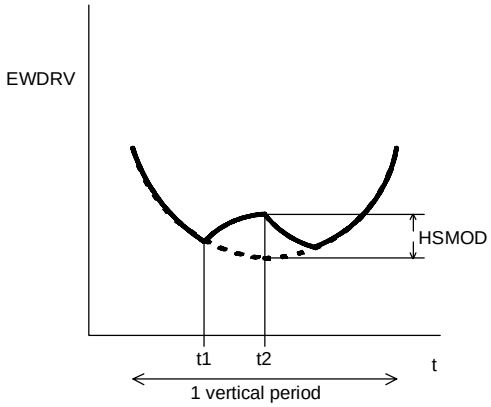


Figure 20.4: EWDRV output with white bar EHT compensation at HSMOD

20.3 Application

If the EHT load increases, the EHT voltage will decrease and thus, horizontal size will increase. This increased size can be compensated for by sinking current from HSMOD. Variation in current at HSMOD from 0 to -120µA will result in a horizontal size variation of 0.02 to 0.69 V at EWDRV. Load variations in the EHT can be compensated for via two possible applications:

1- A parallel capacitor and bleeder are present in the EHT transformer. With a divider and buffer, EHT information can be transferred to HSMOD. This is the best solution, because the signal does not lag in phase. The application at HSMOD can be implemented as shown in Figure 20.5. This divider creates a T1 base voltage of 4.8 V, within the range of the voltage at HSMOD. A decrease of EHT voltage will result in a voltage over R, sinking current from HSMOD. The time constants of the divider (C1*R1 and C2*R2) must be equal. The values for R2 and C2 should be recalculated if the LOT contains other component values for R1 or C1. C2 should have a low leakage current (< 0.1 µA). For a full HSMOD control range with a EHT voltage drop of 10% (2.5kV), the value for R will be 3k9.

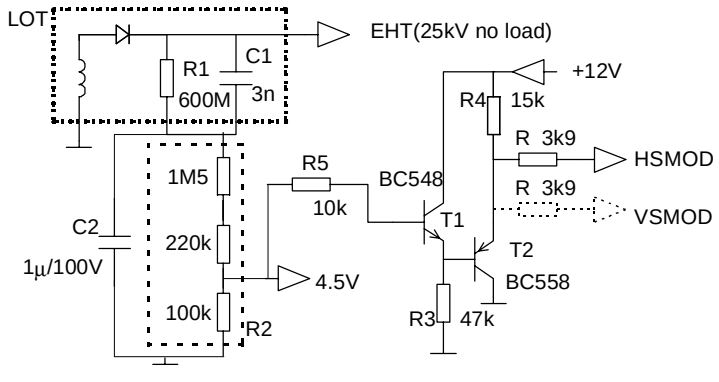


Figure 20.5: HSMOD application with EHT divider

For an optimised dimensioning of R, follow the next steps:

- Adjust horizontal size, pincushion, corner and trapezium correction to optimised values;
- Display a white bar (about 80% width and 30% height);
- Adjust R to an optimised horizontal size correction and apply this value as a fixed resistor.

For optimised alignment, the base of T1 should be set to 4.8 V.

2:

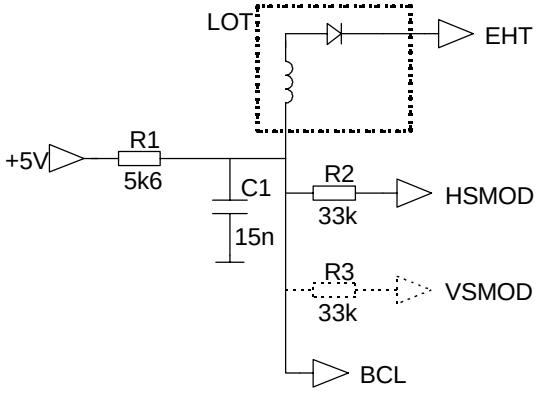


Figure 20.6: Application HSMOD via EHT Current Sense

The footpoint of the EHT transformer (not grounded) can be used for EHT information via a resistor. This solution will, however, result in a HSMOD phase lag and therefor, geometry compensation will not be optimal. The application of HSMOD in this case is depicted in Figure 20.6. The footpoint of the LOT is set to 5 V, equal to the voltage of HSMOD. A variation in beam current from 0 to 700µA will result in a voltage drop over R1 of 700µ*5k6 = 4V. Now, the value for R2 can be calculated, because an equal voltage drop over R2 should sink 120µA from HSMOD: R2 = 4/120µ = 33kΩ. The time constant τ_1, created by R1* C1, should be between horizontal and vertical period ($\tau_1 \approx 0.5$ ms). For an optimised dimensioning of R2 (and R3), follow the next steps:

- Display a cross hatch pattern;
- Adjust horizontal size, pincushion, corner and trapezium correction to optimised values;
- Display a white bar (about 80% width and 30% height);
- Adjust R2 to an optimised horizontal size correction and apply this value as a fixed resistor.

A slight interaction from HSMOD to VSMOD and vice versa is possible. This HSMOD/VSMOD application concept can also be used for beam current limiting (BCL).

20.4 Lay-out

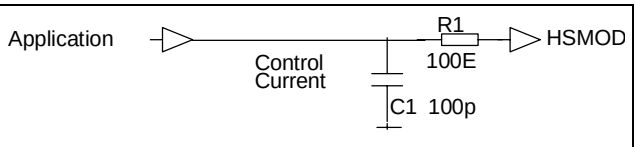


Figure 20.7: EMI filtering HSMOD

In both applications, tracks should be as short as possible, especially the track from resistor to HSMOD. This resistor is ‘R’ in Figure 20.5 and R2 in Figure 20.6. If these tracks are longer then approximately 2 cm, input filtering will be necessary in order to eliminate possible EMI problems. This is done by a current input filter, shown in Figure 20.7, where R1 and C1 should be as close to the input pin as possible.

21. PIN 32: FOCUS (TDA4854 ONLY)

21.1 Characteristics

SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FOCUS maximum output	I_{FOCUS} = 0 mA	5.7	6	6.3	V
FOCUS minimum output	I_{FOCUS} = 0 mA	1.7	2	2.3	V
HFOCUS output swing	register HFOCUS=0_{DEC}	-	0.06	-	V_{pp}
	register HFOCUS=31_{DEC}	-	3.2	-	V_{pp}
VFOCUS output swing	Nominal vertical settings: *VSIZE=127_{DEC} and VOVSCN=0, VSMOD=0µA, VPC=1, VSC=1, VLC=1, HPC=1.* register VFOCUS=0_{DEC}	-	0.02	-	V_{pp}
	Nominal vertical settings register VFOCUS=07_{DEC}	-	0.8	-	V_{pp}
I_{FOCUS} maximum output current		±1.5	-	-	mA
C_{FOCUS} (maximum capacitive load)		-	-	20	pF
$t_{precorr}$	1.9µs < $t_{flyback}$ < 5.5µs	-	350	-	ns
t_{delay} TV-mode	$t_{flyback}$ < 12.5µs	-	300	-	ns

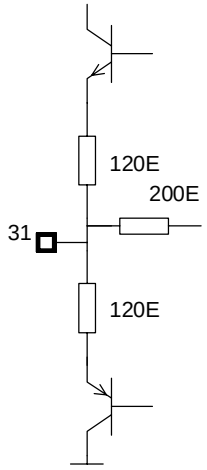


Figure 21.1: Internal pin configuration FOCUS

21.2 Description

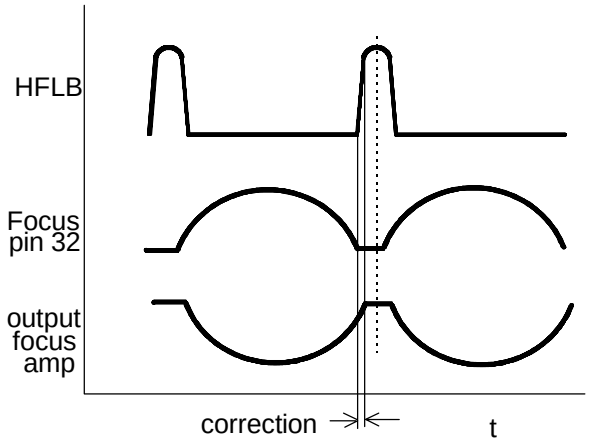


Figure 21.2: Phase advance FOCUS

FOCUS is a voltage output for dynamic focus applications. Both vertical (register VFOCUS) and horizontal (register HFOCUS) parabolas can be adjusted. The horizontal parabola is independent on horizontal frequency, but changing horizontal size may require a correction of HFOCUS. The vertical parabola is frequency-independent and tracks with all vertical adjustments. A phase advance of the horizontal parabola is implemented to compensate for the delay in the external focus amplifier, illustrated in Figure 21.2.

21.3 Application

Pin FOCUS is used to drive a focus amplifier, connected to the Dynamic Focus input of the LOT. Figure 21.3 shows a possible application of the FOCUS pin, in which an optional focus amplifier can be implemented. The inverting amplifier should have a gain of 100-150, determined by R1 and R2. This amplification depends on the tube's focus specification. Capacitor C1 adjusts the delay of the focus amplifier, enabling a correct matching of pre-delay and actual delay. For a more detailed application of a focus amplifier, see Application Note AN97032: 'Circuit Description of CCM420 Monitor' by H. Verhees

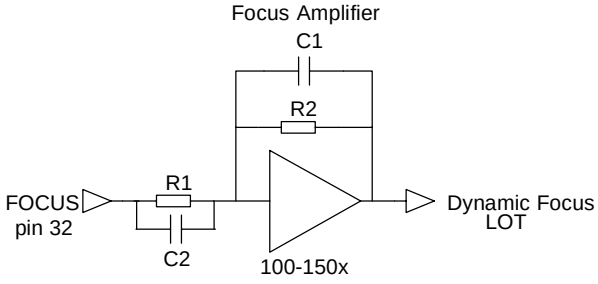


Figure 21.3: Application FOCUS pin

22. INTERNAL ESD PROTECTION

22.1 Pin 4, 11, 12, 13, 16 and 17

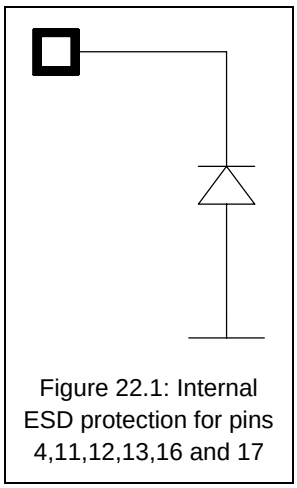


Figure 22.1: Internal ESD protection for pins 4,11,12,13,16 and 17

Pins 4, 11, 12, 13, 16 and 17 have an internal ESD protection circuit as shown in Figure 22.1.

22.2 Pin 2, 3, 5, 18-24 and 26-32

Pins 2, 3, 5, 18-24 and 26-32 have an internal ESD protection circuit as shown in Figure 22.2.

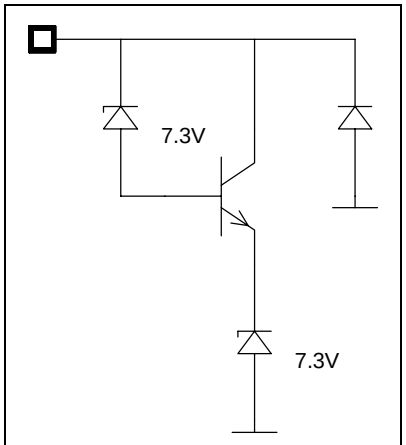


Figure 22.2: Internal ESD protection 2, 3, 5, 18-24 and 26-32

23. I2C SOFTWARE CONTROL

For the software engineers, the flowdiagram given in the data sheet can be simplified.

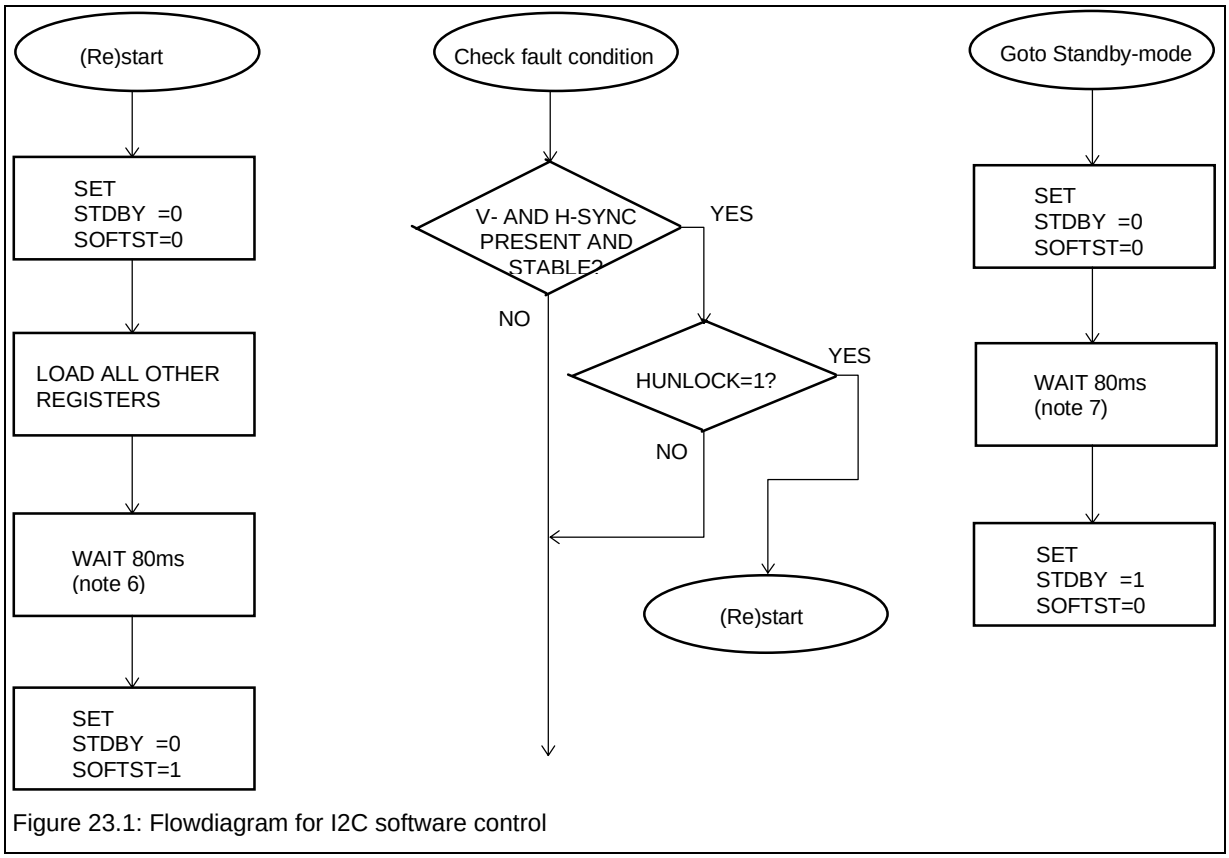


Figure 23.1: Flowdiagram for I2C software control

Notes:

1) If supply voltage < 8.1 Volt, there will be no acknowledge.
2) The IC has no status register; the bits STDBY and SOFTST can be changed internally (e.g. by protection and supply) and externally by I2C, but they can not be read back.
3) Refresh/reload/update is allowed for all registers at all times, except for the command register $0D_{HEX}$.
4) Loading the control bits STDBY and SOFTST =11 is never allowed.
5) Synchronize data transfer with Vsync. This prevents visible disturbances. See also SCL / SDA description (pin 18/19).
6) Allow for the stabilisation of internal operation.
7) Allow for the soft stop of the drive signals HDRV and BDRV.

24. REFERENCES

Ref. 1 ETV/AN96002: 'Modification of 15" Autosync Monitor Mk-II to Positive Flyback Concept' by H. Groot-Hulze, issued November 28 1996

Ref. 2 AN95086: 'PCALE 15" Autosync Monitor Mk-II Circuit Description' by H. Misdom, issued September 5 1995

Ref. 3 Data Handbook IC12: 'I^2C Peripherals', issued October 1995

Ref. 4 ETV8835: 'User's Guide I^2C Control Programs' by A. Demmers, issued December 1988

Ref. 5 AN96091: 'Low Power and Low Cost Horizontal Drive Circuits with U15 Core' by F. Vaneerdewegh, issued August 19 1996

Ref. 6 AN96052: 'B+ Converter Topologies for Horizontal Deflection and EHT Generators' by H. Verhees, issued September 2 1996

Ref. 7 AN97032: 'Circuit Description of CCM420 Monitor' by H. Verhees