PSMN011-60ML

N-channel 60 V 11.3 mΩ logic level MOSFET in LFPAK33

4 June 2013 Product data sheet

1. General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- LFPAK33 package is footprint compatible with other 3.3mm types
- Qualified to 175 °C

3. Applications

- AC-to-DC converters
- Synchronous rectification
- DC-DC converters

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	60	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 1		-	-	61	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	91	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 12		-	9.35	11.3	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C; Fig. 12		-	11	13.1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 15 A; V_{DS} = 30 V; T_j = 25 °C; Fig. 14; Fig. 15		-	5.1	-	nC

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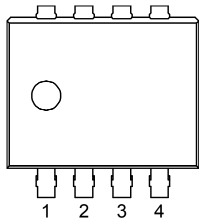
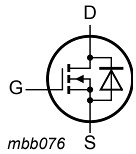
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN011-60ML	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN011-60ML	M11L60

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1		-	61	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1		-	43	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 4		-	242	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	91	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	70	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	242	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 61 A; V_{sup} ≤ 60 V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	48.5	mJ

[1] Continuous current is limited by package

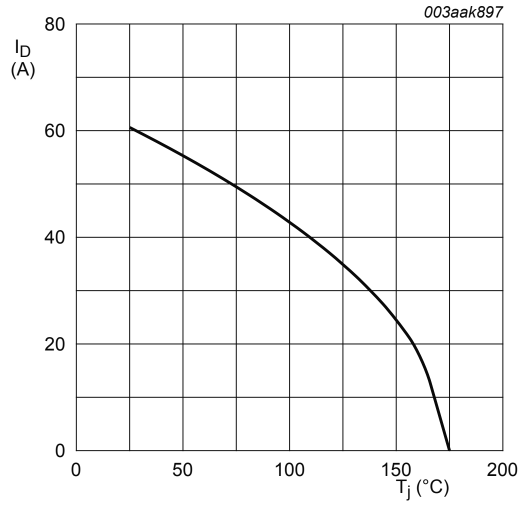

Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10 V$

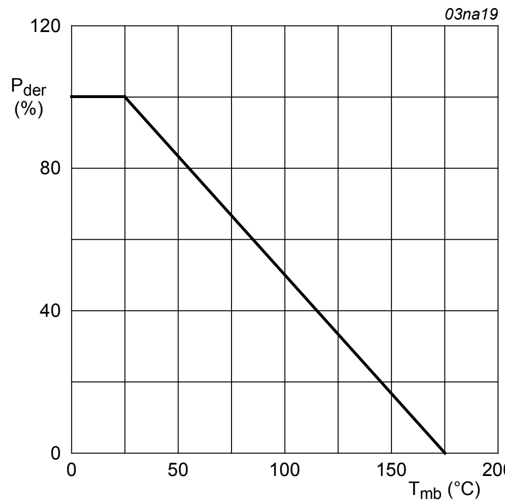

Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

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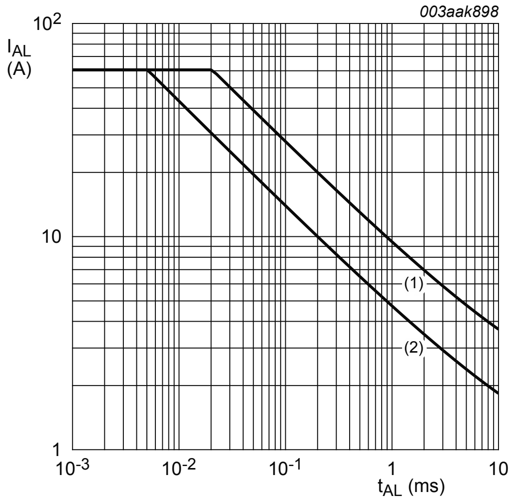

Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\,(init)} = 25°C$; (2) $T_{j\,(init)} = 100°C$

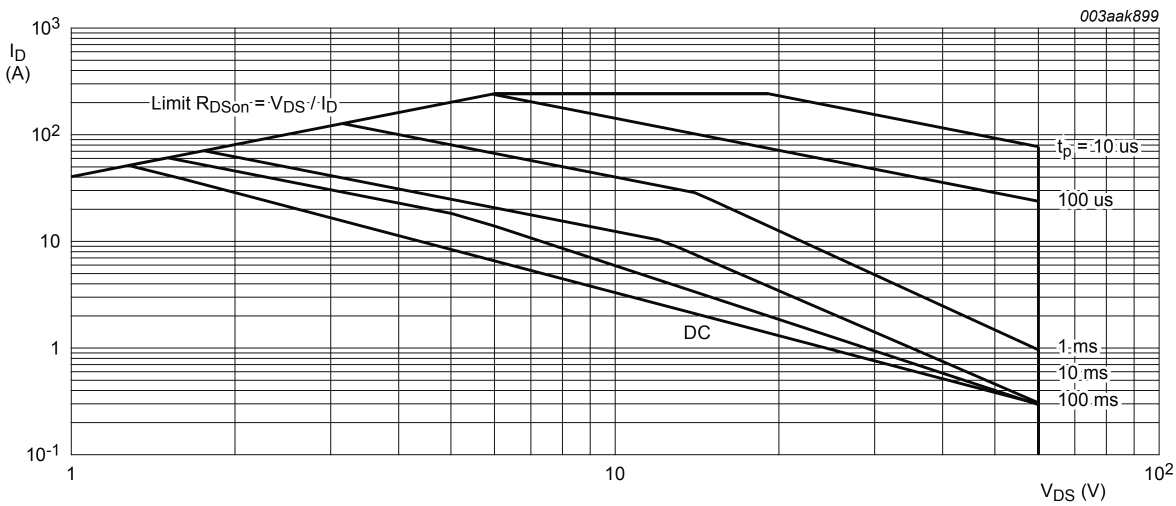

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.44	1.65	K/W

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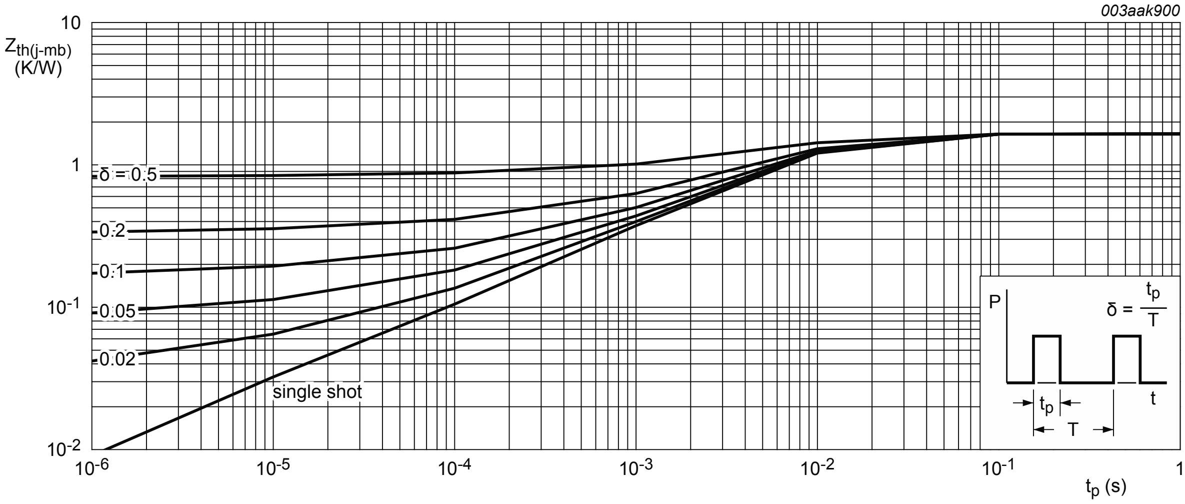

Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 11; Fig. 10		1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	0.03	1	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 12		-	9.35	11.3	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C; Fig. 12		-	11	13.1	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; Fig. 12; Fig. 13		-	-	24.8	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 175 °C; Fig. 12; Fig. 13		-	-	28.8	mΩ
R_G	gate resistance	f = 1 MHz		-	1.86	-	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 30 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	37.2	-	nC
		I_D = 15 A; V_{DS} = 30 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 14; Fig. 15		-	16.6	-	nC
Q_{GS}	gate-source charge			-	5	-	nC
Q_{GD}	gate-drain charge			-	5.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 15 A; V_{DS} = 30 V; T_j = 25 °C; Fig. 14; Fig. 15		-	2.75	-	V
C_{iss}	input capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	2191	-	pF
C_{oss}	output capacitance	V_{DS} 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	199	-	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	111	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 2 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	13.3	-	ns
t_r	rise time			-	20.2	-	ns
$t_{d(off)}$	turn-off delay time			-	27.7	-	ns
t_f	fall time			-	15.5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.84	1.2	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C		-	20.7	-	ns
Q_r	recovered charge			-	15.7	-	nC

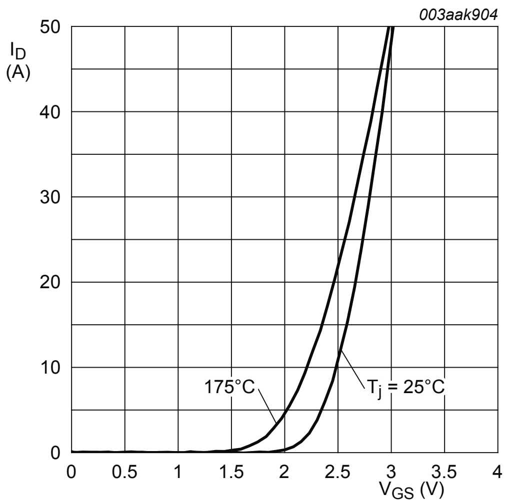
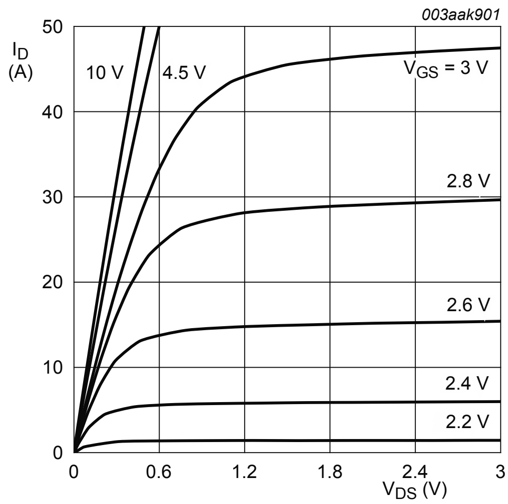


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$



T_j = 25 °C; t_p = 300 µs

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

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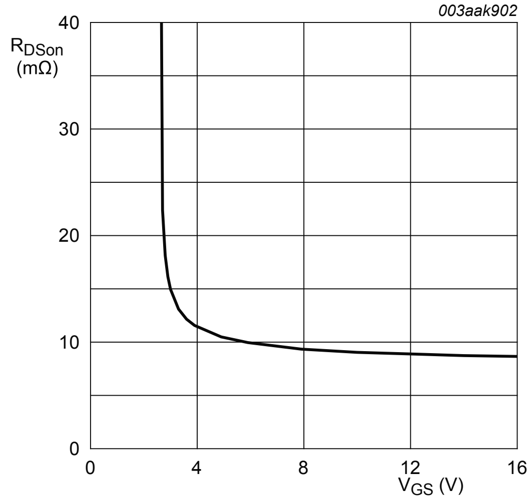

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 15A$

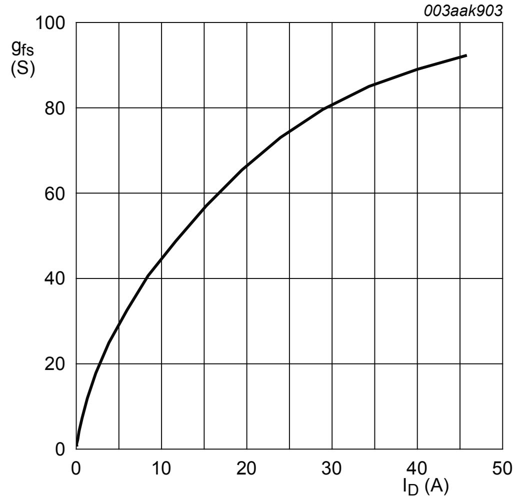

Fig. 9. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

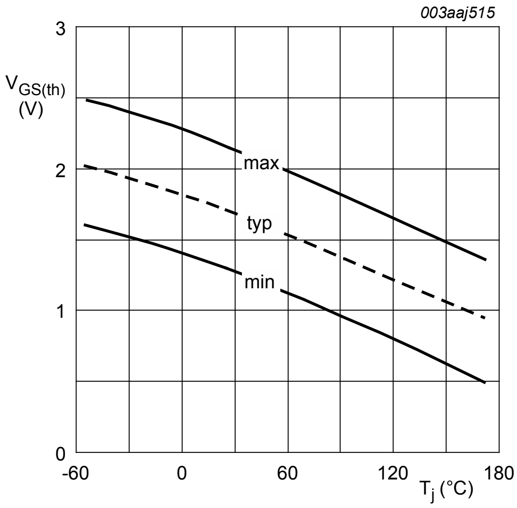

Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1$ mA; $V_{DS} = V_{GS}$

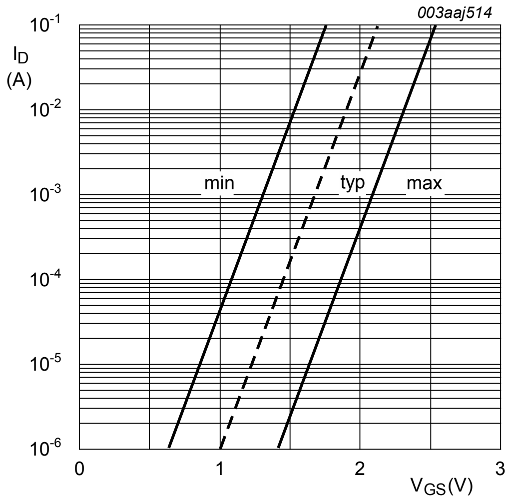

Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C;\ V_{DS} = 5V$

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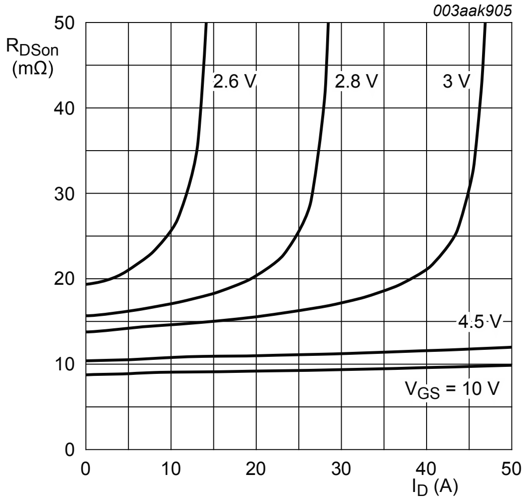

T_j = 25 °C; t_p = 300 μs

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

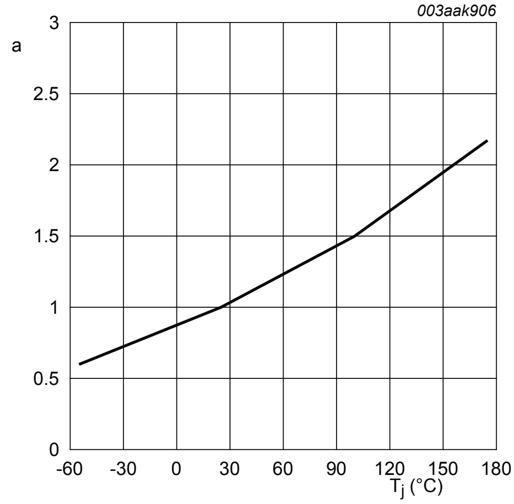

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

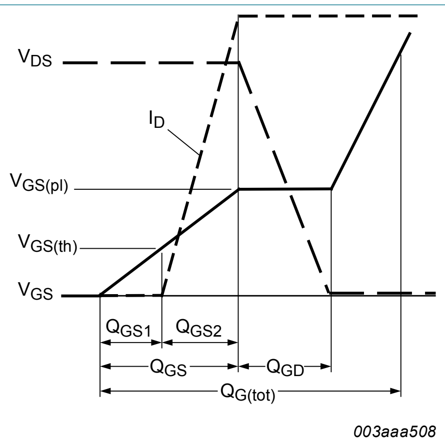

Fig. 14. Gate charge waveform definitions

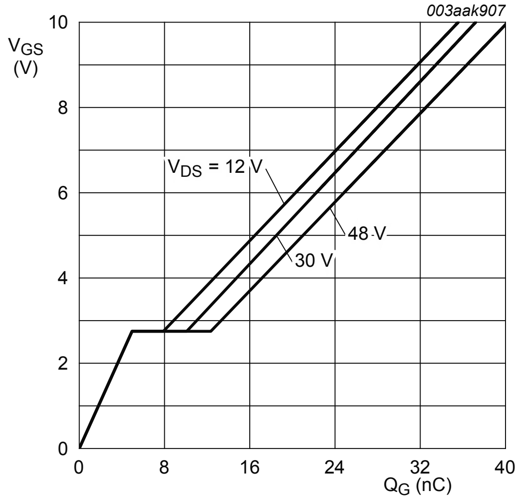

Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 15A$

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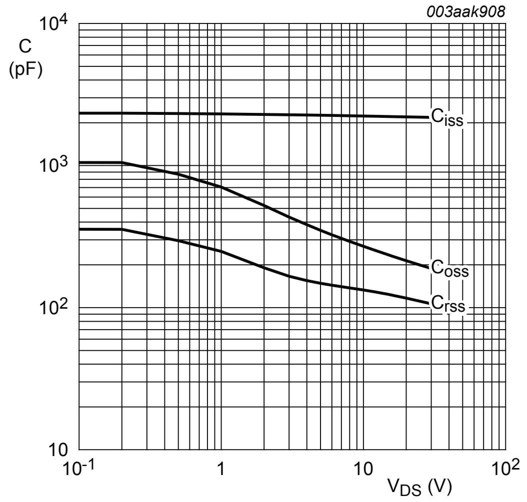

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0 V;\ f = 1 MHz$

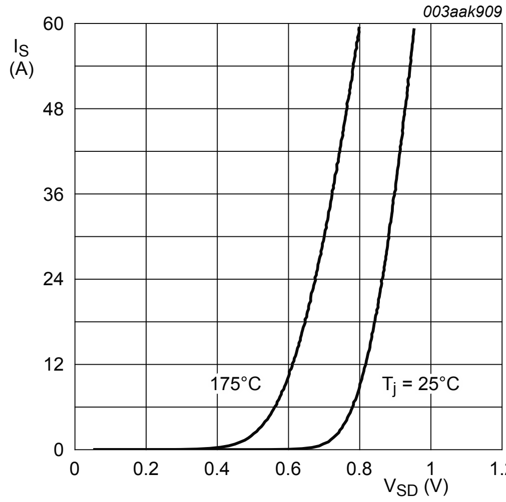

Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0 V$

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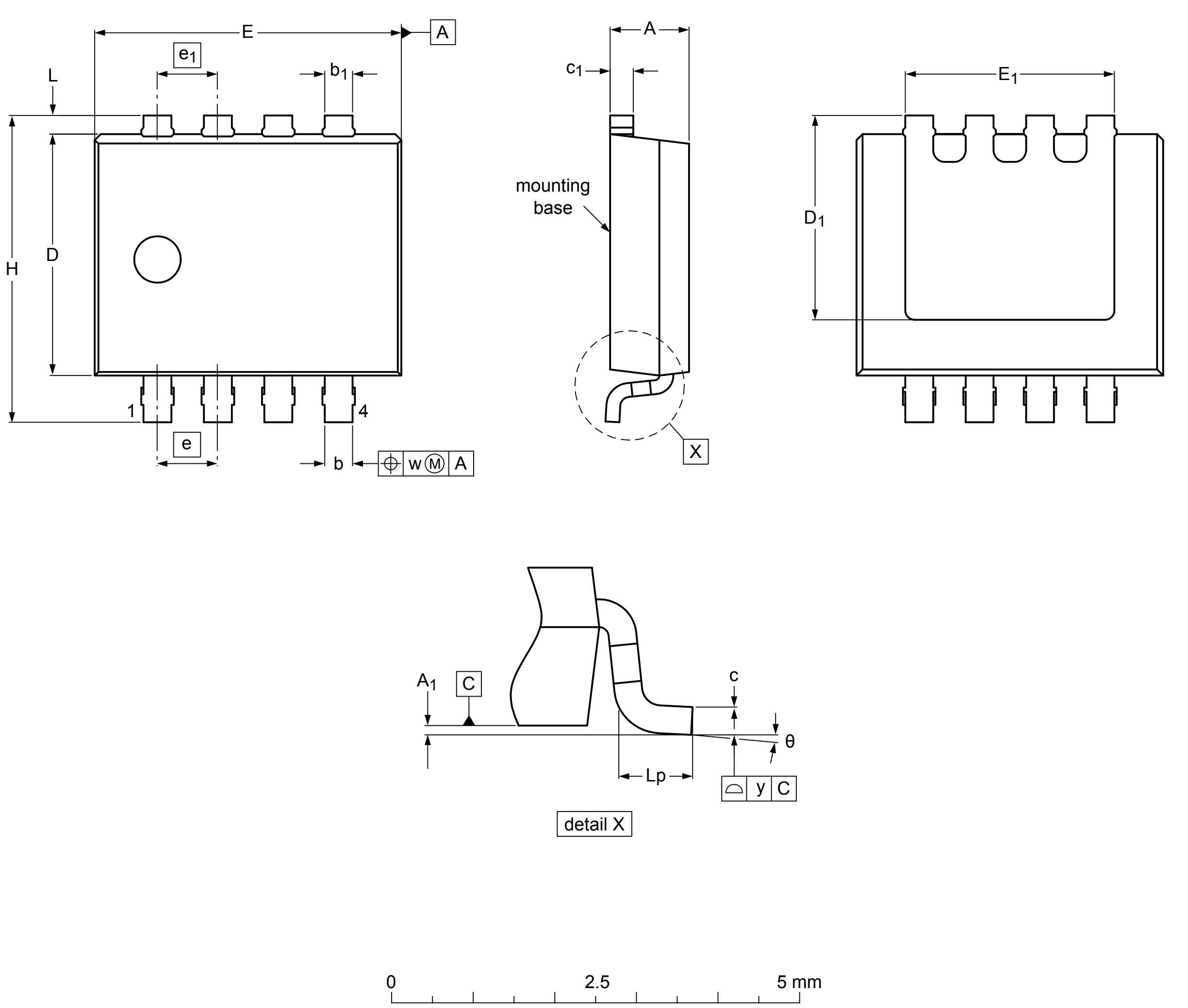
11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b	b_1	c	c_1	D(1)	D_1	E(1)	E_1	e	e_1	H	L	L_p	w	y	θ
mm	max	0.90	0.10	0.35	0.35	0.20	0.30	2.70	2.35	3.40	2.45			3.40	0.25	0.50			8°
	nom											0.65	0.65				0.20	0.10	
	min	0.80	0.00	0.25	0.25	0.10	0.20	2.50	1.90	3.20	2.00			3.20	0.13	0.30			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~11-12-19~~ 12-03-12

Fig. 18. Package outline LFPAK33 (SOT1210)

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12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 4 June 2013